

# DESIGNWARE DW8051 MACROCELL SOLUTION

*The synthesizable DesignWare  
DW8051 MacroCell provides  
up to three times the performance  
of standard 8051 microcontrollers  
while operating at the same  
clock rate.*

## OVERVIEW

The DesignWare® DW8051™ MacroCell is a high-performance, configurable, fully-synthesizable, and reusable 8051 core. It is fully binary compatible with the industry standard 803x/805x microcontrollers.

An encrypted version of the DW8051 MacroCell is available to all DesignWare Foundation Library users at no cost. Unencrypted VHDL and Verilog source code versions are also available. Both the encrypted and source code versions include Synopsys coreConsultant for automatic installation, configuration, simulation, and synthesis of the DW8051.

## HIGH PERFORMANCE AND PORTABILITY

The DesignWare DW8051 MacroCell solution includes the DW8051 MacroCell, a reference design, and our extensive verification environment. The DW8051's high-performance architecture provides up to three times the performance improvement over the standard 8051 when operating at the same clock rate.

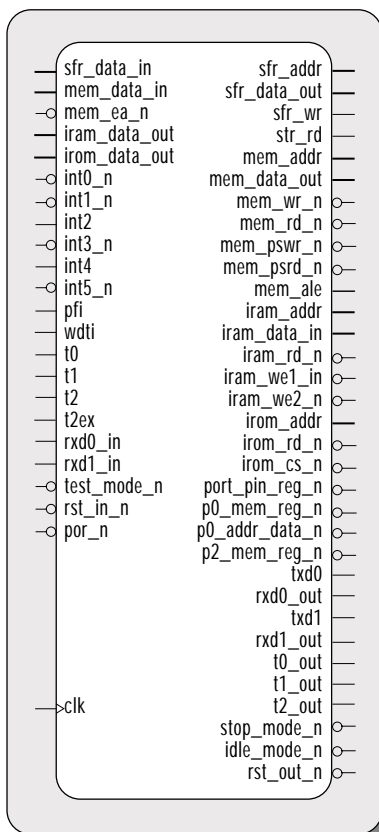
The DW8051 synthesizes automatically through coreConsultant to run at greater than 120 MHz in 0.25-micron processes.

The DW8051 is technology independent and can be implemented in a variety of process technologies. The DW8051 has been fabricated in both ASIC and FPGA technologies.

## PROVEN QUALITY, COMPLETE SOLUTION

To ensure quality, the DW8051 was developed according to Synopsys' strict design-for-reuse methodology. The DW8051 has undergone extensive testing during the design process and has been proven in many different technologies. The DW8051 has also been tested with a variety of third-party 8051 development tools and 8051 evaluation boards.

The DW8051's high-performance, configurable, synthesizable architecture, along with the development environment provided and supported by Synopsys, provide a total solution for building low-cost, high-performance embedded control systems for a wide range of applications.



DW8051 INPUT/OUTPUT SIGNALS

## AUTOMATED DESIGN FLOW WITH SYNOPSIS CORECONSULTANT

The current version of the DW8051 MacroCell solution has been developed and packaged for use with Synopsis coreConsultant. coreConsultant, in turn, provides the following services:

- Automatic installation of the DW8051 coreKit
- Activity checklist that guides you through DW8051 design activities in the correct order
- Automatic, error-free DW8051 configuration, including parameter cross-dependency checking

- Automatic configuration and operation of the DW8051 verification environment
- Automatic, high-quality synthesis with your technology library and your installed version of Design Compiler
- Automatic design checking and synthesis results analysis

You can operate coreConsultant either in its GUI mode (Figure 1) or in batch mode through its command line interface.

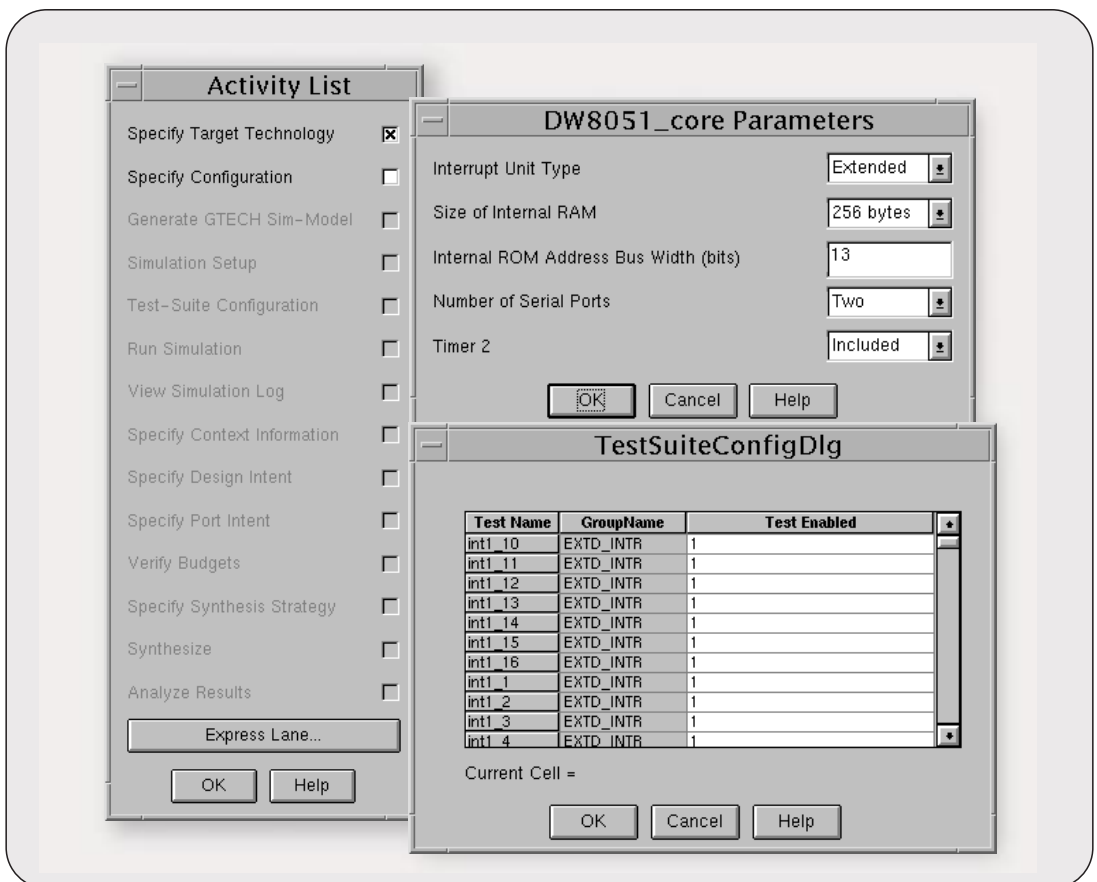
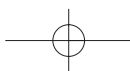


FIGURE 1: EXAMPLE CORECONSULTANT DIALOGS FOR DW8051



## TECHNICAL ADVANTAGES OF THE DW8051

- 4 clocks/instruction cycle versus 12 in standard 8051
  - Up to three times faster execution on average versus standard 8051
- Stretch memory cycle
  - Allows application software to adjust to different external RAM speeds
  - MOVX in as little as eight clock cycles
- Dual data pointers
  - Improves efficiency when moving large blocks of data
- Internal/external peripheral interface
  - Special function register (SFR) bus in DW8051 supports both internal and external peripherals vs. internal only in standard 8051
- Two optional full-duplex serial ports
- Seven additional interrupts
- SFR bus for adding custom peripherals

## DW8051 FEATURES

The DW8051 MacroCell is reusable in design environments that include widely used EDA tools for simulation (e.g., VCS™, VHDL System Simulator™ (VSS), MTI ModelSim, Leapfrog, and Verilog-XL), Synopsys Design Compiler™ for synthesis, and Synopsys Test Compiler™ for test.

### 803x/805x Compatibility

The DW8051 is compatible with the standard 8051 instruction set and can be configured to a wide range of industry standard 803x/805x architectures. Control signals for standard 803x/805x I/O ports are included. Optional full-duplex serial ports and third timer are selectable through parameters.

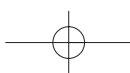
### High-Performance Architecture

DW8051's design is fully static and synchronous. Greater efficiency and performance are achieved by eliminating wasted bus cycles, and by providing dual data pointers for moving large data blocks. The DW8051 core is typically 10k-13k gates depending on configuration and the technology it is implemented in. It runs from 0 megahertz to greater than 120 megahertz. (Clock rates greater than 100 megahertz require a target technology of 0.25 micron or less). Lower performance applications also benefit by being able to run at lower clock rates to get the same performance as a standard 12 clocks/instruction 8051. Lower clock rates lead to lower power consumption and lower electro-magnetic interference (EMI).

### Adding Custom Designed Peripherals

A typical 8051 allows peripheral interface only through port logic. In addition to the ports, the DW8051 also provides direct access to peripherals through the memory and SFR buses (Figure 2):

- You can interface additional peripherals directly to the DW8051's memory bus. This method allows you to make use of the "stretch" memory cycle feature to interface slow peripherals.
- You can also directly attach custom designed peripherals to the efficient SFR bus, the same bus used for interfacing standard DW8051 internal peripherals. SFR addresses that are not used for DW8051 internal SFRs are available for connecting external peripherals. Adding peripherals to the SFR bus offers the following advantages:



- Faster read, write accesses; 1 clock vs. 2 clocks using mem\_bus
- Direct addressing
- Can take advantage of bit manipulation instructions
- Efficient, compact code

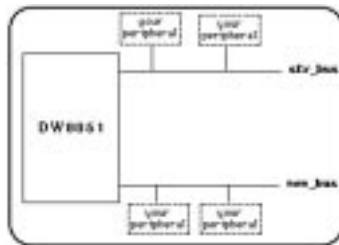


FIGURE 2: DW8051 EXTERNAL SFR AND MEMORY BUSES

**Third-Party Development Tools Support**

Synopsys has an active program in place to support third-party tools. Many industry standard compilers,

assemblers, ROM monitors, and in-circuit emulators have been tested for compatibility with the DW8051. This allows integration of these tools into a design environment and provides a complete development solution for DW8051-based embedded systems on a chip. In-circuit emulation support is provided by Nohau Corporation and Hitex Development Tools.

**DW8051 CONFIGURABLE ARCHITECTURE**

Figure 3 illustrates the hardware architecture of the DW8051 core. The name of the top-level module is DW8051\_core. The internal RAM and ROM modules are located outside DW8051\_core to facilitate simulation and insertion of technology-specific RAM/ROM modules. The following submodules and interfaces are selectable through parameter settings:

- DW8051\_core can address either 128 or 256 bytes of internal RAM
- The internal ROM address range is determined by a parameter (rom\_addr\_size)
- Timer 2 (DW8051\_timer2) is optional
- 0, 1, or 2 serial ports (DW8051\_serial) can be implemented
- The interrupt unit is either DW8051\_intr\_0 (6-source) or DW8051\_intr\_1 (13-source)

coreConsultant automatically generates your selected DW8051 configuration so that no HDL source code editing is necessary.

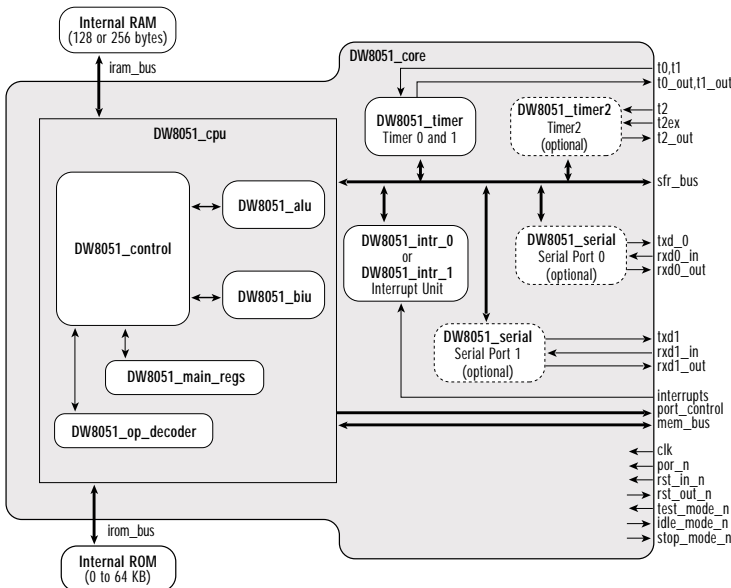
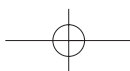


FIGURE 3: DW8051\_core



Feature	Intel				Dallas DS80C320	DesignWare DW8051
	8031	8051	80C32	80C52		
Clocks Per Instruction Cycle	12	12	12	12	4	4
Internal ROM (1)	-	4KB	-	8KB	-	Up to 64KB
Internal RAM (1)	128 bytes	128 bytes	256 bytes	256 bytes	256 bytes	128 bytes or 256 bytes
Data Pointers	1	1	1	1	2	2
Serial Ports	1	1	1	1	2	0, 1, or 2
16-bit Timers	2	2	3	3	3	2 or 3
Interrupt Sources (total of int. and ext.)	5	5	6	6	13	6 or 13
Stretch Memory Cycle	No	No	No	No	Yes	Yes

(1) Internal ROM and RAM are located outside of DW8051\_core.

TABLE 1: FEATURE SUMMARY OF DW8051 AND COMMON 803x/805x CONFIGURATIONS

### 803x/805x FEATURE COMPARISON

Through parameter settings, you can configure the DW8051 hardware to be functionally compatible with a variety of 803x/805x configurations. For example, you can implement two 16-bit timers for compatibility with the Intel 8051, or you can

implement three for compatibility with the Intel 80C32. Table 1 provides a feature-by-feature comparison of the DW8051 MacroCell and several common 803x/805x configurations.

### PERFORMANCE OVERVIEW

The DW8051 processor core offers increased performance by executing instructions in a 4-clock bus cycle, as opposed to the 12-clock bus cycle in the standard 8051 (Figure 4). The shortened bus timing improves the instruction execution rate for most instructions by a factor of three over the standard 8051 architectures.

Some instructions require a different number of instruction cycles on the DW8051 than they do on the standard 8051. In the standard 8051, all

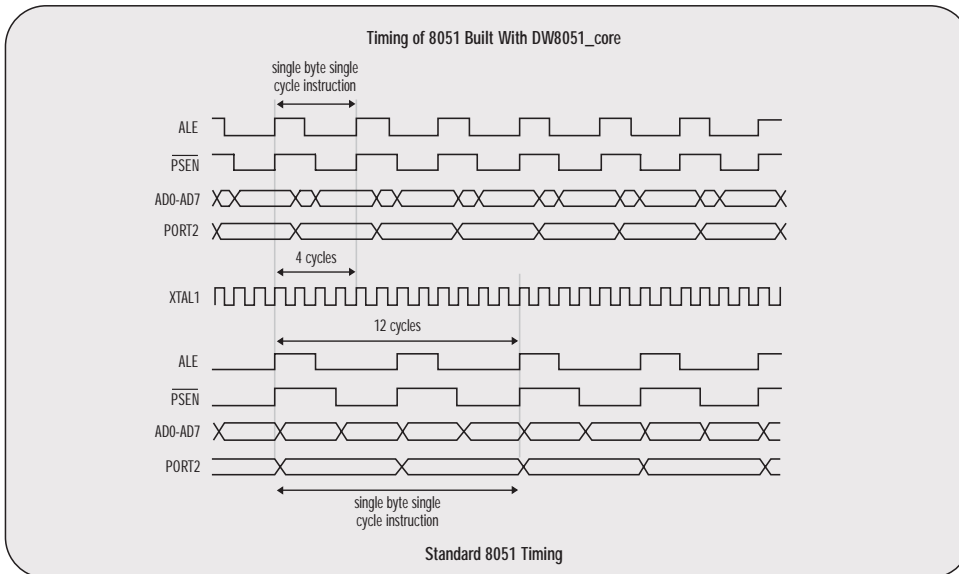
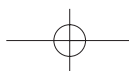


FIGURE 4: INSTRUCTION CYCLE TIMING COMPARISON



instructions except for MUL and DIV take one or two instruction cycles to complete. In the DW8051 architecture, instructions can take between one and five instruction cycles to complete. The average speed improvement for the entire instruction set is approximately two-and-a-half times, calculated as seen in Table 2.

Number of Opcodes	Speed Improvement
150	3.0X
51	1.5X
43	2.0X
2	2.4X

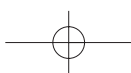
Note: Comparison is for DW8051 and standard 8051 operating at the same clock frequency.

TABLE 2: PERFORMANCE COMPARISON OF DW8051 VS. STANDARD 8051

### DW8051 DEVELOPMENT ENVIRONMENT

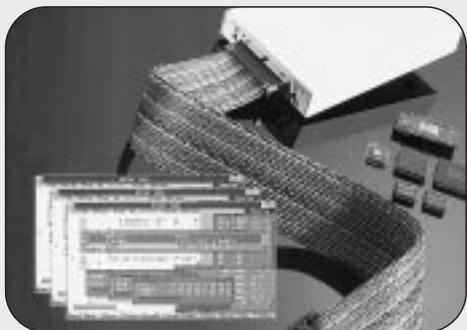
The DW8051 MacroCell solution is developed and packaged for use with Synopsys coreConsultant. The complete DW8051 MacroCell solution coreKit includes:

- The DW8051 MacroCell (DW8051\_core) in either encrypted or (optionally) unencrypted VHDL or Verilog source code
- Multiple-simulator support (e.g., VCS, VSS, MTI ModelSim, Leapfrog, Verilog-XL)
- An example 8032-compatible design
  - This design uses the DW8051\_core and illustrates how to build and connect 8051-compatible port modules for designs where it is preferable to use standard 8051 port modules instead of the 16-bit address memory interface
- Extensive verification environment
  - HDL testbench that instantiates the DW8051\_core, models internal ROM and RAM, and emulates 64 kilobytes of external RAM and 64 kilobytes of external ROM
  - Processes that trace the program counter and write accesses to external RAM
  - A collection of 8051 assembler programs that test all of the instruction set opcodes, plus miscellaneous tests for internal hardware
  - A set of expected results (golden log files)
- Automatic testbench configuration, simulation, and results checking through coreConsultant
- Automatic installation, configuration, simulation, and synthesis of DW8051\_core with Synopsys coreConsultant
- Example test insertion script for Synopsys Test Compiler
- Example CBA library for synthesis
- Complete documentation
  - DW8051 databook in on-line format (PDF), integrated into the coreConsultant on-line help
- Support for third-party development tools
  - Industry standard compilers, assemblers debuggers, ROM monitors, in-circuit emulators from Nohau and Hitex.
  - Keil 8051 software development tools
- Technical support

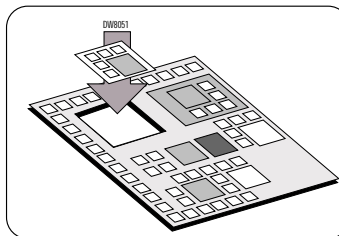


## EMBEDDED SYSTEM DESIGN WITH DW8051

Synopsys provides a complete solution for developing your embedded system-on-a-chip design with the DW8051 MacroCell. For more information, call 1-877-4BEST-IP or email us @ [www.synopsys.com/designware](http://www.synopsys.com/designware).



HITEX ICE SUPPORTS THE DW8051



**TECHNOLOGY  
INDEPENDENT**

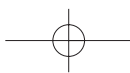
THE DW8051 MACROCELL EMBEDDED SYSTEMS DESIGN PACKAGE



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NOHAU REAL TIME MICROPROCESSOR DEVELOPMENT  
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