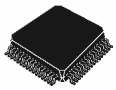
STM32F383xx

ARM Cortex-M4F 32b MCU+FPU, up to 256KB Flash+32KB SRAM timers, 4 ADCs (12/16-bit), 3 DACs, 2 comp., 1.8 V operation

Data brief

Features

- Core: ARM 32-bit Cortex™-M4F CPU (72 MHz max), single-cycle multiplication and HW division, DSP instruction with FPU (floating-point unit) and MPU (memory protection unit)
- Memories
  - 64 to 256 Kbytes of Flash memory
  - 32 Kbytes of SRAM with HW parity check
- CRC calculation unit
- Reset and power management
  - Supply: V_{DD}= 1.8 V +/- 8%, V_{DDA}= 1.65 - 3.6 V
  - External POR pin
  - Low power modes: Sleep, Stop
- Clock management
  - 4 to 32 MHz crystal oscillator
  - 32 kHz oscillator for RTC with calibration
  - Internal 8 MHz RC with x16 PLL option
  - Internal 40 kHz oscillator
- Up to 84 fast I/Os
  - All mappable on external interrupt vectors
  - Up to 45 I/Os with 5 V tolerant capability
- 12-channel DMA controller
- One 12-bit, 1.0 µs ADC (up to 16 channels)
  - Conversion range: 0 to 3.6 V
  - Separate analog supply from 2.4 up to 3.6
- Up to three 16-bit Sigma Delta ADC
  - Separate analog supply from 2.2 to 3.6 V, up to 21 single/ 11 diff channels
- Up to three 12-bit DAC channels
- Two fast rail-to-rail analog comparators with programmable input and output with analog supply from 1.65 to 3.6 V
- Up to 24 capacitive sensing channels supporting touchkey, linear and rotary touchsensors



LQFP48 (7 × 7 mm)
LQFP64 (10 × 10 mm)
LQFP100 (14 × 14 mm)

WLCSP66
(0.400 mm)

UFBGA100
(7 x 7 mm)

- 17 timers
  - Two 32-bit timer and three 16-bit timers with up to 4 IC/OC/PWM or pulse counter
  - Two 16-bit timers with up to 2 IC/OC/PWM or pulse counter
  - Four 16-bit timers with up to 1 IC/OC/PWM or pulse counter
  - Independent and system watchdog timers
  - SysTick timer: 24-bit downcounter
  - Three 16-bit basic timers to drive the DAC
- Calendar RTC with Alarm and periodic wakeup from Stop
- Communication interfaces
  - CAN interface (2.0B Active)
  - Two I2C interfaces; one supporting Fast Mode Plus (1 Mbit/s) with 20 mA current sink, SMBus/PMBus, wakeup from STOP
  - Three USARTs supporting master synchronous SPI and modem control; with ISO7816 interface, LIN, IrDA capability, auto baud rate detection, wakeup feature
  - Three SPIs (18 Mbit/s) with 4 to 16 programmable bit frame, muxed I2S
  - HDMI-CEC bus interface
- Serial wire devices, JTAG, Cortex-M4F ETM
- 96-bit unique ID

Table 1. Device summary

Reference	Part number
STM32F383xx	STM32F383CC, STM32F383RC, STM32F383VC

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1 Introduction

This databrief provides the ordering information and mechanical device characteristics of the STM32F38x microcontrollers.

This STM32F38x databrief should be read in conjunction with the STM32F38x reference manual. The reference manual is available from the STMicroelectronics website www.st.com.

For information on the Cortex™-M4F core please refer to the Cortex™-M4F Technical Reference Manual, available from the www.arm.com website at the following address: http://infocenter.arm.com/help/index.jsp?topic=/com.arm.doc.subset.cortexm.m4/index.html

2 Description

The STM32F38x family is based on the high-performance ARM® Cortex™-M4F 32-bit RISC core operating at a frequency of up to 72 MHz, and embedding a floating point unit (FPU), a memory protection unit (MPU) and an embedded trace macrocell (ETM). The family incorporates high-speed embedded memories (up to 256 Kbyte of Flash memory, up to 32 Kbytes of SRAM), and an extensive range of enhanced I/Os and peripherals connected to two APB buses.

The STM32F38x devices offer one fast 12-bit ADC (1 Msps), up to three 16-bit Sigma delta ADCs, up to two Comparators, up to two DACs (DAC1 with 2 channels and DAC2 with 1 channel), a low-power RTC, 9 general-purpose 16-bit timers, two general-purpose 32-bit timers, three basic timers.

They also feature standard and advanced communication interfaces: up to two I2Cs, three SPIs, all with muxed I2Ss, three USARTs, CAN.

The STM32F38x family operates in the -40 to +85 °C and -40 to +105 °C temperature ranges from a 1.8 V +/- 8% power supply. A comprehensive set of power-saving mode allows the design of low-power applications.

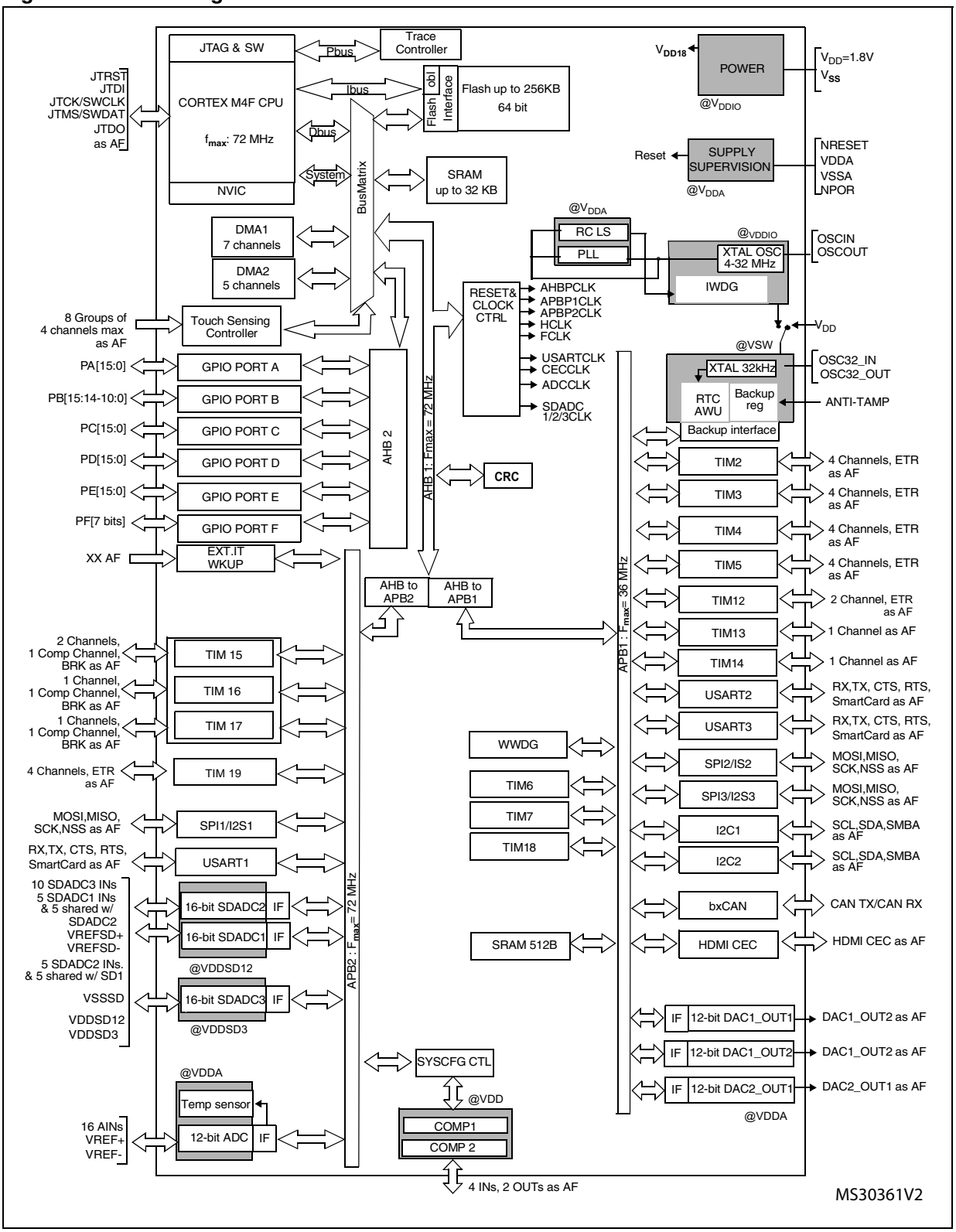
The STM32F38x family offers devices in five packages ranging from 48 pins to 100 pins. The set of included peripherals changes with the device chosen.

Table 2. Device overview

Peripheral		STM32F 383Cx			STM32F 383Rx			STM32F 383Vx		
Flash (Kbytes)		64	128	256	64	128	256	64	128	256
SRAM (Kbytes)		16	24	32	16	24	32	16	24	32
Timers	General purpose	9 (16-bit) 2 (32 bit)								
	Basic	3 (16-bit)								
Comm. interfaces	SPI/I2S	3								
	I^2C	2								
	USART	3								
	CAN	1								
GPIOs	Normal I/Os (TC, TTa)	36			52			84		
	5 volts Tolerant I/Os (FT, Ftf)	20			28			45		
12-bit ADCs		1								
16-bit ADCs Sigma- Delta		3								
12-bit DACs outputs		3								
Analog comparator		2								
CPU frequency		72 MHz								
Main operating voltage		1.8 V +/- 8%								
16-bit SDADC operating voltage		2.2 to 3.6 V								
Operating temperature		Ambient operating temperature: −40 to 85 °C / −40 to 105 °C Junction temperature: −40 to 125 °C								
Packages		LQFP48			LQFP64, WLCSP66			LQFP100, UFBGA100(1)		

1. UFBGA100 package available on 256-KB versions only.

Figure 1. Block diagram



1. AF: alternate function on I/O pins.
2. Example given for STM32F383xx device.

3 Functional overview

3.1 ARM® Cortex™-M4F core with embedded Flash and SRAM

The ARM Cortex-M4F processor is the latest generation of ARM processors for embedded systems. It was developed to provide a low-cost platform that meets the needs of MCU implementation, with a reduced pin count and low-power consumption, while delivering outstanding computational performance and an advanced response to interrupts.

The ARM Cortex-M4F 32-bit RISC processor features exceptional code-efficiency, delivering the high-performance expected from an ARM core in the memory size usually associated with 8- and 16-bit devices.

The processor supports a set of DSP instructions which allow efficient signal processing and complex algorithm execution.

Its single precision FPU speeds up software development by using metalanguage development tools, while avoiding saturation.

With its embedded ARM core, the STM32F38x family is compatible with all ARM tools and software.

Figure 1 shows the general block diagram of the STM32F38x family.

3.2 Memory protection unit

The memory protection unit (MPU) is used to separate the processing of tasks from the data protection. The MPU can manage up to 8 protection areas that can all be further divided up into 8 subareas. The protection area sizes are between 32 bytes and the whole 4 gigabytes of addressable memory.

The memory protection unit is especially helpful for applications where some critical or certified code has to be protected against the misbehavior of other tasks. It is usually managed by an RTOS (real-time operating system). If a program accesses a memory location that is prohibited by the MPU, the RTOS can detect it and take action. In an RTOS environment, the kernel can dynamically update the MPU area setting, based on the process to be executed.

The MPU is optional and can be bypassed for applications that do not need it.

The Cortex-M4F processor is a high performance 32-bit processor designed for the microcontroller market. It offers significant benefits to developers, including:

- Outstanding processing performance combined with fast interrupt handling
- Enhanced system debug with extensive breakpoint and trace capabilities
- Efficient processor core, system and memories
- Ultralow power consumption with integrated sleep modes
- Platform security robustness with optional integrated memory protection unit (MPU).

With its embedded ARM core, the STM32F38x devices are compatible with all ARM development tools and software.

3.3 Embedded Flash memory

All STM32F38x devices feature up to 256 Kbytes of embedded Flash memory available for storing programs and data. The Flash memory access time is adjusted to the CPU clock frequency (0 wait state from 0 to 24 MHz, 1 wait state from 24 to 48 MHz and 2 wait states above).

3.4 CRC (cyclic redundancy check) calculation unit

The CRC (cyclic redundancy check) calculation unit is used to get a CRC code using a configurable generator polynomial value and size.

Among other applications, CRC-based techniques are used to verify data transmission or storage integrity. In the scope of the EN/IEC 60335-1 standard, they offer a means of verifying the Flash memory integrity. The CRC calculation unit helps compute a signature of the software during runtime, to be compared with a reference signature generated at linktime and stored at a given memory location.

3.5 Embedded SRAM

All STM32F38x devices feature up to 32 Kbytes of embedded SRAM with hardware parity check. The memory can be accessed in read/write at CPU clock speed with 0 wait states.

3.6 Boot modes

At startup, Boot0 pin and Boot1 option bit are used to select one of three boot options:

- Boot from user Flash
- Boot from system memory
- Boot from embedded SRAM

The boot loader is located in system memory. It is used to reprogram the Flash memory by using USART1, USART2 or I2C.

3.7 Power management

3.7.1 Power supply schemes

- V_{DD}: external power supply for I/Os and core. It is provided externally through V_{DD} pins, and can be 1.8 V +/- 8%.
- V_{DDA} = 1.65 to 3.6 V:
  - external analog power supplies for Reset blocks, RCs and PLL
  - supply voltage for 12-bit ADC, DACs and comparators (minimum voltage to be applied to V_{DDA} is 2.4 V when the 12-bit ADC and DAC are used).
- VDDSD12 and VDDSD3= 2.2 V to 3.6: supply voltages for SDADC1/2 and SDADCD3 sigma delta ADCs. Independent from V_{DD}/V_{DDA}.

3.7.2 Power supply supervisor

Device power on reset is controlled through the external NPOR pin. The device remains in reset mode when NPOR is held low. NPOR pin has an internal pull-up resistor so the external driver can be open drain type.

To guarantee a proper power-on reset, the NPOR pin must be held low until V_{DD} is stable.

When V_{DD} is stable, the reset state can be exited by:

- either putting the NPOR pin in high impedance. NPOR pin has an internal pull up.
- or forcing the pin to high level by connecting it to V_{DDA}.

3.7.3 Low-power modes

The STM32F38x supports two low-power modes to achieve the best compromise between low power consumption, short startup time and available wakeup sources:

- **Sleep mode**

  In Sleep mode, only the CPU is stopped. All peripherals continue to operate and can wake up the CPU when an interrupt/event occurs.

- **Stop mode**

  Stop mode achieves the lowest power consumption while retaining the content of SRAM and registers. All clocks in the 1.8 V domain are stopped, the PLL, the HSI RC and the HSE crystal oscillators are disabled.

  The device can be woken up from Stop mode by any of the EXTI line. The EXTI line source can be one of the 16 external lines, the PVD output, the USARTs, the I2Cs, the CEC and the RTC alarm.

3.8 Clocks and startup

System clock selection is performed on startup, however the internal RC 8 MHz oscillator is selected as default CPU clock on reset. An external 4-32 MHz clock can be selected, in which case it is monitored for failure. If failure is detected, the system automatically switches back to the internal RC oscillator. A software interrupt is generated if enabled. Similarly, full interrupt management of the PLL clock entry is available when necessary (for example with failure of an indirectly used external oscillator).

Several prescalers allow to configure the AHB frequency, the high speed APB (APB2) and the low speed APB (APB1) domains. The maximum frequency of the AHB and the high speed APB domains is 72 MHz, while the maximum allowed frequency of the low speed APB domain is 36 MHz.

3.9 GPIOs (general-purpose inputs/outputs)

Each of the GPIO pins can be configured by software as output (push-pull or open-drain), as input (with or without pull-up or pull-down) or as peripheral alternate function. Most of the GPIO pins are shared with digital or analog alternate functions. All GPIOs are high current capable except for analog inputs.

The I/Os alternate function configuration can be locked if needed following a specific sequence in order to avoid spurious writing to the I/Os registers.

Do not reconfigure GPIO pins which are not present on 48 and 64 pin packages to the analog mode. Additional current consumption in the range of tens of µA per pin can be observed if V_{DDA} is higher than V_{DDIO}.

3.10 DMA (direct memory access)

The flexible 12-channel, general-purpose DMA is able to manage memory-to-memory, peripheral-to-memory and memory-to-peripheral transfers. The DMA controller supports circular buffer management, avoiding the generation of interrupts when the controller reaches the end of the buffer.

Each channel is connected to dedicated hardware DMA requests, with software trigger support for each channel. Configuration is done by software and transfer sizes between source and destination are independent.

The two DMAs can be used with the main peripherals: SPIs, I2Cs, USARTs, DACs, ADC, SDADCs, general-purpose timers.

3.11 Interrupts and events

3.11.1 Nested vectored interrupt controller (NVIC)

The STM32F38x devices embed a nested vectored interrupt controller (NVIC) able to handle up to 60 maskable interrupt channels and 16 priority levels.

The NVIC benefits are the following:

- Closely coupled NVIC gives low latency interrupt processing
- Interrupt entry vector table address passed directly to the core
- Closely coupled NVIC core interface
- Allows early processing of interrupts
- Processing of late arriving higher priority interrupts
- Support for tail chaining
- Processor state automatically saved
- Interrupt entry restored on interrupt exit with no instruction overhead

The NVIC hardware block provides flexible interrupt management features with minimal interrupt latency.

3.11.2 Extended interrupt/event controller (EXTI)

The extended interrupt/event controller consists of 29 edge detector lines used to generate interrupt/event requests and wake-up the system. Each line can be independently configured to select the trigger event (rising edge, falling edge, both) and can be masked independently. A pending register maintains the status of the interrupt requests. The EXTI can detect an external line with a pulse width shorter than the internal clock period. Up to 84 GPIOs can be connected to the 16 external interrupt lines.

3.12 12-bit ADC (analog-to-digital converter)

The 12-bit analog-to-digital converter is based on a successive approximation register (SAR) architecture. It has up to 16 external channels (AIN15:0) and 3 internal channels (temperature sensor, voltage reference, $V_{BAT} = V_{DD}$ voltage measurement) performing conversions in single-shot or scan modes. In scan mode, automatic conversion is performed on a selected group of analog inputs.

The ADC can be served by the DMA controller.

An analog watchdog feature allows very precise monitoring of the converted voltage of one, some or all selected channels. An interrupt is generated when the converted voltage is outside the programmed thresholds.

The events generated by the timers (TIMx) can be internally connected to the ADC start and injection trigger, respectively, to allow the application to synchronize A/D conversion and timers.

3.12.1 Temperature sensor

The temperature sensor (TS) generates a voltage V_{SENSE} that varies linearly with temperature.

The temperature sensor is internally connected to the ADC_IN16 input channel which is used to convert the sensor output voltage into a digital value.

The sensor provides good linearity but it has to be calibrated to obtain good overall accuracy of the temperature measurement. As the offset of the temperature sensor varies from chip to chip due to process variation, the uncalibrated internal temperature sensor is suitable for applications that detect temperature changes only.

To improve the accuracy of the temperature sensor measurement, each device is individually factory-calibrated by ST. The temperature sensor factory calibration data are stored by ST in the system memory area, accessible in read-only mode.

Table 3. Temperature sensor calibration values

Calibration value name	Description	Memory address
TS_CAL1	TS ADC raw data acquired at temperature of 30 °C, V_{DDA}= 3.3 V	0x1FFF F7B8 - 0x1FFF F7B9
TS_CAL2	TS ADC raw data acquired at temperature of 110 °C V_{DDA}= 3.3 V	0x1FFF F7C2 - 0x1FFF F7C3

3.12.2 Internal voltage reference (V_{REFINT})

The internal voltage reference (V_{REFINT}) provides a stable (bandgap) voltage output for the ADC and Comparators. V_{REFINT} is internally connected to the ADC_IN17 input channel. The precise voltage of V_{REFINT} is individually measured for each part by ST during production test and stored in the system memory area. It is accessible in read-only mode.

Table 4. Temperature sensor calibration values

Calibration value name	Description	Memory address
VREFINT_CAL	Raw data acquired at temperature of 30 °C V_{DDA}= 3.3 V	0x1FFF F7BA - 0x1FFF F7BB

3.13 16-bit sigma delta analog-to-digital converters (SDADC)

Up to three 16-bit sigma-delta analog-to-digital converters are embedded in the STM32F38x. They have up to two separate supply voltages allowing the analog function voltage range to be independent from the STM32F38x power supply. They share up to 21 input pins which may be configured in any combination of single-ended (up to 21) or differential inputs (up to 11).

The conversion speed is up to 16.6 ksps for each SDADC when converting multiple channels and up to 50 ksps per SDADC if single channel conversion is used. There are two conversion modes: single conversion mode or continuous mode, capable of automatically scanning any number of channels. The data can be automatically stored in a system RAM buffer, reducing the software overhead.

A timer triggering system can be used in order to control the start of conversion of the three SDADCs and/or the 12-bit fast ADC. This timing control is very flexible, capable of triggering simultaneous conversions or inserting a programmable delay between the ADCs.

Up to two external reference pins (VREFSD+, VREFSD-) and an internal 1.2/1.8V reference can be used in conjunction with a programmable gain (x0.5 to x32) in order to fine-tune the input voltage range of the SDADC.

3.14 DAC (digital-to-analog converter)

The devices feature up to two 12-bit buffered DACs with three output channels that can be used to convert three digital signals into three analog voltage signal outputs. The internal structure is composed of integrated resistor strings and an amplifier in inverting configuration.

This digital Interface supports the following features:

- Up to two DAC converters with three output channels:
  - DAC1 with two output channels
  - DAC2 with one output channel.
- 8-bit or 12-bit monotonic output
- Left or right data alignment in 12-bit mode
- Synchronized update capability
- Noise-wave generation
- triangular-wave generation
- Dual DAC channel independent or simultaneous conversions (DAC1 only)
- DMA capability for each channel
- External triggers for conversion

3.15 Fast comparators

The STM32F38x embeds up to 2 comparators with rail-to-rail inputs and high-speed output. The reference voltage can be internal or external (delivered by an I/O).

The threshold can be one of the following:

- DACs channel outputs
- External I/O
- Internal reference voltage (V_{REFINT}) or submultiple (1/4 V_{REFINT}, 1/2 V_{REFINT} and 3/4 V_{REFINT})

The comparators can be combined into a window comparator.

Both comparators can wake up the device from Stop mode and generate interrupts and breaks for the timers.

3.16 Touch sensing controller (TSC)

The device has an embedded independent hardware controller (TSC) for controlling touch sensing acquisitions on the I/Os.

Up to 24 touch sensing electrodes can be controlled by the TSC. The touch sensing I/Os are organized in 8 acquisition groups, with up to 4 I/Os in each group.

Table 5. Capacitive sensing GPIOs available on STM32F38x devices

Pin name	Capacitive sensing signal name	Pin name	Capacitive sensing signal name
PA0	TSC_G1_IO1	PA9	TSC_G4_IO1
PA1	TSC_G1_IO2	PA10	TSC_G4_IO2
PA2	TSC_G1_IO3	PA13	TSC_G4_IO3
PA3	TSC_G1_IO4	PA14	TSC_G4_IO4
PA4	TSC_G2_IO1	PB3	TSC_G5_IO1
PA5	TSC_G2_IO2	PB4	TSC_G5_IO2
PA6	TSC_G2_IO3	PB6	TSC_G5_IO3
PA7	TSC_G2_IO4	PB7	TSC_G5_IO4
PC4	TSC_G3_IO1	PB14	TSC_G6_IO1
PC5	TSC_G3_IO2	PB15	TSC_G6_IO2
PB0	TSC_G3_IO3	PD8	TSC_G6_IO3
PB1	TSC_G3_IO4	PD9	TSC_G6_IO4
PE2	TSC_G7_IO1	PD12	TSC_G8_IO1
PE3	TSC_G7_IO2	PD13	TSC_G8_IO2
PE4	TSC_G7_IO3	PD14	TSC_G8_IO3
PE5	TSC_G7_IO4	PD15	TSC_G8_IO4

Table 6. No. of capacitive sensing channels available on STM32F38x devices

Analog I/O group	Number of capacitive sensing channels		
	STM32F38xCx	STM32F38xRx	STM32F38xVx
G1	3	3	3
G2	2	3	3
G3	1	3	3
G4	3	3	3
G5	3	3	3
G6	2	2	3
G7	0	0	3
G8	0	0	3
Number of capacitive sensing channels	14	17	24

3.17 Timers and watchdogs

The STM32F38x includes two 32-bit and nine 16-bit general-purpose timers, three basic timers, two watchdog timers and a SysTick timer. The table below compares the features of the advanced control, general purpose and basic timers.

Table 7. Timer feature comparison

Timer type	Timer	Counter resolution	Counter type	Prescaler factor	DMA request generation	Capture/ compare Channels	Complementary outputs
General-purpose	TIM2 TIM5	32-bit	Up, Down, Up/Down	Any integer between 1 and 65536	Yes	4	0
General-purpose	TIM3, TIM4, TIM19	16-bit	Up, Down, Up/Down	Any integer between 1 and 65536	Yes	4	0
General-purpose	TIM12	16-bit	Up	Any integer between 1 and 65536	No	2	0
General-purpose	TIM15	16-bit	Up	Any integer between 1 and 65536	Yes	2	1
General-purpose	TIM13, TIM14	16-bit	Up	Any integer between 1 and 65536	No	1	0

Table 7. Timer feature comparison (continued)

Timer type	Timer	Counter resolution	Counter type	Prescaler factor	DMA request generation	Capture/ compare Channels	Complementary outputs
General-purpose	TIM16, TIM17	16-bit	Up	Any integer between 1 and 65536	Yes	1	1
Basic	TIM6, TIM7, TIM18	16-bit	Up	Any integer between 1 and 65536	Yes	0	0

3.17.1 General-purpose timers (TIM2 to TIM5, TIM12 to TIM17, TIM19)

There are eleven synchronizable general-purpose timers embedded in the STM32F38x (see *Table 7* for differences). Each general-purpose timer can be used to generate PWM outputs, or act as a simple time base.

- TIM2, 3, 4, 5 and 19

  These five timers are full-featured general-purpose timers:

  – TIM2 and TIM5 have 32-bit auto-reload up/downcounters and 32-bit prescalers

  – TIM3, 4, and 19 have 16-bit auto-reload up/downcounters and 16-bit prescalers.

  These timers all feature 4 independent channels for input capture/output compare, PWM or one-pulse mode output. They can work together, or with the other general-purpose timers via the Timer Link feature for synchronization or event chaining.

  The counters can be frozen in debug mode.

  All have independent DMA request generation and support quadrature encoders.

- TIM12, 13, 14, 15, 16, 17

  These six timers general-purpose timers with mid-range features:

  They have 16-bit auto-reload upcounters and 16-bit prescalers.

  – TIM12 has 2 channels

  – TIM13 and TIM14 have 1 channel

  – TIM15 has 2 channels and 1 complementary channel

  – TIM16 and TIM17 have 1 channel and 1 complementary channel

  All channels can be used for input capture/output compare, PWM or one-pulse mode output.

  The timers can work together via the Timer Link feature for synchronization or event chaining. The timers have independent DMA request generation.

  The counters can be frozen in debug mode.

3.17.2 Basic timers (TIM6, TIM7, TIM18)

These timers are mainly used for DAC trigger generation. They can also be used as a generic 16-bit time base.

3.17.3 Independent watchdog (IWDG)

The independent watchdog is based on a 12-bit downcounter and 8-bit prescaler. It is clocked from an independent 40 kHz internal RC and as it operates independently from the main clock, it can operate in Stopmode. It can be used either as a watchdog to reset the device when a problem occurs, or as a free running timer for application timeout management. It is hardware or software configurable through the option bytes. The counter can be frozen in debug mode.

3.17.4 System window watchdog (WWDG)

The system window watchdog is based on a 7-bit downcounter that can be set as free running. It can be used as a watchdog to reset the device when a problem occurs. It is clocked from the APB1 clock (PCLK1) derived from the main clock. It has an early warning interrupt capability and the counter can be frozen in debug mode.

3.17.5 SysTick timer

This timer is dedicated to real-time operating systems, but could also be used as a standard down counter. It features:

- A 24-bit down counter
- Autoreload capability
- Maskable system interrupt generation when the counter reaches 0.
- Programmable clock source

3.18 Real-time clock (RTC) and backup registers

The RTC and the backup registers are supplied through V_{DD} supply pin. The backup registers are thirty two 32-bit registers used to store 128 bytes of user application data when V_{DD} power is not present.

They are not reset by a system or power reset.

The RTC is an independent BCD timer/counter. Its main features are the following:

- Calendar with subsecond, seconds, minutes, hours (12 or 24 format), week day, date, month, year, in BCD (binary-coded decimal) format.
- Automatically correction for 28, 29 (leap year), 30, and 31 day of the month.
- 2 programmable alarms with wake up from Stop mode capability.
- Periodic wakeup unit with programmable resolution and period.
- On-the-fly correction from 1 to 32767 RTC clock pulses. This can be used to synchronize it with a master clock.
- Digital calibration circuit with 1 ppm resolution, to compensate for quartz crystal inaccuracy.
- 3 anti-tamper detection pins with programmable filter. The MCU can be woken up from Stop mode on tamper event detection.
- Timestamp feature which can be used to save the calendar content. This function can triggered by an event on the timestamp pin, or by a tamper event. The MCU can be woken up from Stop mode on timestamp event detection.

The RTC clock sources can be:

- A 32.768 kHz external crystal
- A resonator or oscillator
- The internal low-power RC oscillator (typical frequency of 40 kHz)
- The high-speed external clock divided by 32

3.19 I²C bus

Up to two I2C bus interfaces can operate in multimaster and slave modes. They can support standard (up to 100 kHz), fast (up to 400 kHz) and fast mode + (up to 1 MHz) modes with 20 mA output drive. They support 7-bit and 10-bit addressing modes, multiple 7-bit slave addresses (2 addresses, 1 with configurable mask). They also include programmable analog and digital noise filters.

Table 8. Comparison of I2C analog and digital filters

	Analog filter	Digital filter
Pulse width of suppressed spikes	≥ 50 ns	Programmable length from 1 to 15 I2C peripheral clocks
Benefits	Available in Stop mode	1. Extra filtering capability vs. standard requirements. 2. Stable length
Drawbacks	Variations depending on temperature, voltage, process	Disabled when Wakeup from Stop mode is enabled

In addition, they provide hardware support for SMBUS 2.0 and PMBUS 1.1: ARP capability, Host notify protocol, hardware CRC (PEC) generation/verification, timeout verifications and ALERT protocol management. They also have a clock domain independent from the CPU clock, allowing the application to wake up the MCU from Stop mode on address match.

The I2C interfaces can be served by the DMA controller

Refer to *Table 9* for the differences between I2C1 and I2C2.

Table 9. STM32F38x I²C implementation

I2C features(1)	I2C1	I2C2
7-bit addressing mode	X	X
10-bit addressing mode	X	X
Standard mode (up to 100 kbit/s)	X	X
Fast mode (up to 400 kbit/s)	X	X
Fast Mode Plus with 20mA output drive I/Os (up to 1 Mbit/s)	X	
Independent clock	X	
SMBus	X	
Wakeup from STOP	X	

1. X = supported.

3.20 Universal synchronous/asynchronous receiver transmitter (USART)

The STM32F38x embeds three universal synchronous/asynchronous receiver transmitters (USART1, USART2 and USART3).

All USARTs interfaces are able to communicate at speeds of up to 9 Mbit/s.

They provide hardware management of the CTS and RTS signals, they support IrDA SIR ENDEC, the multiprocessor communication mode, the single-wire half-duplex communication mode, Smart Card mode (ISO 7816 compliant), autobaudrate feature and have LIN Master/Slave capability. The USART interfaces can be served by the DMA controller.

Refer to *Table 10* for the features of USART1, USART2 and USART3.

Table 10. STM32F38x USART implementation

USART modes/features(1)	USART1	USART2	USART3
Hardware flow control for modem	X	X	X
Continuous communication using DMA	X	X	X
Multiprocessor communication	X	X	X
Synchronous mode	X	X	X
Smartcard mode	X	X	X
Single-wire half-duplex communication	X	X	X
IrDA SIR ENDEC block	X	X	X
LIN mode	X	X	X
Dual clock domain and wakeup from Stop mode	X	X	X
Receiver timeout interrupt	X	X	X
Modbus communication	X	X	X
Auto baud rate detection	X	X	X
Driver Enable	X	X	X

1. X = supported.

3.21 Serial peripheral interface (SPI)/Inter-integrated sound interfaces (I^2S)

Up to three SPIs are able to communicate at up to 18 Mbits/s in slave and master modes in full-duplex and simplex communication modes. The 3-bit prescaler gives 8 master mode frequencies and the frame is configurable to 8 bits or 16 bits. The hardware CRC generation/verification supports basic SD Card/MMC modes.

The SPIs can be served by the DMA controller.

Three standard I^2S interfaces (multiplexed with SPI1, SPI2 and SPI3) are available, that can be operated in master or slave mode. These interfaces can be configured to operate with 16/32 bit resolution, as input or output channels. Audio sampling frequencies from 8 kHz up to 192 kHz are supported. When either or both of the I^2S interfaces is/are configured in

master mode, the master clock can be output to the external DAC/CODEC at 256 times the sampling frequency.

Refer to *Table 11* for the features between SPI1 and SPI2.

Table 11. STM32F38x SPI/I2S implementation

SPI features[1]	SPI1	SPI2	SPI3
Hardware CRC calculation	X	X	X
Rx/Tx FIFO	X	X	X
NSS pulse mode	X	X	X
I2S mode	X	X	X
TI mode	X	X	X

1. X = supported.

3.22 High-definition multimedia interface (HDMI) - consumer electronics control (CEC)

The device embeds a HDMI-CEC controller that provides hardware support for the Consumer Electronics Control (CEC) protocol (Supplement 1 to the HDMI standard).

This protocol provides high-level control functions between all audiovisual products in an environment. It is specified to operate at low speeds with minimum processing and memory overhead. It has a clock domain independent from the CPU clock, allowing the HDMI_CEC controller to wakeup the MCU from Stop mode on data reception.

3.23 Controller area network (CAN)

The CAN is compliant with specifications 2.0A and B (active) with a bit rate up to 1 Mbit/s. It can receive and transmit standard frames with 11-bit identifiers as well as extended frames with 29-bit identifiers. It has three transmit mailboxes, two receive FIFOs with 3 stages and 14 scalable filter banks.

3.24 Serial wire JTAG debug port (SWJ-DP)

The ARM SWJ-DP Interface is embedded, and is a combined JTAG and serial wire debug port that enables either a serial wire debug or a JTAG probe to be connected to the target.

The JTAG TMS and TCK pins are shared respectively with SWDIO and SWCLK and a specific sequence on the TMS pin is used to switch between JTAG-DP and SW-DP.

3.25 Embedded trace macrocell™

The ARM embedded trace macrocell provides a greater visibility of the instruction and data flow inside the CPU core by streaming compressed data at a very high rate from the STM32F38x through a small number of ETM pins to an external hardware trace port analyzer (TPA) device. The TPA is connected to a host computer using USB, Ethernet, or any other high-speed channel. Real-time instruction and data flow activity can be recorded

and then formatted for display on the host computer running debugger software. TPA hardware is commercially available from common development tool vendors. It operates with third party debugger software tools.

4 Pinouts and pin description

Figure 2. STM32F38x LQFP48 pinout

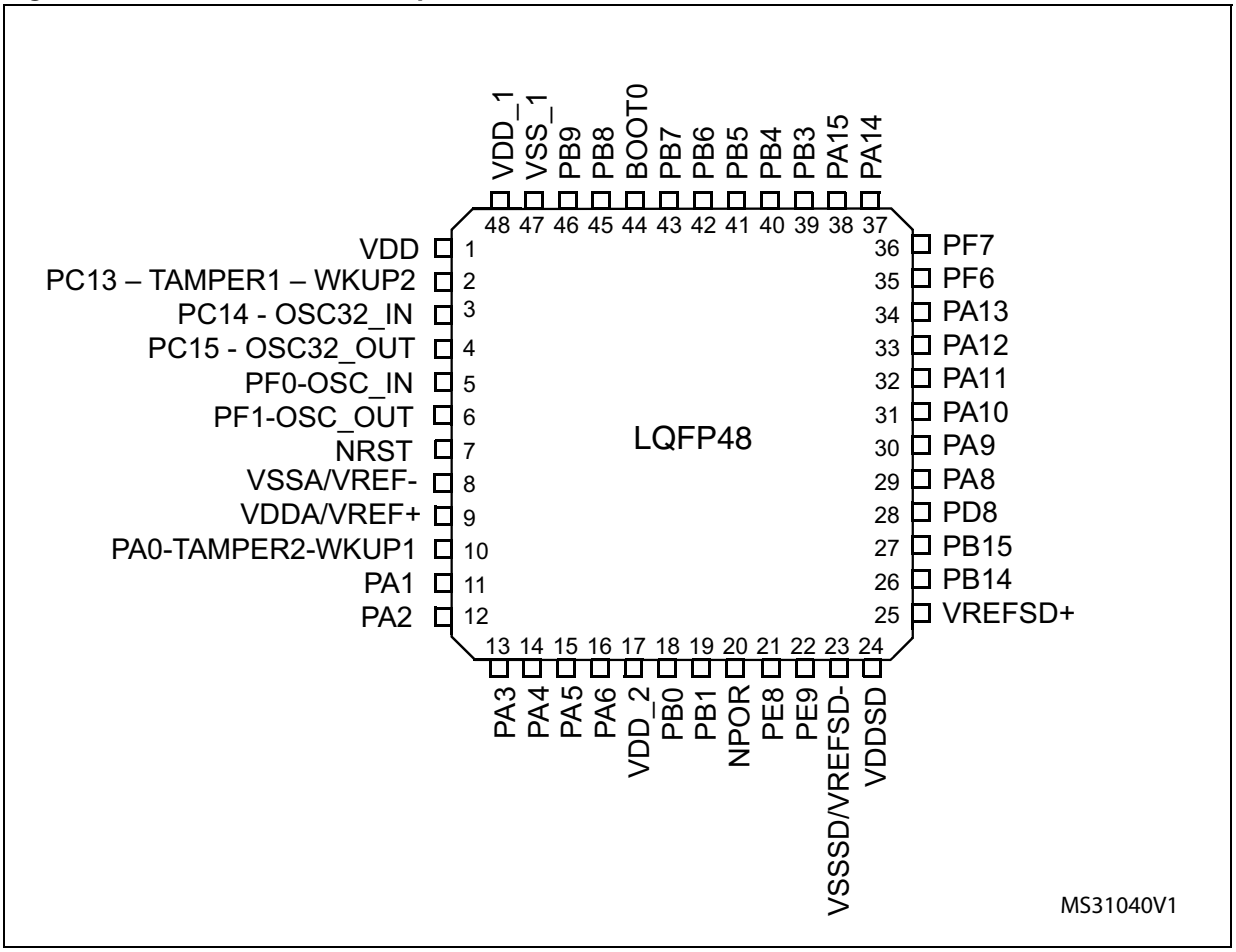


Figure 3. STM32F38x LQFP64 pinout

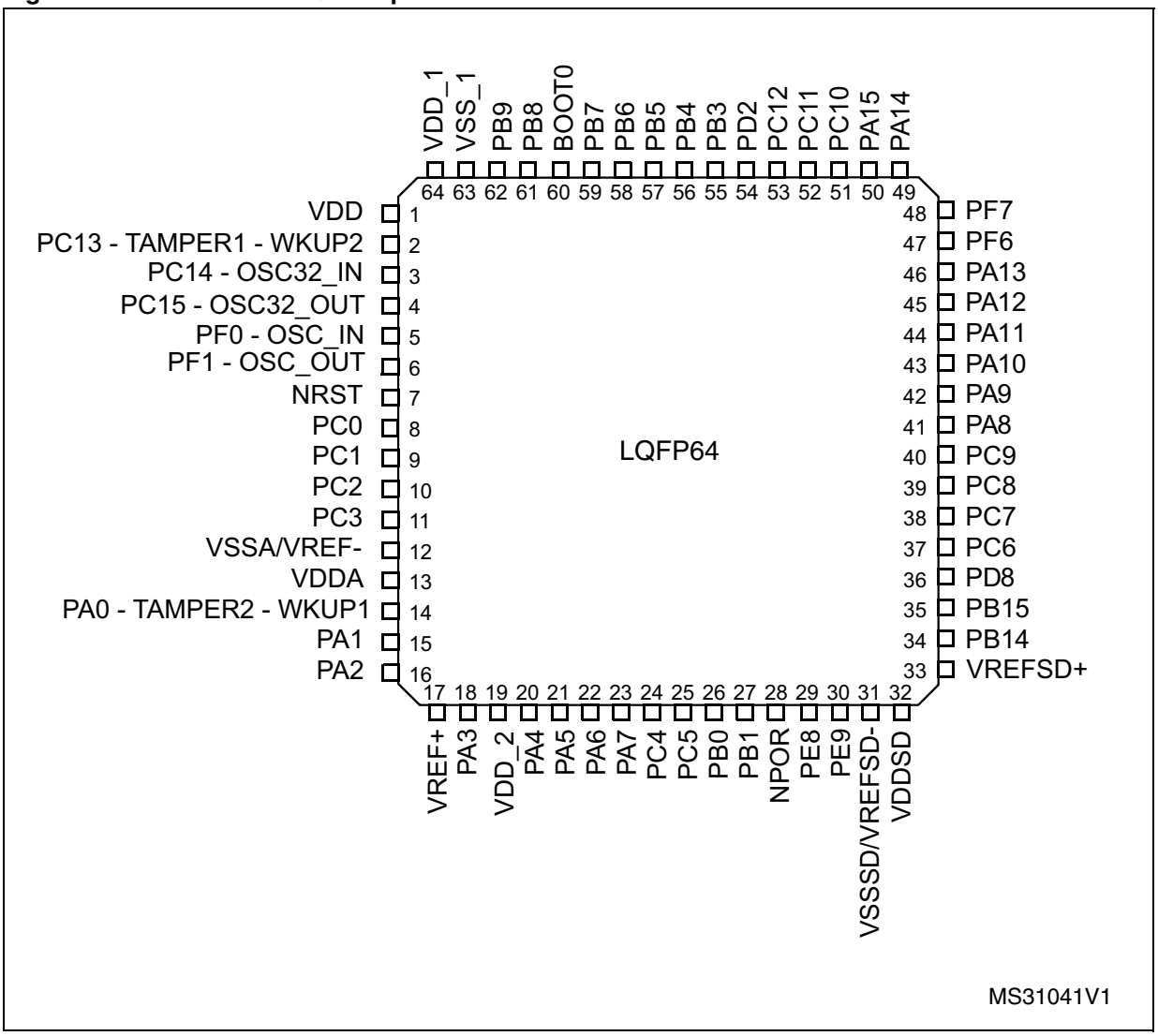


Figure 4. STM32F38x LQFP100 pinout

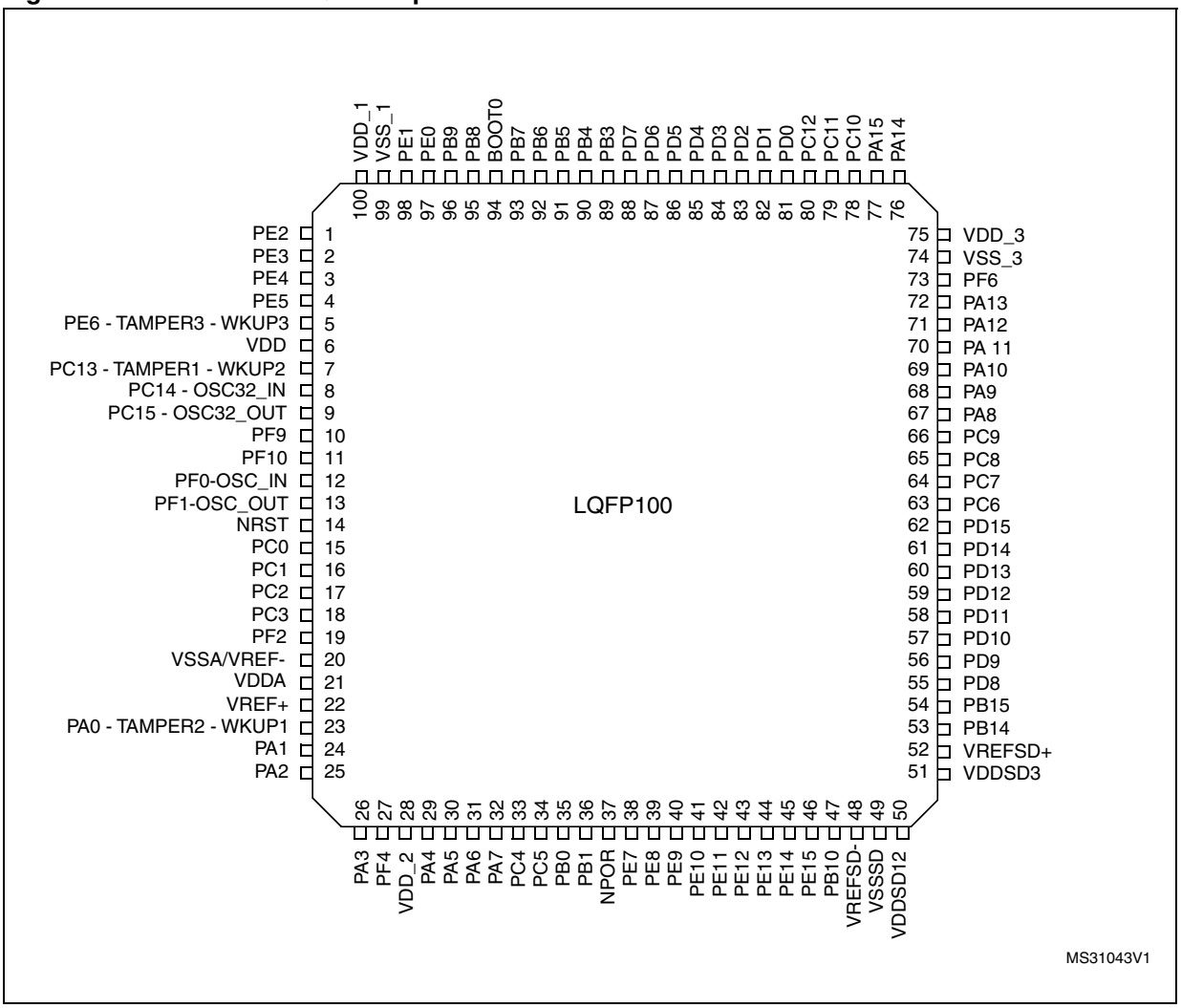


Figure 5. STM32F38x BGA100 pinout

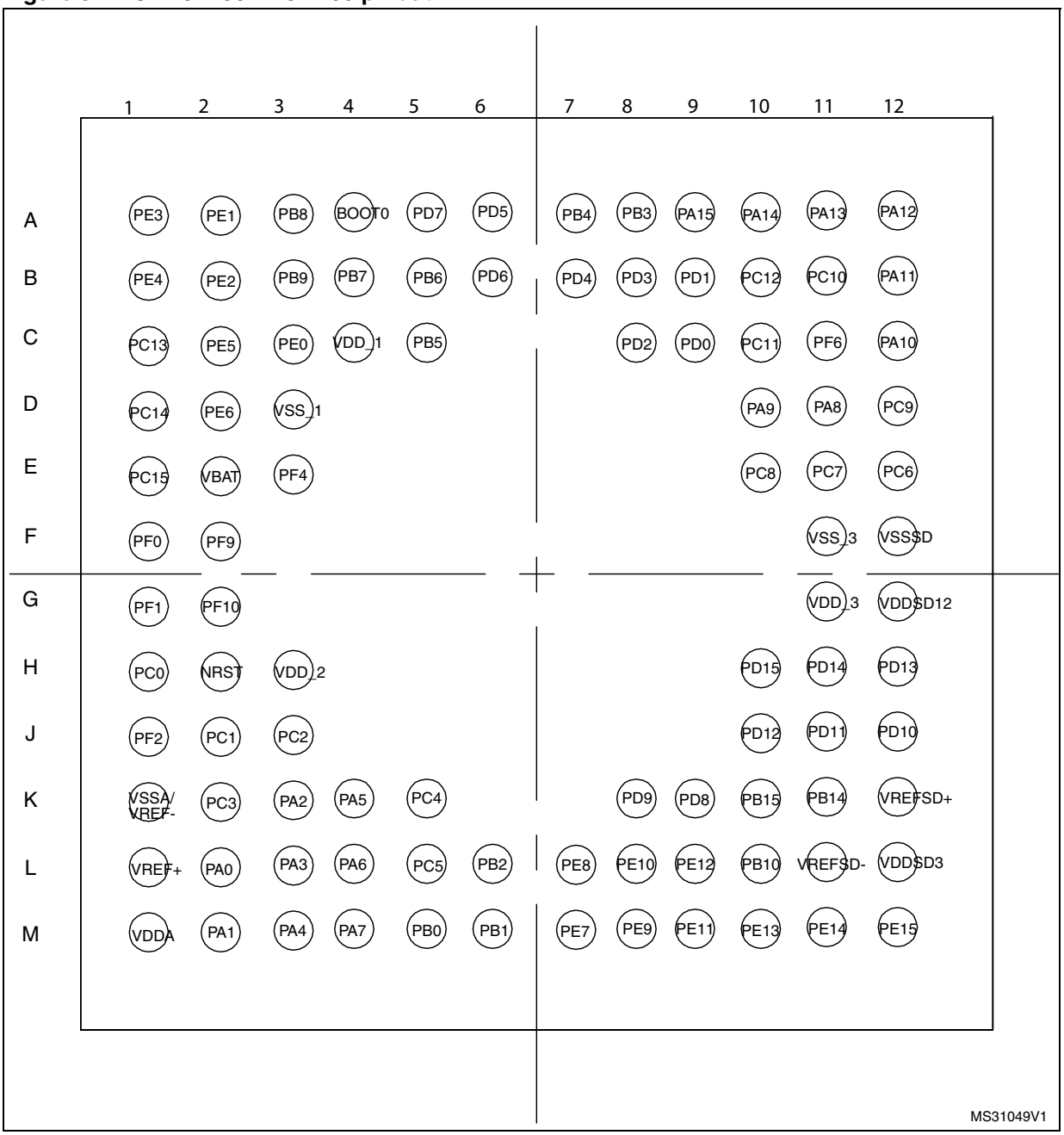


Figure 6. STM32F38x WLCSP66 pinout

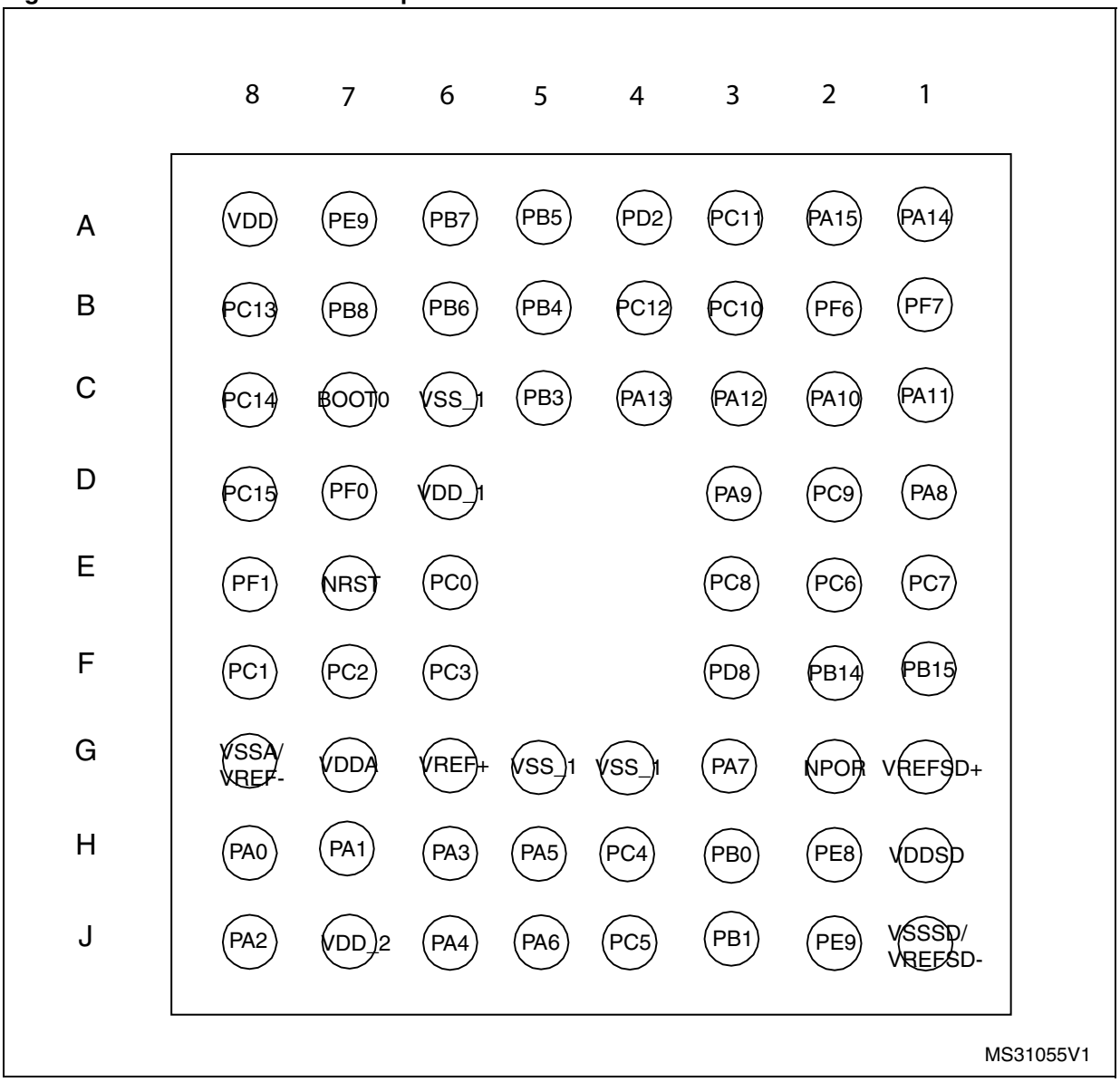


Table 12. Legend/abbreviations used in the pinout table

Name		Abbreviation	Definition
Pin name		Unless otherwise specified in brackets below the pin name, the pin function during and after reset is the same as the actual pin name	
Pin type		S	Supply pin
		I	Input only pin
		I/O	Input / output pin
I/O structure		FT	5 V tolerant I/O
		FTf	5 V tolerant I/O, FM+ capable
		TTa	3.3 V tolerant I/O directly connected to ADC or SDADC
		TC	Standard 3.3V I/O
		B	Dedicated BOOT0 pin
		RST	Bidirectional reset pin with embedded weak pull-up resistor
Notes		Unless otherwise specified by a note, all I/Os are set as floating inputs during and after reset	
Pin functions	Alternate functions	Functions selected through GPIOx_AFR registers	
	Additional functions	Functions directly selected/enabled through peripheral registers	

Table 13. STM32F38x pin definitions

Pin numbers					Pin name (function after reset)	Pin type	Notes	I/O structure	Pin functions	
LQFP100	BGA100	LQFP64	LQFP48	WLCSP66					Alternate function	Additional functions
1	B2				PE2	I/O	(1)	FT	TSC_G7_IO1, TRACECLK	
2	A1				PE3	I/O	(1)	FT	TSC-G7_IO2, TRACED0	
3	B1				PE4	I/O	(1)	FT	TSC_G7_IO3, TRACED1	
4	C2				PE5	I/O	(1)	FT	TSC_G7_IO4, TRACED2	
5	D2				PE6 - TAMPER3 - WKUP3	I/O	(1)	TTa	TRACED3	WKUP3, RTC_TAMPER3
6	E2	1	1	A8	VDD	S				
7	C1	2	2	B8	PC13 - TAMPER1 - WKUP2	I/O		TC		WKUP2_ALARM_OUT_ CALIB_OUT_TIMESTA MP, RTC_TAMPER1
8	D1	3	3	C8	PC14 - OSC32_IN	I/O		TC		OSC32_IN
9	E1	4	4	D8	PC15 - OSC32_O UT	I/O		TC		OSC32_OUT
10	F2				PF9	I/O	(1)	FT	TIM14_CH1	
11	G2				PF10	I/O	(1)	FT		
12	F1	5	5	D7	PF0 - OSC_IN	I/O		FTf	I2C2_SDA	OSC_IN
13	G1	6	6	E8	PF1 - OSC_OUT	I/O		FTf	I2C2_SCL	OSC_OUT
14	H2	7	7	E7	NRST	I/O		RST		
15	H1	8		E6	PC0	I/O	(1)	TTa	TIM5_CH1_ETR	ADC_IN10
16	J2	9		F8	PC1	I/O	(1)	TTa	TIM5_CH2	ADCIN11
17	J3	10		F7	PC2	I/O	(1)	TTa	SPI2_MISO/I2S2_MCK, TIM5_CH3	ADC_IN12
18	K2	11		F6	PC3	I/O	(1)	TTa	SPI2_MOSI/I2S2_SD, TIM5_CH4	ADC_IN13
19	J1				PF2	I/O	(1)	FT	I2C2_SMBAI	
20	K1	12	8	G8	VSSA/ VREF-	S				
			9		VDDA/ VREF+	S	(1)			
21	M1	13		G7	VDDA	S	(1)			
22	L1	17		G6	VREF+	S	(1)			

Table 13. STM32F38x pin definitions (continued)

Pin numbers					Pin name (function after reset)	Pin type	Notes	I/O structure	Pin functions	
LQFP100	BGA100	LQFP64	LQFP48	WLCSP66					Alternate function	Additional functions
23	L2	14	10	H8	PA0 - TAMPER2 - WKUP1	I/O		TTa	USART2_CTS, TIM2_CH1_ETR, TIM5_CH1_ETR, TIM19_CH1, TSC_G1_IO1, COMP1_OUT	RTC_ TAMPER2, WKUP1, ADC_IN0, COMP1_INn
24	M2	15	11	H7	PA1	I/O		TTa	SPI3_SCK/I2S3_CK, USART2_RTS, TIM2_CH2, TIM15_CH1N, TIM5_CH2, TIM19_CH2, TSC_G1_IO2,	ADC_IN1, COMP1_INp, RTC_REF_CLK_IN
25	K3	16	12	J8	PA2	I/O		TTa	COMP2_OUT, TSC_G1_IO3, SPI3_MISO/I2S3_MCK, USART2_TX, TIM2_CH3, TIM15_CH1, TIM5_CH3, TIM19_CH3	ADC_IN2, COMP2_INn
26	L3	18	13	H6	PA3	I/O		TTa	SPI3_MOSI, I2S3_SD, USART2_RX, TIM2_CH4, TIM15_CH2, TIM5_CH4, TIM19_CH4, TSC_G1_IO4	ADC_IN3, COMP2_Inp
27	E3				PF4	I/O	(1)	FT		
28	H3	19	17	J7	VDD_2	S				
29	M3	20	14	J6	PA4	I/O		TTa	SPI1_NSS/I2S1_WS, SPI3_NSS/I2S3_WS, USART2_CK, TIM3_CH2, TIM12_CH1, TSC_G2_IO1, COMP1_OUT	ADC_IN4, DAC1_OUT1
30	K4	21	15	H5	PA5	I/O		TTa	SPI1_SCK/I2S1_CK, CEC, TIM2_CH1_ETR, TIM14_CH1, TIM12_CH2, TSC_G2_IO2	ADC_IN5, DAC1_OUT2
31	L4	22	16	J5	PA6	I/O		TTa	SPI1_MISO/I2S1_MCK, TIM3_CH1, TIM13_CH1, TIM16_CH1, COMP1_OUT, TSC_G2_IO3	ADC_IN6, DAC2_OUT1
32	M4	23		G3	PA7	I/O	(1)	TTa	SPI1_MOSI/I2S1_SD, TIM14_CH1, TIM17_CH1, TIM3_CH2, COMP2_OUT, TSC_G2_IO4	ADC_IN7
33	K5	24		H4	PC4	I/O	(1)	TTa	TIM1_TX, TIM13_CH1, TSC_G3_IO1	ADC_IN14
34	L5	25		J4	PC5	I/O	(1)	TTa	TIM1_RX, TSC_G3_IO2	ADC_IN15
35	M5	26	18	H3	PB0	I/O		TTa	SPI1_MOSI/I2S1_SD, TIM3_CH3, TSC_G3_IO3	ADC_IN8, SDADC1_ADC_IN6P

Table 13. STM32F38x pin definitions (continued)

Pin numbers					Pin name (function after reset)	Pin type	Notes	I/O structure	Pin functions	
LQFP100	BGA100	LQFP64	LQFP48	WLCSP66					Alternate function	Additional functions
36	M6	27	19	J3	PB1	I/O		TTa	TIM3_CH4, TSC_G3_IO4	ADC_IN9, SDADC1_5P, SDADC1_AIN6M
37	L6	28	20	G2	NPOR			TC	power-on reset	
38	M7				PE7	I/O	(1)(2)	TC		SDADC1_AIN3P, SDADC1_AIN4M, SDADC2_AIN5P, SDADC2_AIN6M
39	L7	29	21	H2	PE8	I/O	(2)	TC		SDADC1_AIN8P, SDADC2_AIN8P
40	M8	30	22	J2	PE9	I/O	(2)	TC		SDADC1_AIN7P, SDADC1_AIN8M, SDADC2_AIN7P, SDADC2_AIN8M
41	L8				PE10	I/O	(2) (1)	TC		SDADC1_AIN2P
42	M9				PE11	I/O	(1)(2)	TC		SDADC1_AIN1P, SDADC1_AIN2M, SDADC2_AIN4P
43	L9				PE12	I/O	(1)(2)	TC		SDADC1_AIN0P, SDADC2_AIN3P, SDADC2_AIN4M
44	M10				PE13	I/O	(1)(2)	TC		SDADC1_AIN0M, SDADC2_AIN2P
45	M11				PE14	I/O	(1)(2)	TC		SDADC2_AIN1P, SDADC2_AIN2M
46	M12				PE15	I/O	(1)(2)	TC	USART3_RX	SDADC2_AIN0P
47	L10				PB10	I/O	(1)(2)	TC	SPI2_SCK/I2S2_CK, CEC, USART3_TX, TSC_SYNC	TIM2_CH3, SDADC2_AIN0M
48	L11				VREFSD-	S	(1)			
49	F12				VSSSD	S	(1)			
		31	23	J1	VSSSD/ VREFSD-	S				
50	G12				VDDSD12	S	(1)			
		32	24	H1	VDDSD	S				
51	L12				VDDSD3	S	(1)			
52	K12	33	25	G1	VREFSD+	S				
53	K11	34	26	F2	PB14	I/O	(3)	TC	SPI2_MISO/I2S2_MCK, USART3_RTS, TIM15_CH1, TIM12_CH1, TSC_G6_IO1	SDADC3_AIN8P

Table 13. STM32F38x pin definitions (continued)

Pin numbers					Pin name (function after reset)	Pin type	Notes	I/O structure	Pin functions	
LQFP100	BGA100	LQFP64	LQFP48	WLCSP66					Alternate function	Additional functions
54	K10	35	27	F1	PB15	I/O	(3)	TC	SPI2_MOSI/I2S2_SD, TIM15_CH1N, TIM15_CH2, TIM12_CH2, TSC_G6_IO2	SDADC3_7P, SDADC3_AIN8M, RTC_REFCLKIN
55	K9	36	28	F3	PD8	I/O	(3)	TC	SPI2_SCK/I2S2_CK, USART3_TX, TSC_G6_IO3	SDADC3_AIN6P
56	K8				PD9	I/O	(3) (1)	TC	USART3_RX, TSC_G6_IO4	SDADC3_AIN5P, SDADC3_AIN6M
57	J12				PD10	I/O	(1)(3)	TC	USART3_CK	SDADC3_AIN4P
58	J11				PD11	I/O	(1)(3)	TC	USART3_CTS	SDADC3_AIN3P, SDADC3_AIN4M
59	J10				PD12	I/O	(1)(3)	TC	USART3_RTS	TIM4_CH1,G8_IO1, SDADC3_AIN2P
60	H12				PD13	I/O	(1)(3)	TC	TIM4_CH2, TSC_G8_IO2	SDADC3_AIN1P, SDADC3_AIN2M
61	H11				PD14	I/O	(1)(3)	TC	TIM4_CH3, TSC_G8_IO3	SDADC3_AIN0P
62	H10				PD15	I/O	(1)(3)	TC	TIM4_CH4, TSC_G8_IO4	SDADC3_AIN0M
63	E12	37		E2	PC6	I/O	(1)	FT	SPI1_NSS/I2S1_WS, TIM3_CH1	
64	E11	38		E1	PC7	I/O	(1)	FT	SPI1_SCK/I2S1_CK, TIM3_CH2	
65	E10	39		E3	PC8	I/O	(1)	FT	SPI1_MISO/I2S1_MCK, TIM3_CH3	
66	D12	40		D2	PC9	I/O	(1)	FT	SPI1_MOSI/I2S1_SD, TIM3_CH4	
67	D11	41	29	D1	PA8	I/O		FT	SPI2_SCK/I2S2_CK, I2C2_SMBAI, USART1_CK, TIM4_ETR, TIM5_CH1_ETR, CLK_CLKOUT	
68	D10	42	30	D3	PA9	I/O		FTf	SPI2_MISO/I2S2_MCK, I2C2_SCL, USART1_TX, TIM2_CH3, TIM15_BKIN, TIM13_CH1, TSC_G4_IO1	
69	C12	43	31	C2	PA10	I/O		FTf	SPI2_MOSI/I2S2_SD, I2C2_SDA, USART1_RX, TIM2_CH4, TIM17_BKIN, TIM14_CH1, TSC_G4_IO2	

Table 13. STM32F38x pin definitions (continued)

Pin numbers					Pin name (function after reset)	Pin type	Notes	I/O structure	Pin functions	
LQFP100	BGA100	LQFP64	LQFP48	WLCSP66					Alternate function	Additional functions
70	B12	44	32	C1	PA11	I/O		FT	SPI2_NSS/I2S2_WS, SPI1_NSS/I2S1_WS, USART1_CTS, CAN_RX, TIM4_CH1, TIM5_CH2, COMP1_OUT	
71	A12	45	33	C3	PA12	I/O		FT	SPI1_SCK/I2S1_CK, USART1_RTS, CAN_TX, TIM16_CH1, TIM4_CH2, TIM5_CH3, COMP2_OUT	
72	A11	46	34	C4	PA13	I/O		FT	SPI1_MISO/I2S1_MCK, USART3_CTS, IR_OUT, TIM16_CH1N, TIM4_CH3, TIM5_CH4, G4_IO3, SWDAT-JTMS	
73	C11	47	35	B2	PF6	I/O		FTf	SPI1_MOSI, I2S1_SD, USART3_RTS, TIM4_CH4, I2C2_SCL	
74	F11				VSS_3	S	(1)			
75	G11				VDD_3	S	(1)			
		48	36	B1	PF7	I/O		FTf	I2C2_SDA, USART2_CK	
76	A10	49	37	A1	PA14	I/O		FTf	I2C1_SDA, TIM12_CH1, TSC_G4_IO4, SWCLK-JTCK	
77	A9	50	38	A2	PA15	I/O		FTf	SPI1_NSS/I2S1_WS, SPI3_NSS/I2S3_WS, I2C1_SCL, TIM2_CH1_ETR, TIM12_CH2, TSC_SYNC, JTDI	
78	B11	51		B3	PC10	I/O	(1)	FT	SPI3_SCK/I2S3_CK, USART3_TX, TIM19_CH1	
79	C10	52		A3	PC11	I/O	(1)	FT	SPI3_MISO/I2S3_MCK, USART3_RX, TIM19_CH2	
80	B10	53		B4	PC12	I/O	(1)	FT	SPI3_MOSI/I2S3_SD, USART3_CK, TIM19_CH3	
81	C9				PD0	I/O	(1)	FT	CAN_RX, TIM19_CH4	
82	B9				PD1	I/O	(1)	FT	CAN_TX, TIM19_ETR	
83	C8	54		A4	PD2	I/O	(1)	FT	TIM3_ETR	
84	B8				PD3	I/O	(1)	FT	SPI2_MISO/I2S2_MCK, USART2_CTS	
85	B7				PD4	I/O	(1)	FT	SPI2_MOSI/I2S2_SD, USART2_RTS	

Table 13. STM32F38x pin definitions (continued)

Pin numbers					Pin name (function after reset)	Pin type	Notes	I/O structure	Pin functions	
LQFP100	BGA100	LQFP64	LQFP48	WLCSP66					Alternate function	Additional functions
86	A6				PD5	I/O	(1)	FT	USART2_TX	
87	B6				PD6	I/O	(1)	FT	SPI2_NSS/I2S2_WS, USART2_RX	
88	A5				PD7	I/O	(1)	FT	SPI2_SCK/I2S2_CK, USART2_CK	
89	A8	55	39	C5	PB3	I/O		FT	SPI1_SCK/I2S1_CK, SPI3_SCK/I2S3_CK, USART2_TX, TIM2_CH2, TIM3_ETR, TIM4_ETR, TIM13_CH1, TSC_G5_IO1, JTDO-TRACESWO	
90	A7	56	40	B5	PB4	I/O		FT	SPI1_MISO/I2S1_MCK, SPI3_MISO/I2S3_MCK, USART2_RX, TIM16_CH1, TIM3_CH1, TIM17_BKIN, TIM15_CH1N, TSC_G5_IO2, JNTRST	
91	C5	57	41	A5	PB5	I/O		FT	SPI1_MOSI/I2S1_SD, SPI3_MOSI/I2S3_SD, I2C1_SMBAI, USART2_CK, TIM16_BKIN, TIM3_CH2, TIM17_CH1, TIM19_ETR	
92	B5	58	42	B6	PB6	I/O		FTf	I2C1_SCL, USART1_TX, TIM16_CH1N, TIM3_CH3, TIM4_CH1, TIM19_CH1, TIM15_CH1, TSC_G5_IO3	
93	B4	59	43	A6	PB7	I/O		FTf	I2C1_SDA, USART1_RX, TIM17_CH1N, TIM3_CH4, TIM4_CH2, TIM19_CH2, TIM15_CH2, TSC_G5_IO4	
94	A4	60	44	C7	BOOT0	I		B	Boot memory selection	
95	A3	61	45	B7	PB8	I/O		FTf	SPI2_SCK/I2S2_CK, I2C1_SCL, USART3_TX, CAN_RX, CEC, TIM16_CH1, TIM4_CH3, TIM19_CH3, COMP1_OUT, TSC_SYNC	
96	B3	62	46	A7	PB9	I/O		FTf	SPI2_NSS/I2S2_WS, I2C1_SDA, USART3_RX, CAN_TX, IR_OUT, TIM17_CH1, TIM4_CH4, TIM19_CH4, COMP2_OUT	
97	C3				PE0	I/O	(1)	FT	USART1_TX, TIM4_ETR	

Table 13. STM32F38x pin definitions (continued)

Pin numbers					Pin name (function after reset)	Pin type	Notes	I/O structure	Pin functions	
LQFP100	BGA100	LQFP64	LQFP48	WLCSP66					Alternate function	Additional functions
98	A2				PE1	I/O	(1)	FT	USART1_RX	
99	D3	63	47	C6	VSS_1	S			Ground	
				G5	VSS_1	S	(1)		Ground	
				G4	VSS_1	S	(1)		Ground	
100	C4	64	48	D6	VDD_1	S			Digital power supply	

1. When using the small packages (48 and 64 pin packages), the GPIO pins which are not present on these packages, must not be configured in analog mode.
2. these pins are powered by VDDSD12
3. these pins are powered by VDDSD3

Table 14. Alternate functions for port PA

Pin Name	AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF14	AF15
PA0		TIM2_CH1_ETR	TIM5_CH1_ETR	TSC_G1_IO1				USART2_CTS	COMP1_OUT			TIM19_CH1		EVENTOUT
PA1		TIM2_CH2	TIM5_CH2	TSC_G1_IO2			SPI3_SCK / I2S3_CK	USART2_RTS		TIM15_CH1N		TIM19_CH2		EVENTOUT
PA2		TIM2_CH3	TIM5_CH3	TSC_G1_IO3			SPI3_MISO/ I2S3_MCK	USART2_TX	COMP2_OUT	TIM15_CH1		TIM19_CH3		EVENTOUT
PA3		TIM2_CH4	TIM5_CH4	TSC_G1_IO4			SPI3_MOSI / I2S3_SD	USART2_RX		TIM15_CH2		TIM19_CH4		EVENTOUT
PA4			TIM3_CH2	TSC_G2_IO1		SPI1_NSS / I2S1_WS	SPI3_NSS / I2S3_WS	USART2_CK			TIM12_CH1			EVENTOUT
PA5		TIM2_CH1_ETR		TSC_G2_IO2		SPI1_SCK / I2S1_CK		CEC		TIM14_CH1	TIM12_CH2			EVENTOUT
PA6		TIM16_CH1	TIM3_CH1	TSC_G2_IO3		SPI1_MISO / I2S1_MCK			COMP1_OUT	TIM13_CH1				EVENTOUT
PA7		TIM17_CH1	TIM3_CH2	TSC_G2_IO4		SPI1_MOSI / I2S1_SD			COMP2_OUT	TIM14_CH1				EVENTOUT
PA8	MCO		TIM5_CH1_ETR		I2C2_SMBAI	SPI2_SCK / I2S2_CK		USART1_CK			TIM4_ETR			EVENTOUT
PA9			TIM13_CH1	TSC_G4_IO1	I2C2_SCL	SPI2_MISO / I2S2_MCK		USART1_TX		TIM15_BKIN	TIM2_CH3			EVENTOUT
PA10		TIM17_BKIN		TSC_G4_IO2	I2C2_SDA	SPI2_MOSI / I2S2_SD		USART1_RX		TIM14_CH1	TIM2_CH4			EVENTOUT
PA11			TIM5_CH2			SPI2_NSS / I2S2_WS	SPI1_NSS / I2S1_WS	USART1_CTS	COMP1_OUT	CAN_RX	TIM4_CH1			EVENTOUT
PA12		TIM16_CH1	TIM5_CH3				SPI1_SCK / I2S1_CK	USART1_RTS	COMP2_OUT	CAN_TX	TIM4_CH2			EVENTOUT

Table 14. Alternate functions for port PA (continued)

Pin Name	AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF14	AF15
PA13	JTMS-SWDAT	TIM16_CH1N	TIM5_CH4	TSC_G4_IO3		IR-Out	SPI1_MISO / I2S1_MCK	USART3_CTS			TIM4_CH3			EVENTOUT
PA14	JTCK-SWCLK			TSC_G4_IO4	I2C1_SDA						TIM12_CH1			EVENTOUT
PA15	JTDI	TIM2_CH1_ETR		TSC_SYNC	I2C1_SCL	SPI1_NSS / I2S1_WS	SPI3_NSS / I2S3_WS				TIM12_CH2			EVENTOUT

Table 15. Alternate functions for port PB

Pin Name	AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF15
PB0			TIM3_CH3	TSC_ G3_IO3		SPI_MOSI / I2S1_SD					TIM3_ CH2		EVENTOUT
PB1			TIM3_CH4	TSC_ G3_IO4									EVENTOUT
PB3	JTDO/ TRACESWO	TIM2_ CH2	TIM4_ETR	TSC_ G5_IO1		SPI1_SCK / I2S1_CK	SPI3_SCK/ I2S3_CK	USART2_TX		TIM13_ CH1	TIM3_ ETR		EVENTOUT
PB4	JTRST	TIM16_ CH1	TIM3_CH1	TSC_ G5_IO2		SPI1_MISO / I2S1_MCK	SPI3_MISO/ I2S3_MCK	USART2_RX		TIM15_ CH1N	TIM17 _BKIN		EVENTOUT
PB5		TIM16_ BKIN	TIM3_CH2		I2C1_ SMBAI	SPI1_MOSI / I2S1_SD	SPI3_MOSI / I2S3_SD	USART2_CK			TIM17 _CH1	TIM19 _ETR	EVENTOUT
PB6		TIM16_ CH1N	TIM4_CH1	TSC_ G5_IO3	I2C1_ SCL			USART1_TX		TIM15_ CH1	TIM3_ CH3	TIM19 _CH1	EVENTOUT
PB7		TIM17_ CH1N	TIM4_CH2	TSC_ G5_IO4	I2C1_ SDA			USART1_RX		TIM15_ CH2	TIM3_ CH4	TIM19 _CH2	EVENTOUT
PB8		TIM16_ CH1	TIM4_CH3	TSC_ SYNC	I2C1_ SCL	SPI2_SCK / I2S2_CK	CEC	USART3_TX	COMP1 _OUT	CAN_ RX		TIM19 _CH3	EVENTOUT
PB9		TIM17_ CH1	TIM4_CH4		I2C1_ SDA	SPI2_NSS / I2S2_WS	IR-Out	USART3_RX	COMP2 _OUT	CAN_ TX		TIM19 _CH4	EVENTOUT
PB10		TIM2_ CH3		TSC_ SYNCH		SPI2_SCK / I2S2_CK	CEC	USART3_TX					EVENTOUT
PB14		TIM15_ CH1		TSC_ G6_IO1		SPI2_MISO / I2S2_MCK		USART3_RTS		TIM12_ CH1			EVENTOUT
PB15		TIM15_ CH2	TIM15_ CH1N	TSC_ G6_IO2		SPI2_MOSI / I2S2_SD				TIM12_ CH2			EVENTOUT

Table 16. Alternate functions for port PC

Pin Name	AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7
PC0		EVENTOUT	TIM5_CH1_ETR					
PC1		EVENTOUT	TIM5_CH2					
PC2		EVENTOUT	TIM5_CH3			SPI2_MISO / I2S2_MCK		
PC3		EVENTOUT	TIM5_CH4			SPI2_MOSI / I2S2_SD		
PC4		EVENTOUT	TIM13_CH1	TSC_G3_IO1				USART1_TX
PC5		EVENTOUT		TSC_G3_IO2				USART1_RX
PC6		EVENTOUT	TIM3_CH1			SPI1_NSS / I2S1_WS		
PC7		EVENTOUT	TIM3_CH2			SPI1_SCK / I2S1_CK		
PC8		EVENTOUT	TIM3_CH3			SPI1_MISO/I2S1_MCK		
PC9		EVENTOUT	TIM3_CH4			SPI1_MOSI / I2S1_SD		
PC10		EVENTOUT	TIM19_CH1				SPI3_SCK / I2S3_CK	USART3_TX
PC11		EVENTOUT	TIM19_CH2				SPI3_MISO /I2S3_MCK	USART3_RX
PC12		EVENTOUT	TIM19_CH3				SPI3_MOSI / I2S3_SD	USART3_CK
PC13								
PC14								
PC15								

Table 17. Alternate functions for port PD

Pin Name	AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7
PD0		EVENTOUT	TIM19_CH4					CAN_RX
PD1		EVENTOUT	TIM19_ETR					CAN_TX
PD2		EVENTOUT	TIM3_ETR					
PD3		EVENTOUT				SPI2_MISO / I2S2_MCK		USART2_CTS
PD4		EVENTOUT				SPI2_MOSI / I2S2_SD		USART2_RTS
PD5		EVENTOUT						USART2_TX
PD6		EVENTOUT				SPI2_NSS / I2S2_WS		USART2_RX
PD7		EVENTOUT				SPI2_SCK / I2S2_CK		USART2_CK
PD8		EVENTOUT		TSC_G6_IO3		SPI2_SCK / I2S2_CK		USART3_TX
PD9		EVENTOUT		TSC_G6_IO4				USART3_RX
PD10		EVENTOUT						USART3_CK
PD11		EVENTOUT						USART3_CTS
PD12		EVENTOUT	TIM4_CH1	TSC_G8_IO1				USART3_RTS
PD13		EVENTOUT	TIM4_CH2	TSC_G8_IO2				
PD14		EVENTOUT	TIM4_CH3	TSC_G8_IO3				
PD15		EVENTOUT	TIM4_CH4	TSC_G8_IO4				

Table 18. Alternate functions for port PE

Pin Name	AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7
PE0		EVENTOUT	TIM4_ETR					USART1_TX
PE1		EVENTOUT						USART1_RX
PE2	TRACECLK	EVENTOUT		TSC_G7_IO1				
PE3	TRACED0	EVENTOUT		TSC_G7_IO2				
PE4	TRACED1	EVENTOUT		TSC_G7_IO3				
PE5	TRACED2	EVENTOUT		TSC_G7_IO4				
PE6	TRACED3	EVENTOUT						
PE7		EVENTOUT						
PE8		EVENTOUT						
PE9		EVENTOUT						
PE10		EVENTOUT						
PE11		EVENTOUT						
PE12		EVENTOUT						
PE13		EVENTOUT						
PE14		EVENTOUT						
PE15		EVENTOUT						USART3_RX

Table 19. Alternate functions for port PF

Pin Name	AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7
PF0					I2C2_SDA			
PF1					I2C2_SCL			
PF2		EVENTOUT			I2C2_SMBAI			
PF4		EVENTOUT						
PF6		EVENTOUT	TIM4_CH4		I2C2_SCL	SPI1_MOSI / I2S1_SD		USART3_RTS
PF7		EVENTOUT			I2C2_SDA			USART2_CK
PF9		EVENTOUT	TIM14_CH1					
PF10		EVENTOUT						

5 Memory mapping

Figure 7. STM32F38x memory map

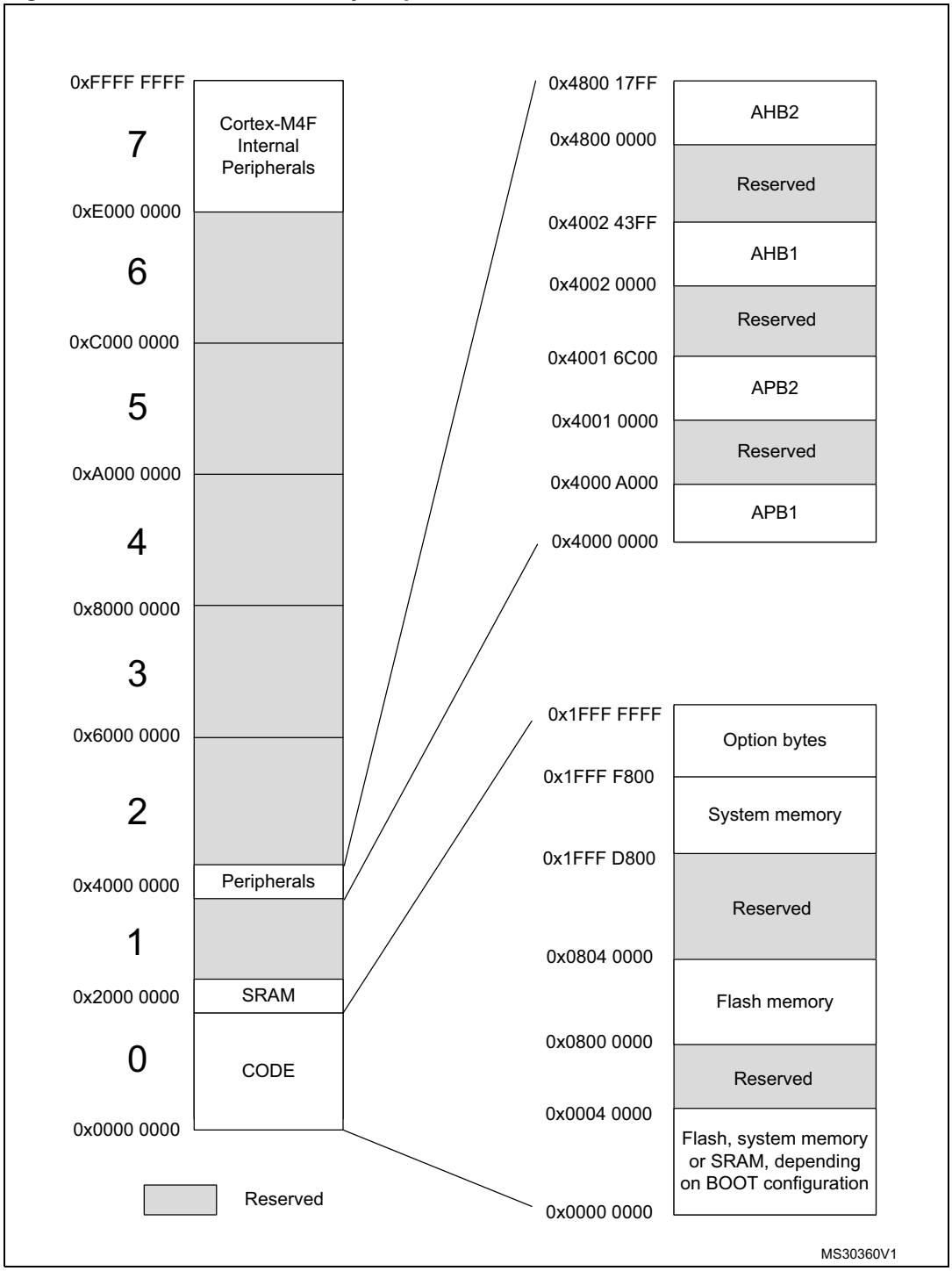


Table 20. STM32F38x peripheral register boundary addresses

Bus	Boundary address	Size	Peripheral
AHB2	0x4800 1400 - 0x4800 17FF	1KB	GPIOF
	0x4800 1000 - 0x4800 13FF	1KB	GPIOE
	0x4800 0C00 - 0x4800 0FFF	1KB	GPIOD
	0x4800 0800 - 0x4800 0BFF	1KB	GPIOC
	0x4800 0400 - 0x4800 07FF	1KB	GPIOB
	0x4800 0000 - 0x4800 03FF	1KB	GPIOA
	0x4002 4400 - 0x47FF FFFF	~128 MB	Reserved
AHB1	0x4002 4000 - 0x4002 43FF	1 KB	TSC
	0x4002 3400 - 0x4002 3FFF	3 KB	Reserved
	0x4002 3000 - 0x4002 33FF	1 KB	CRC
	0x4002 2400 - 0x4002 2FFF	3 KB	Reserved
	0x4002 2000 - 0x4002 23FF	1 KB	FLASH memory interface
	0x4002 1400 - 0x4002 1FFF	3 KB	Reserved
	0x4002 1000 - 0x4002 13FF	1 KB	RCC
	0x4002 0800- 0x4002 0FFF	2 KB	Reserved
	0x4002 0400 - 0x4002 07FF	1 KB	DMA2
	0x4002 0000 - 0x4002 03FF	1 KB	DMA1
	0x4001 6C00 - 0x4001 FFFF	37 KB	Reserved

Table 20. STM32F38x peripheral register boundary addresses (continued)

Bus	Boundary address	Size	Peripheral
APB2	0x4001 6800 - 0x4001 6BFF	1 KB	SDADC3
	0x4001 6400 - 0x4001 67FF	1 KB	SDADC2
	0x4001 6000 - 0x4001 63FF	1 KB	SDADC1
	0x4001 5C00 - 0x4001 5FFF	1 KB	TIM19
	0x4001 4C00 - 0x4001 5BFF	4 KB	Reserved
	0x4001 4800 - 0x4001 4BFF	1 KB	TIM17
	0x4001 4400 - 0x4001 47FF	1 KB	TIM16
	0x4001 4000 - 0x4001 43FF	1 KB	TIM15
	0x4001 3C00 - 0x4001 3FFF	1 KB	Reserved
	0x4001 3800 - 0x4001 3BFF	1 KB	USART1
	0x4001 3400 - 0x4001 37FF	1 KB	Reserved
	0x4001 3000 - 0x4001 33FF	1 KB	SPI1/I2S1
	0x4001 2800 - 0x4001 2FFF	1 KB	Reserved
	0x4001 2400 - 0x4001 27FF	1 KB	ADC
	0x4001 0800 - 0x4001 23FF	7 KB	Reserved
	0x4001 0400 - 0x4001 07FF	1 KB	EXTI
	0x4001 0000 - 0x4001 03FF	1 KB	SYSCFG
	0x4000 4000 - 0x4000 FFFF	24 KB	Reserved
APB1	0x4000 9C00 – 0x4000 9FFF	1 KB	TIM18
	0x4000 9800 - 0x4000 9BFF	1 KB	DAC2
	0x4000 7C00 - 0x4000 97FF	8 KB	Reserved
	0x4000 7800 - 0x4000 7BFF	1 KB	CEC
	0x4000 7400 - 0x4000 77FF	1 KB	DAC1
	0x4000 7000 - 0x4000 73FF	1 KB	PWR
	0x4000 6800 - 0x4000 6FFF	2 KB	Reserved
	0x4000 6400 - 0x4000 67FF	1 KB	CAN
	0x4000 5C00 - 0x4000 63FF	2 KB	Reserved

Table 20. STM32F38x peripheral register boundary addresses (continued)

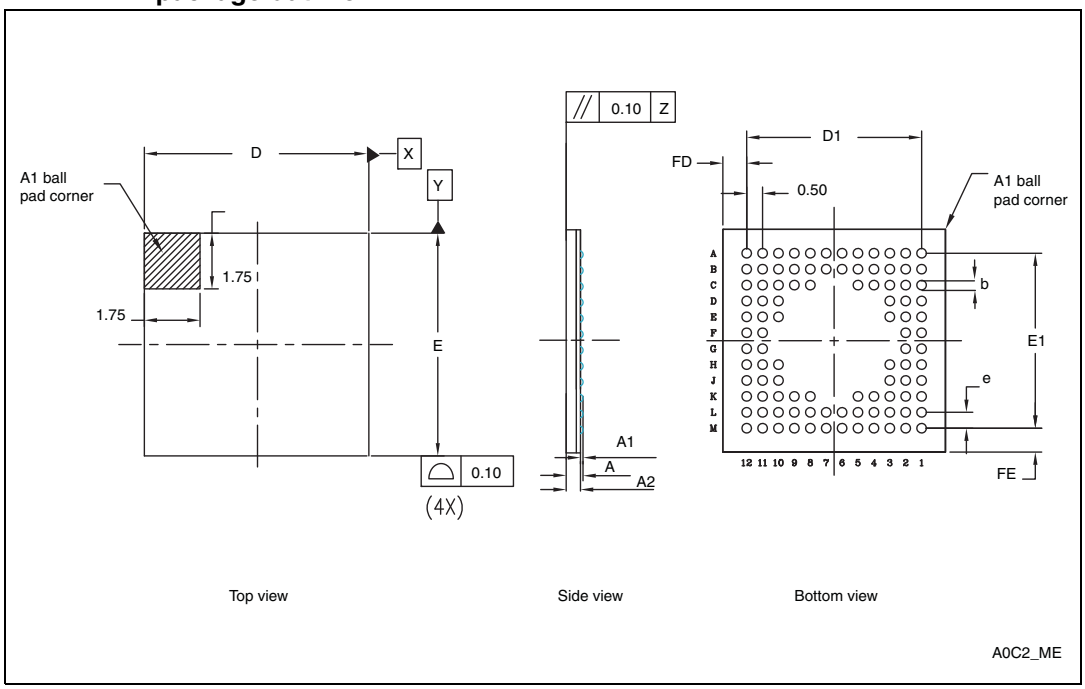
Bus	Boundary address	Size	Peripheral
APB1	0x4000 5800 - 0x4000 5BFF	1 KB	I2C2
	0x4000 5400 - 0x4000 57FF	1 KB	I2C1
	0x4000 4C00 - 0x4000 53FF	2 KB	Reserved
	0x4000 4800 - 0x4000 4BFF	1 KB	USART3
	0x4000 4400 - 0x4000 47FF	1 KB	USART2
	0x4000 4000 - 0x4000 43FF	1 KB	Reserved
	0x4000 3C00 - 0x4000 3FFF	1 KB	SPI3/I2S3
	0x4000 3800 - 0x4000 3BFF	1 KB	SPI2/I2S2
	0x4000 3400 - 0x4000 37FF	1 KB	Reserved
	0x4000 3000 - 0x4000 33FF	1 KB	IWWDG
	0x4000 2C00 - 0x4000 2FFF	1 KB	WWDG
	0x4000 2800 - 0x4000 2BFF	1 KB	RTC
	0x4000 2400 - 0x4000 27FF	1 KB	Reserved
	0x4000 2000 - 0x4000 23FF	1 KB	TIM14
	0x4000 1C00 - 0x4000 1FFF	1 KB	TIM13
	0x4000 1800 - 0x4000 1BFF	1 KB	TIM12
	0x4000 1400 - 0x4000 17FF	1 KB	TIM7
	0x4000 1000 - 0x4000 13FF	1 KB	TIM6
	0x4000 0C00 - 0x4000 0FFF	1 KB	TIM5
	0x4000 0800 - 0x4000 0BFF	1 KB	TIM4
	0x4000 0400 - 0x4000 07FF	1 KB	TIM3
	0x4000 0000 - 0x4000 03FF	1 KB	TIM2

6 Package characteristics

6.1 Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: *www.st.com*. ECOPACK® is an ST trademark.

Figure 8. UFBGA100 – ultra fine pitch ball grid array, 7 x 7 mm, 0.50 mm pitch, package outline



1. Drawing is not to scale.

Table 21. UFBGA100 – ultra fine pitch ball grid array, 7 x 7 mm, 0.50 mm pitch, package mechanical data

Symbol	millimeters			inches[1]		
	Min	Typ	Max	Min	Typ	Max
A	0.46	0.53	0.6	0.0181	0.0209	0.0236
A1	0.06	0.08	0.1	0.0024	0.0031	0.0039
A2	0.4	0.45	0.5	0.0157	0.0177	0.0197
b	0.2	0.25	0.3	0.0079	0.0098	0.0118
D		7			0.2756	
D1		5.5			0.2165	
E		7			0.2756	
E1		5.5			0.2165	
e		0.5			0.0197	
FD		0.75			0.0295	
FE		0.75			0.0295	

1. Values in inches are converted from mm and rounded to 4 decimal digits.

Figure 9. WLCSP66 – 0.400 mm pitch wafer level chip size package outline

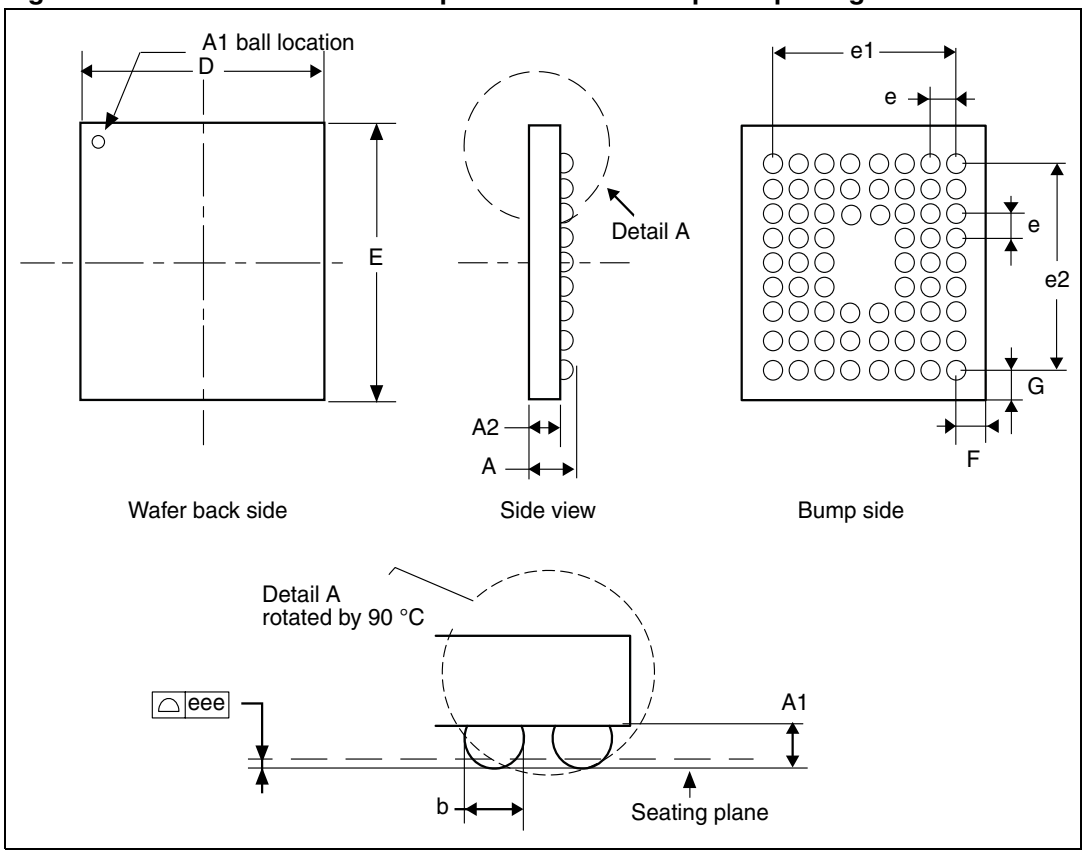
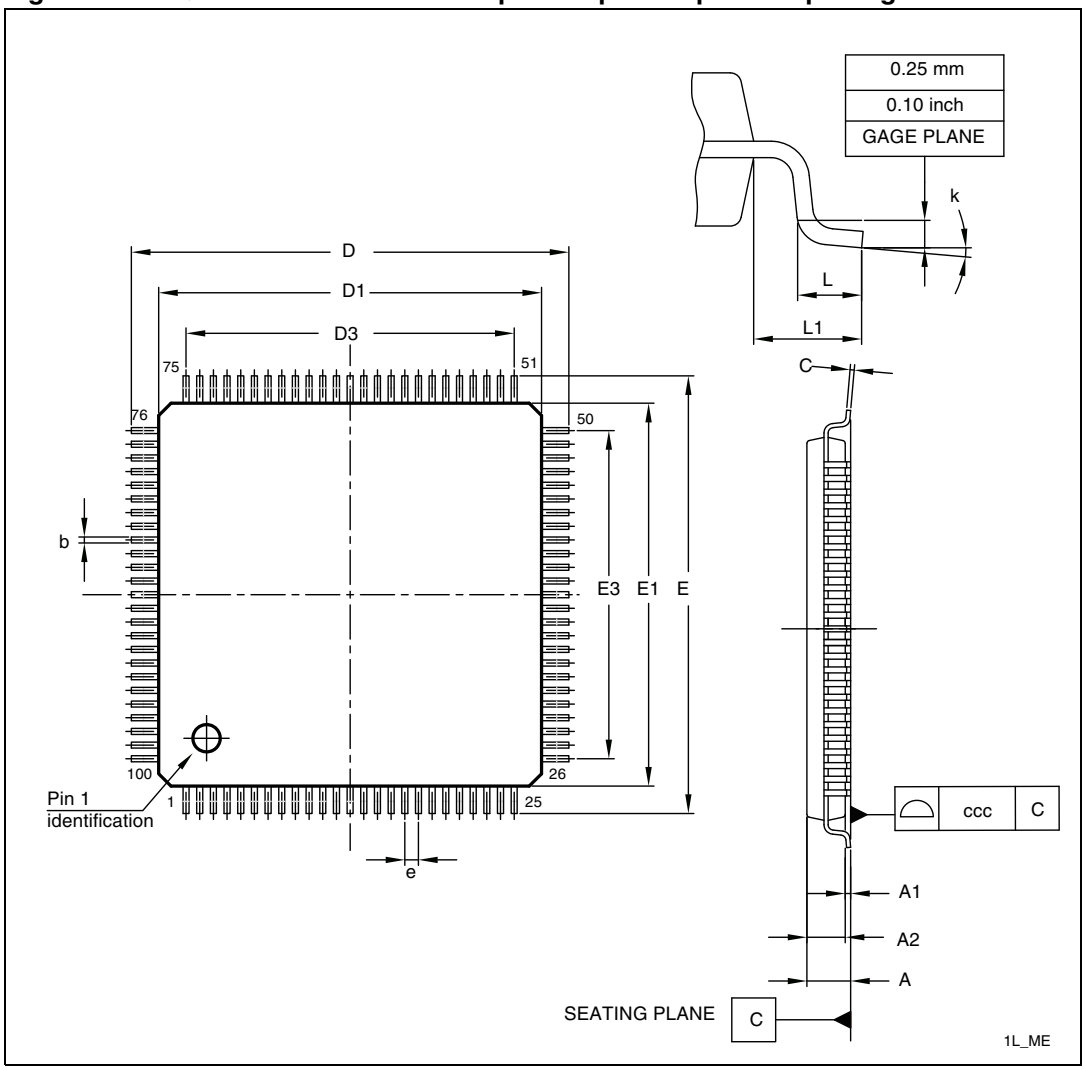


Table 22. WLCSP66 – 0.400 mm pitch wafer level chip size package mechanical data

Symbol	millimeters			inches		
	Min	Typ	Max	Min	Typ	Max
A	0.520	0.570	0.600	0.0205	0.0224	0.0236
A1	0.170	0.190	0.210	0.0067	0.0075	0.0083
A2	0.350	0.380	0.410	0.0138	0.0150	0.0161
b	0.245	0.270	0.295	0.0096	0.0106	0.0116
D	3.747	3.767	3.787	0.1475	0.1483	0.1491
E	4.209	4.229	4.249	0.1657	0.1665	0.1673
e		0.400			0.0157	
e1		2.800			0.1102	
e2		3.200			0.1260	
F		0.484			0.0191	
G		0.515			0.0203	
eee			0.050			0.0020

Figure 10. LQFP100 –14 x 14 mm 100-pin low-profile quad flat package outline



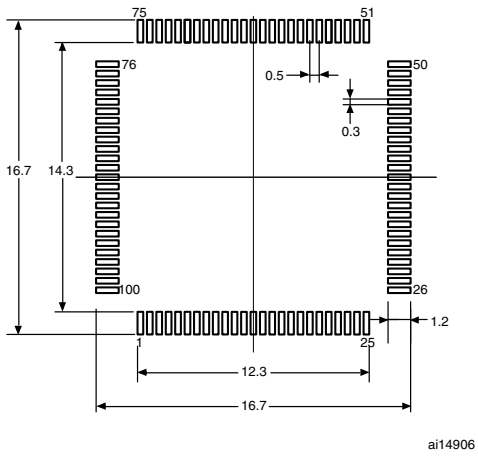
1. Drawing is not to scale.

Table 23. LQPF100 – 14 x 14 mm 100-pin low-profile quad flat package mechanical data

Symbol	millimeters			inches[1]		
	Min	Typ	Max	Min	Typ	Max
A			1.60			0.063
A1	0.05		0.15	0.002		0.0059
A2	1.35	1.40	1.45	0.0531	0.0551	0.0571
b	0.17	0.22	0.27	0.0067	0.0087	0.0106
c	0.09		0.20	0.0035		0.0079
D	15.80	16.00	16.20	0.622	0.6299	0.6378
D1	13.80	14.00	14.20	0.5433	0.5512	0.5591
D3		12.00			0.4724	
E	15.80	16.00	16.20	0.622	0.6299	0.6378
E1	13.80	14.00	14.20	0.5433	0.5512	0.5591
E3		12.00			0.4724	
e		0.50			0.0197	
L	0.45	0.60	0.75	0.0177	0.0236	0.0295
L1		1.00			0.0394	
k	0°	3.5°	7°	0°	3.5°	7°
ccc		0.08			0.0031	

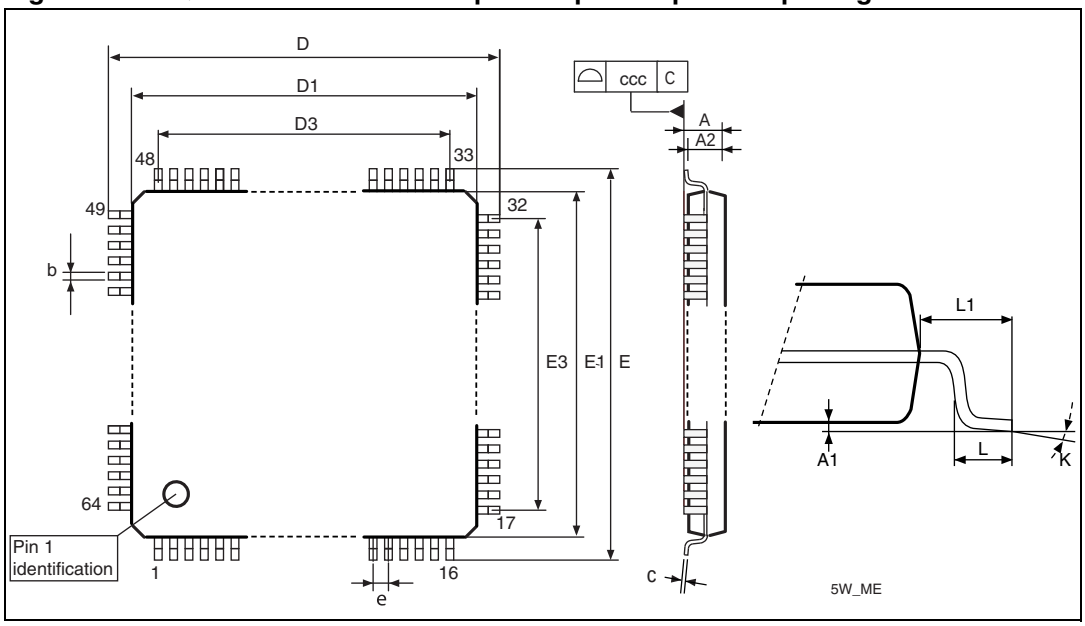
1. Values in inches are converted from mm and rounded to 4 decimal digits.

Figure 11. Recommended footprint



1. Dimensions are in millimeters.

Figure 12. LQFP64 – 10 x 10 mm 64 pin low-profile quad flat package outline



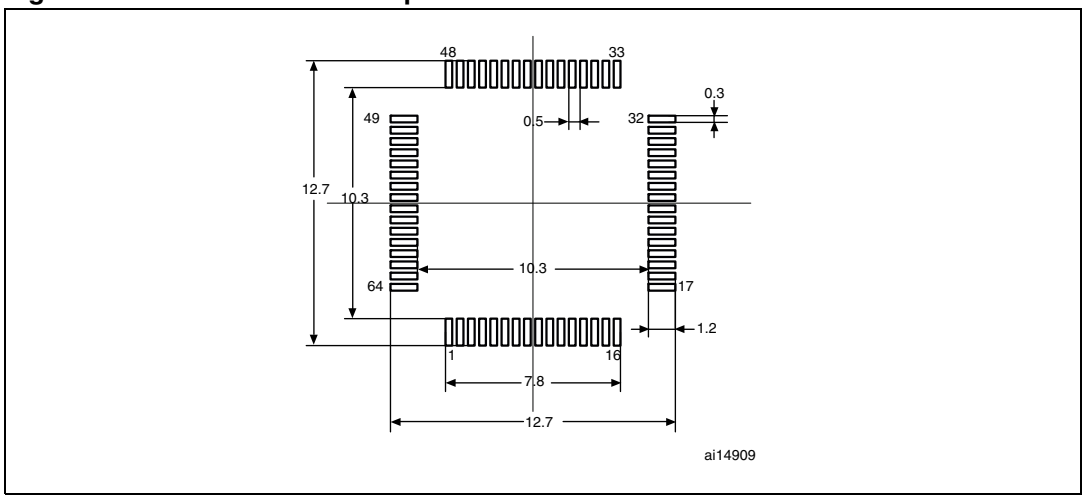
1. Drawing is not to scale.

Table 24. LQFP64 – 10 x 10 mm 64 pin low-profile quad flat package mechanical data

Symbol	millimeters			inches[1]		
	Min	Typ	Max	Min	Typ	Max
A			1.600			0.0630
A1	0.050		0.150	0.0020		0.0059
A2	1.350	1.400	1.450	0.0531	0.0551	0.0571
b	0.170	0.220	0.270	0.0067	0.0087	0.0106
c	0.090		0.200	0.0035		0.0079
D	11.800	12.000	12.200	0.4646	0.4724	0.4803
D1	9.800	10.000	10.200	0.3858	0.3937	0.4016
D.		7.500				
E	11.800	12.000	12.200	0.4646	0.4724	0.4803
E1	9.800	10.00	10.200	0.3858	0.3937	0.4016
e		0.500			0.0197	
k	0°	3.5°	7°	0°	3.5°	7°
L	0.450	0.600	0.75	0.0177	0.0236	0.0295
L1		1.000			0.0394	
ccc	0.080			0.0031		
N	Number of pins					
	64					

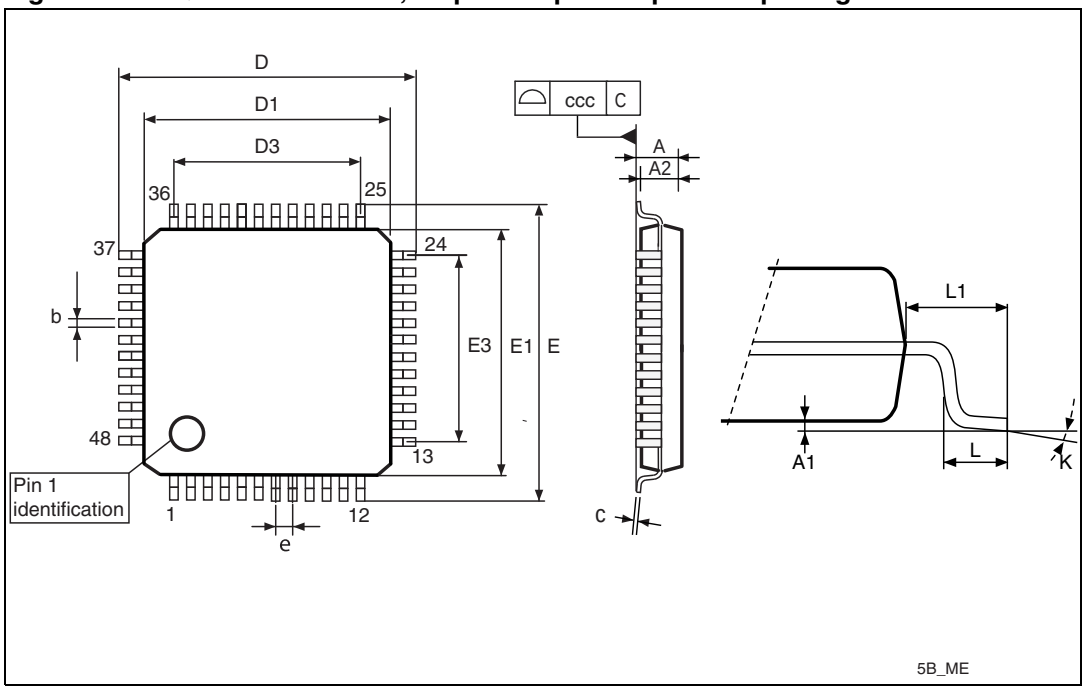
1. Values in inches are converted from mm and rounded to 4 decimal digits.

Figure 13. Recommended footprint



1. Dimensions are in millimeters.

Figure 14. LQFP48 – 7 x 7 mm, 48-pin low-profile quad flat package outline



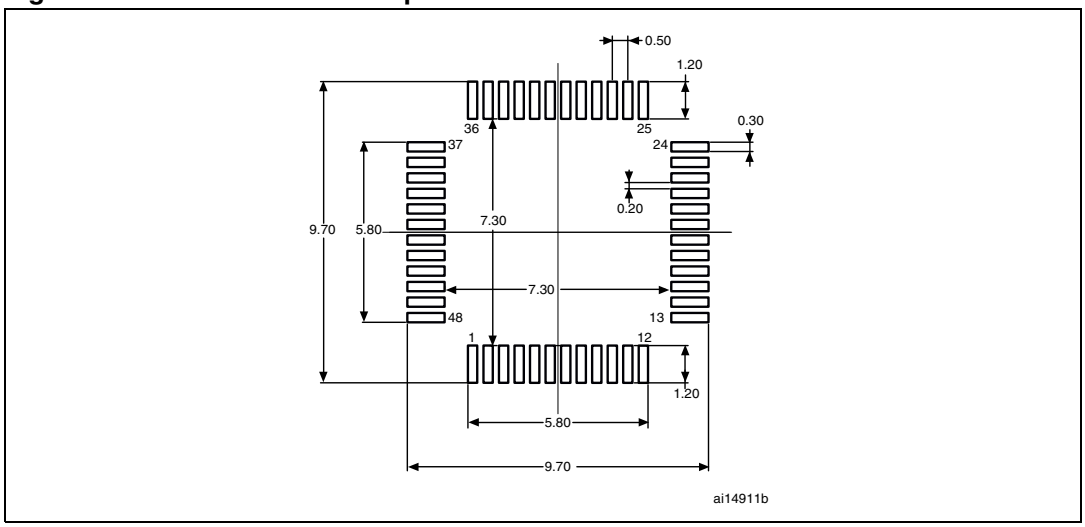
1. Drawing is not to scale.

Table 25. LQFP48 – 7 x 7 mm, 48-pin low-profile quad flat package mechanical data

Symbol	millimeters			inches[1]		
	Min	Typ	Max	Min	Typ	Max
A			1.600			0.0630
A1	0.050		0.150	0.0020		0.0059
A2	1.350	1.400	1.450	0.0531	0.0551	0.0571
b	0.170	0.220	0.270	0.0067	0.0087	0.0106
c	0.090		0.200	0.0035		0.0079
D	8.800	9.000	9.200	0.3465	0.3543	0.3622
D1	6.800	7.000	7.200	0.2677	0.2756	0.2835
D3		5.500			0.2165	
E	8.800	9.000	9.200	0.3465	0.3543	0.3622
E1	6.800	7.000	7.200	0.2677	0.2756	0.2835
E3		5.500			0.2165	
e		0.500			0.0197	
L	0.450	0.600	0.750	0.0177	0.0236	0.0295
L1		1.000			0.0394	
k	0°	3.5°	7°	0°	3.5°	7°
ccc		0.080			0.0031	

1. Values in inches are converted from mm and rounded to 4 decimal digits.

Figure 15. Recommended footprint



1. Dimensions are in millimeters.

6.2 Thermal characteristics

The maximum chip junction temperature ($T_J$max) must never exceed the values given in *Table 24: General operating conditions on page 54*.

The maximum chip-junction temperature, T_J max, in degrees Celsius, may be calculated using the following equation:

$$T_J \text{ max} = T_A \text{ max} + (P_D \text{ max x } \Theta_{JA})$$

Where:

- T_A max is the maximum ambient temperature in °C,
- Θ_{JA} is the package junction-to-ambient thermal resistance, in °C/W,
- P_D max is the sum of P_{INT} max and $P_{I/O}$ max (P_D max = P_{INT} max + $P_{I/O}$max),
- P_{INT} max is the product of I_{DD} and V_{DD}, expressed in Watts. This is the maximum chip internal power.

$P_{I/O}$ max represents the maximum power dissipation on output pins where:

$$P_{I/O} \text{ max} = \Sigma (V_{OL} \times I_{OL}) + \Sigma((V_{DD} - V_{OH}) \times I_{OH}),$$

taking into account the actual V_{OL} / I_{OL} and V_{OH} / I_{OH} of the I/Os at low and high level in the application.

Table 26. Package thermal characteristics

Symbol	Parameter	Value	Unit
Θ_{JA}	**Thermal resistance junction-ambient** LQFP64 - 10 × 10 mm / 0.5 mm pitch	45	°C/W
	Thermal resistance junction-ambient LQFP48 - 7 × 7 mm	55	
	Thermal resistance junction-ambient LQFP100 - 14 × 14 mm / 0.5 mm pitch	46	
	Thermal resistance junction-ambient BGA100 - 7 x 7 mm	59	
	Thermal resistance junction-ambient WLCSP66 - 0.400 mm	53	

6.2.1 Reference document

JESD51-2 Integrated Circuits Thermal Test Method Environment Conditions - Natural Convection (Still Air). Available from www.jedec.org

6.2.2 Selecting the product temperature range

When ordering the microcontroller, the temperature range is specified in the ordering information scheme shown in *Section 7: Part numbering*.

Each temperature range suffix corresponds to a specific guaranteed ambient temperature at maximum dissipation and, to a specific maximum junction temperature.

As applications do not commonly use the STM32F38x at maximum dissipation, it is useful to calculate the exact power consumption and junction temperature to determine which temperature range will be best suited to the application.

The following examples show how to calculate the temperature range needed for a given application.

Example 1: High-performance application

Assuming the following application conditions:

Maximum ambient temperature T_{Amax} = 82 °C (measured according to JESD51-2), I_{DDmax} = 50 mA, V_{DD} = 1.8 V, maximum 3 I/Os used at the same time in output at low level with I_{OL} = 8 mA, V_{OL}= 0.4 V and maximum 2 I/Os used at the same time in output at low level with I_{OL} = 20 mA, V_{OL}= 1.3 V

P_{INTmax} = 50 mA × 1.8 V= 90 mW

P_{IOmax} = 3 × 8 mA × 0.4 V + 2 × 20 mA × 1.3 V = 61.6 mW

This gives: P_{INTmax} = 90 mW and P_{IOmax} = 61.6 mW:

P_{Dmax} = 90 + 61.6 = 151.6 mW

Thus: P_{Dmax} = 151.6 mW

Using the values obtained in *Table 26* T_{Jmax} is calculated as follows:

– For LQFP64, 45°C/W

T_{Jmax} = 82 °C + (45°C/W × 151.6 mW) = 82 °C + 6.8 °C = 88.8 °C

This is within the range of the suffix 6 version parts (–40 < T_J < 105 °C).

In this case, parts must be ordered at least with the temperature range suffix 6 (see *Section 7: Part numbering*).

Example 2: High-temperature application

Using the same rules, it is possible to address applications that run at high ambient temperatures with a low dissipation, as long as junction temperature T_J remains within the specified range.

Assuming the following application conditions:

Maximum ambient temperature T_{Amax} = 115 °C (measured according to JESD51-2), I_{DDmax} = 20 mA, V_{DD} = 1.8 V, maximum 9 I/Os used at the same time in output at low level with I_{OL} = 8 mA, V_{OL}= 0.4 V

P_{INTmax} = 20 mA × 1.8 V= 36 mW

P_{IOmax} = 9 × 8 mA × 0.4 V = 28.8 mW

This gives: P_{INTmax} = 36 mW and P_{IOmax} = 28.8 mW:

P_{Dmax} = 36+ 28.8 = 64.8 mW

Thus: P_{Dmax} = 64.8 mW

Using the values obtained in *Table 26* T_{Jmax} is calculated as follows:

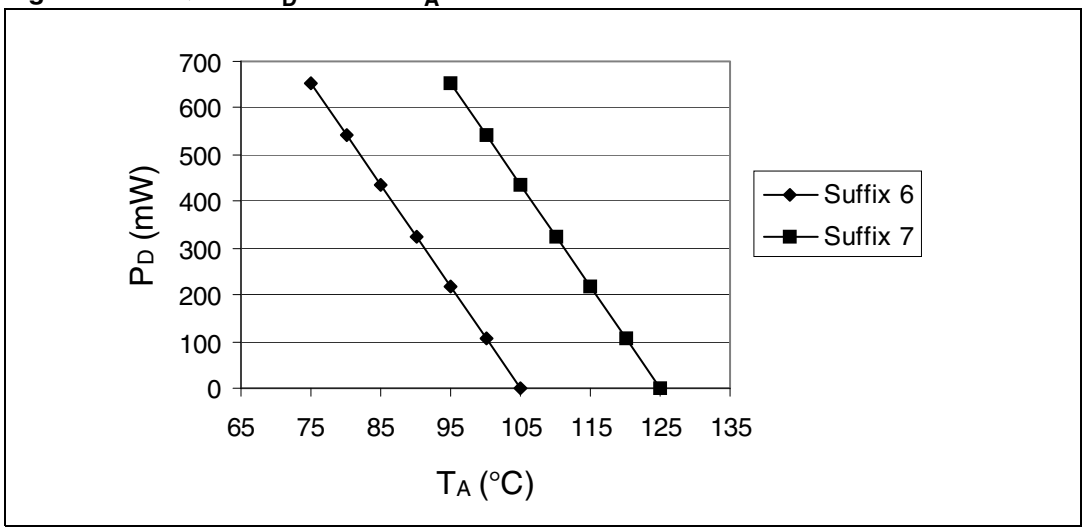
– For LQFP100, 46°C/W

T_{Jmax} = 115 °C + (46°C/W × 64.8 mW) = 115 °C + 2.98 °C = 118 °C

This is within the range of the suffix 7 version parts (–40 < T_J < 125 °C).

In this case, parts must be ordered at least with the temperature range suffix 7 (see *Section 7: Part numbering*).

Figure 16. LQFP64 P_D max vs. T_A



7 Part numbering

For a list of available options (memory, package, and so on) or for further information on any aspect of this device, please contact your nearest ST sales office.

Table 27. Ordering information scheme

Example: STM32 F 372 R 8 T 6 x

Device family

STM32 = ARM-based 32-bit microcontroller

Product type

F = General-purpose

Sub-family

383 = STM32F383xx

Pin count

C = 48 pins
R = 64/66 pins
V = 100 pins

Code size

8 = 64 Kbytes of Flash memory
B = 128 Kbytes of Flash memory
C = 256 Kbytes of Flash memory

Package

T = LQFP
H = BGA
Y = WLCSP

Temperature range

6 = Industrial temperature range, –40 to 85 °C
7 = Industrial temperature range, –40 to 105 °C

Options

xxx = programmed parts
TR = tape and real

8 Revision history

Table 28. Document revision history

Date	Revision	Changes
07-Sep-2012	1	Initial release.

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