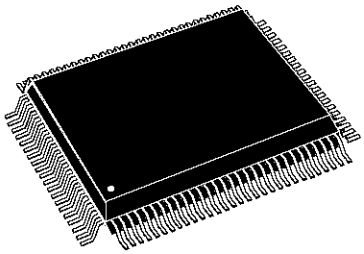
SGS-THOMSON MICROELECTRONICS

ST10F166

16-BIT MCU WITH 256K FLASH MEMORY

- High Performance 16-bit CPU with 4-Stage Pipeline
- 100 ns Instruction Cycle Time at 20 MHz CPU Clock
- 500 ns Multiplication (16 × 16 bit), 1 µs Division (32 / 16 bit)
- Enhanced Boolean Bit Manipulation Facilities
- Register-Based Design with Multiple Variable Register Banks
- Single-Cycle Context Switching Support
- Up to 256 KBytes Linear Address Space for Code and Data
- 1 KByte On-Chip RAM
- **32 KBytes On-Chip Flash EPROM with Bank Erase Feature**
- Protection-Optional Flash Memory
- Dedicated Flash Control Register with Operation Lock Mechanism
- 12 V External Flash Programming Voltage
- Flash Program Verify and Erase Verify Modes
- 1000 Flash Program/Erase Cycles guaranteed
- Programmable External Bus Characteristics for Different Address Ranges
- 8-Bit or 16-Bit External Data Bus
- Multiplexed or Demultiplexed External Address/ Data Buses
- Hold and Hold-Acknowledge Bus Arbitration Support
- 512 Bytes On-Chip Special Function Register Area
- Idle and Power Down Modes
- 8-Channel Interrupt-Driven Single-Cycle Data Transfer Facilities via Peripheral Event Controller (PEC)



PQFP100

- 16-Priority-Level Interrupt System
- 10-Channel 10-bit A/D Converter with 9.7 µs Conversion Time (ST10F166)
- 16-Channel Capture/Compare Unit
- Two Multi-Functional General Purpose Timer Units with 5 Timers
- Two Serial Channels (USARTs)
- Programmable Watchdog Timer
- Up to 76 General Purpose I/O Lines
- Supported by a Wealth of Development Tools like C-Compilers, Macro-Assembler Packages, Emulators, Evaluation Boards, HLL-Debuggers, Simulators, Logic Analyzer Disassemblers, Programming Boards
- On-Chip Bootstrap Loader
- 100-Pin Plastic PQFP Package

Table of Contents

1 INTRODUCTION

The ST10F166 is the FLASH memory members of the ST10 family of microcontrollers developed and produced by SGS-THOMSON Microelectronics in CMOS technology. they combine high CPU performance (up to 10 million instructions per second) with high peripheral functionality, enhanced IO-capabilities and an on-chip reprogrammable 32 KByte Flash Memory.

The ST10F166-16 derives its CPU clock signal (operating clock) directly from the on-chip oscillator without using a prescaler.

With a clock duty cycle of 0.4 to 0.6, the recommended clock frequency is 16MHz for the ST10F166.

The ST10F166 operates at half the oscillator clock frequency (using a 2:1 oscillator prescaler).

Figure 1. Logic Symbol

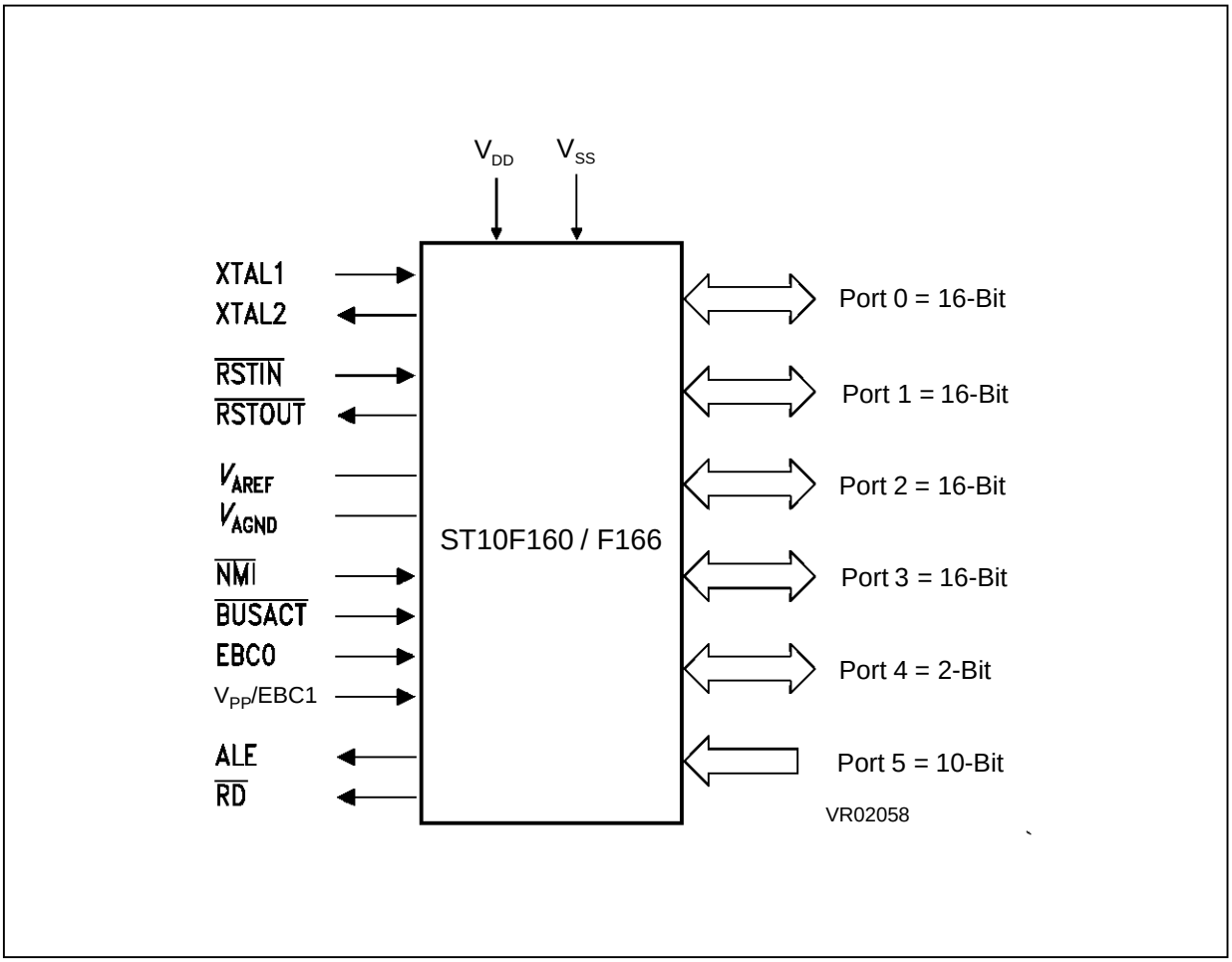


Figure 2. Pin Configuration Rectangular PQFP-100 (top view)

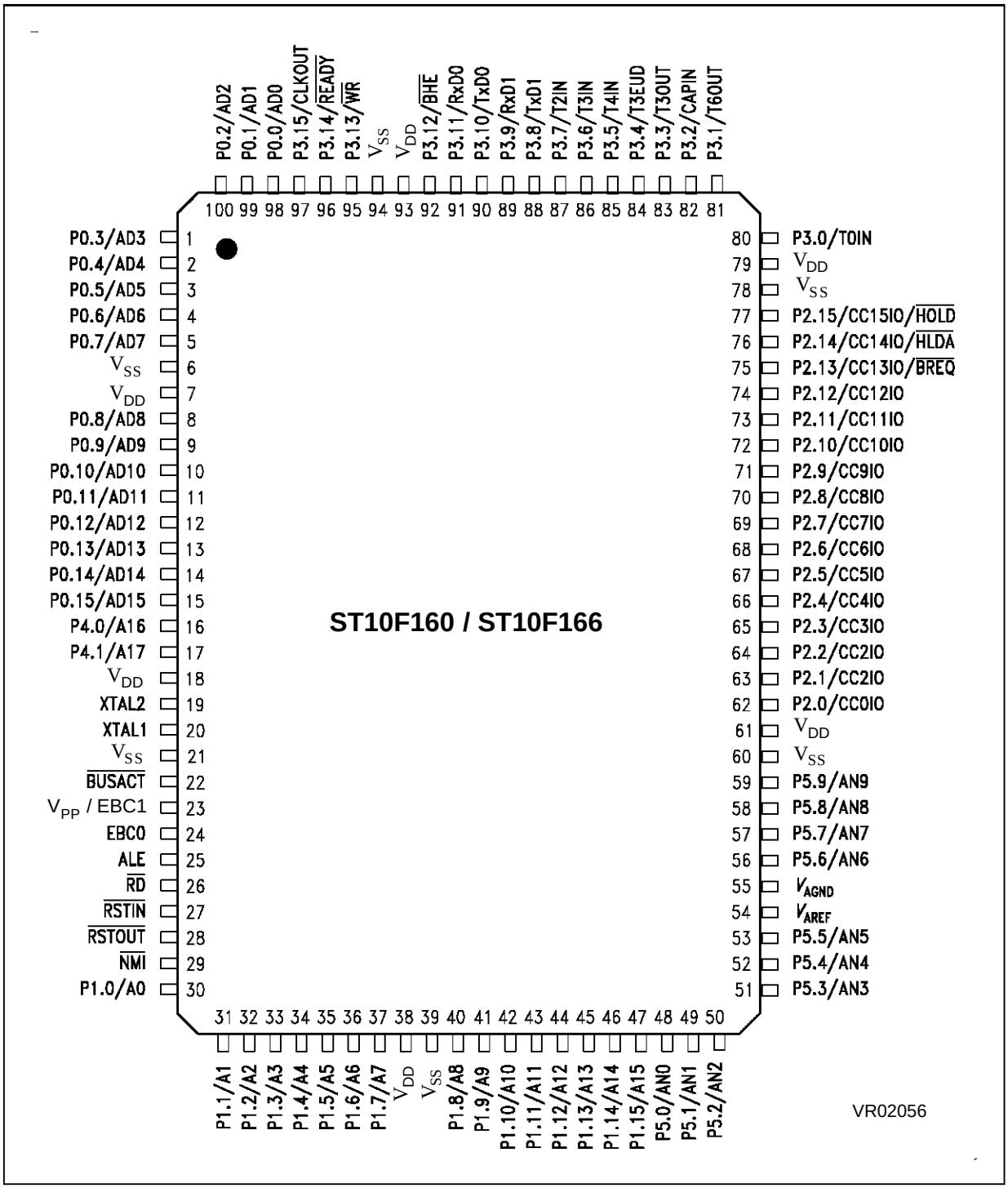


Table 1. Pin Definition and Function

Symbol	Pin Number	Input (I) Output (O)	Function
P4.0 – P4.1	16 - 17	I/O	Port 4 is a 2-bit bidirectional I/O port. It is bit-wise programmable for input or output via direction bits. For a pin configured as input, the output driver is put into high-impedance state. In case of an external bus configuration, Port 4 can be used to output the segment address lines: P4.0A16Least Significant Segment Addr. Line P4.1A17Most Significant Segment Addr. Line
	16 17	O O	
XTAL1 XTAL2	20 19	I O	XTAL1:Input to the oscillator amplifier and input to the internal clock generator XTAL2:Output of the oscillator amplifier circuit. To clock the device from an external source, drive XTAL1, while leaving XTAL2 unconnected. Minimum and maximum high/low and rise/fall times specified in the AC Characteristics must be observed.
$\overline{BUSACT}$, EBC1, EBC0	22 23 24	 I I I	External Bus Configuration selection inputs. These pins are sampled during reset and select either the single chip mode or one of the four external bus configurations: $\overline{BUSACT}$ EBC1 EBC0 Mode/Bus Configuration 00 0 8-bit demultiplexed bus 00 1 8-bit multiplexed bus 01 0 16-bit muliplexed bus 01 1 16-bit demultiplexed bus 10 0 Single chip mode 10 1 Reserved. 11 0 Reserved. 11 1 Reserved.
V_{PP}	23		After reset pin EBC1 accepts the programming voltage for the Flash Memory as an “alternate function”: Flash Memory Programming Voltage V_{PP} = 12 V.
$\overline{RSTIN}$	27	I	Reset Input with Schmitt-Trigger characteristics. A low level at this pin for a specified duration while the oscillator is running resets the ST10R165. An internal pullup resistor permits power-on reset using only a capacitor connected to V_{SS}.
$\overline{RSTOUT}$	28	O	Internal Reset Indication Output. This pin is set to a low level when the part is executing either a hardware-, a software- or a watchdog timer reset. $\overline{RSTOUT}$ remains low until the EINIT (end of initialization) instruction is executed.

Table 1. Pin Definition and Function

Symbol	Pin Number	Input (I) Output (O)	Function
$\overline{NMI}$	29	I	Non-Maskable Interrupt Input. A high to low transition at this pin causes the CPU to vector to the $\overline{NMI}$ trap routine. When the PWRDN (power down) instruction is executed, the $\overline{NMI}$ pin must be low in order to force the ST10R165 to go into power down mode. If $\overline{NMI}$ is high, when PWRDN is executed, the part will continue to run in normal mode. If not used, pull $\overline{NMI}$ high externally.
ALE	25	O	Address Latch Enable Output. Can be used for latching the address into external memory or an address latch in the multiplexed bus modes.
RD	26	O	External Memory Read Strobe. $\overline{RD}$ is activated for every external instruction or data read access.
P1.0 – P1.15	30 - 37 40 - 47	I/O	Port 1 is a 16-bit bidirectional I/O port. It is bit-wise programmable for input or output via direction bits. For a pin configured as input, the output driver is put into high-impedance state. Port 1 is used as the 16-bit address bus (A) in demultiplexed bus modes and also after switching from a demultiplexed bus mode to a multiplexed bus mode..
P5.0 – P5.9	48 – 53 56 – 59	I I	Port 5 is a 10-bit input-only port with Schmitt-Trigger characteristics. The pins of Port 5 also serve as the (up to 10) analog input channels for the A/D converter, where P5.x equals ANx (Analog input channel x) for ST10F166 & ST10F166-16.
P2.0 – P2.15	62 – 77 62 ... 75 76 77	I/O I/O I/O O I/O O I/O I	Port 2 is a 16-bit bidirectional I/O port. It is bit-wise programmable for input or output via direction bits. For a pin configured as input, the output driver is put into high-impedance state. The following Port 2 pins also serve for alternate functions: P2.0CC0IOCAPCOM: CC0 Cap.-In/Comp.Out ... ... P2.13CC13IOCAPCOM: CC13 Cap.-In/Comp.Out, $\overline{BREQ}$External Bus Request Output P2.14CC14IOCAPCOM: CC14 Cap.-In/Comp.Out, $\overline{HLDA}$External Bus Hold Acknowl. Output P2.15CC15IOCAPCOM: CC15 Cap.-In/Comp.Out, $\overline{HOLD}$External Bus Hold Request Input

Table 1. Pin Definition and Function

Symbol	Pin Number	Input (I) Output (O)	Function
P3.0 – P3.15	80 – 92, 95 – 97	I/O I/O	Port 3 is a 16-bit bidirectional I/O port. It is bit-wise programmable for input or output via direction bits. For a pin configured as input, the output driver is put into high-impedance state. The following Port 3 pins also serve for alternate functions: P3.0T0INCAPCOM Timer T0 Count Input P3.1T6OUTGPT2 Timer T6 Toggle Latch Output P3.2CAPINGPT2 Register CAPREL Capture Input P3.3T3OUTGPT1 Timer T3 Toggle Latch Output P3.4T3EUDGPT1 Timer T3 Ext.Up/Down Ctrl.Input P3.5T4INGPT1 Timer T4 Input for Count/Gate/Reload/Capture P3.6T3INGPT1 Timer T3 Count/Gate Input P3.7T2INGPT1 Timer T2 Input for Count/Gate/Reload/Capture P3.8TxD1ASC1 Clock/Data Output (Asyn./Syn.) P3.9RxD1ASC1 Data Input (Asyn.) or I/O (Syn.) P3.10T×D0ASC0 Clock/Data Output (Asyn./Syn.) P3.11R×D0ASC0 Data Input (Asyn.) or I/O (Syn.) P3.12$\overline{BHE}$Ext. Memory High Byte Enable Signal, P3.13$\overline{WR}$External Memory Write Strobe P3.14$\overline{READY}$Ready Signal Input P3.15CLKOUTSystem Clock Output (=CPU Clock)
	80 81 82 83 84 85 86 87 88 89 90 91 92 95 96 97	I O I O I I I I O I/O O I/O O O I O	
P0.0 – P0.15	98 – 5 8 – 15	I/O	Port 0 is a 16-bit bidirectional IO port. It is bit-wise programmable for input or output via direction bits. For a pin configured as input, the output driver is put into high-impedance state. In case of an external bus configuration, Port 0 serves as the address (A) and address/data (AD) bus in multiplexed bus modes and as the data (D) bus in demultiplexed bus modes. **Demultiplexed bus modes:** Data Path Width:8-bit 16-bit P0.0 – P0.7:D0 – D7 D0 - D7 P0.8 – P0.15:output! D8 - D15 **Multiplexed bus modes:** Data Path Width:8-bit 16-bit P0.0 – P0.7:AD0 – AD7AD0 - AD7 P0.8 – P0.15:A8 - A15 AD8 - AD15
V_{AREF}	54	-	Reference voltage for the A/D converter for ST10F166 & ST10F166-16..
V_{AGND}	55	-	Reference ground for the A/D converter for ST10F166 & ST10F166-16..
V_{DD}	7, 18, 38, 61, 79, 93	-	Digital Supply Voltage: + 5 V during normal operation and idle mode. ≥ 2.5 V during power down mode
V_{SS}	6, 21, 39, 60, 78, 94	-	Digital Ground.

2 MEMORY ORGANIZATION

The memory space of the ST10F166 is configured in a Von Neumann architecture which means that code memory, data memory, registers and I/O ports are organized within the same linear address space which currently includes 256 Kbytes. The entire memory space can be accessed bytewise or wordwise. Particular portions of the on-chip memory have additionally been made directly bit addressable.

The ST10F166 contains 32 Kbytes of FLASH EPROM for code or constant data, mapped in segment 0 or in segment 1 by software.

A large dual port RAM of 1 Kbyte is provided as a storage for user defined variables, for the system stack, general purpose register banks and even for code. A register bank can consist of up to 16 wordwide (R0 to R15) and/or bytewide (RL0, RH0, . . ., RL7, RH7) called General Purpose Registers (GPRs).

512 bytes of the address space are reserved for the Special Function Register (SFR) area. SFRs are registers which are used for controlling and monitoring functions of the different on-chip units. 118 SFRs are currently implemented. Unused SFR addresses are reserved for future members of the ST10 Family.

In order to meet the needs of designs where more memory is required than is provided on chip, up to 256 Kbytes of external RAM and/or ROM can be connected to the microcontroller.

3 EXTERNAL BUS CONTROLLER

All external memory accesses are performed by the on-chip External Bus Controller (EBC). During Reset, it can be programmed to either the Single Chip Mode when no external memory is required, or to one of four different external memory access modes, which are as follow:

16/18 bit Addresses, 8 bit Data, Demultiplexed

16/18 bit Addresses, 8 bit Data, Multiplexed

16/18 bit Addresses, 16 bit Data, Demultiplexed

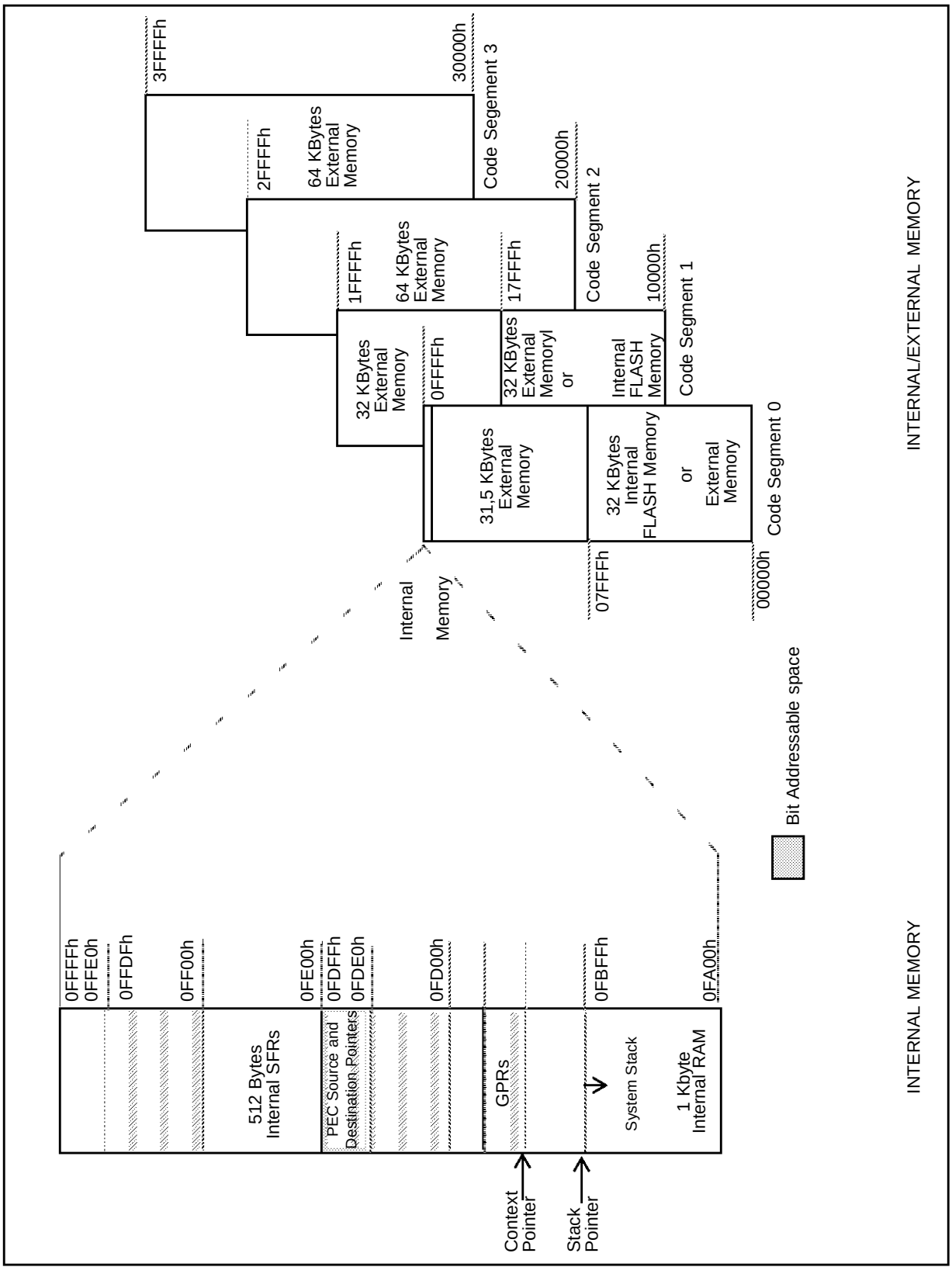
16/18 bit Addresses, 16 bit Data, Multiplexed

In the demultiplexed bus mode, Port 1 is used as an output for addresses and Port 0 is used as an input/output for data. In the multiplexed bus modes, one of the two 16 bit ports, Port 0, is used as an input/output for both addresses and data.

For applications which require less than 64 Kbytes of memory space, a non-segmented memory model can be selected. During the initialization phase, the bus configuration and mapping of the Flash Memory to segment 1 may be programmed. After the EINIT instruction, only the external bus configuration can be changed at any time.

In this case,all memory locations can be addressed by 16 bits, and thus port 4 is not needed as an output for the two significant address biss (A17 and A16, as is the case when using the segmented memory model.

Figure 3. Memory Organization



4 FLASH MEMORY

The ST10F166 provides, in addition to the RAM, 32 k bytes of Electrically Erasable and reprogram-mable non-volatile (FLASH) memory. This memory is organised as 8K x 32 bit allowing a complete instruction to be read during one instruction fetch cycle. Data values stored can be read as 16 bit operands using all addressing modes of ST10F166 instruction set.

The FLASH memory is located in segment 0 (0 to 07FFFh) during reset, and thus contains the reset and interrupt vectors. To provide full flexibility in the use of the ST10F166, the FLASH memory may be remapped to segment ~ (0000 to 17FFFh) during initialization. This allows the interrupt vector to be programmed from external memory, while retaining the common routines and constants programmed into the FLASH memory.

For ease of program updating, the FLASH memory is organised into 4 banks, each of which may be independently Erased.

Table 2. FLASH memory Bank Organisation

Bank	Addresses (Segment 0)	Size (bytes)
0	00000h to 02FFFh	12K
1	03000h to 05FFFh	12K
2	06000h to 077FFh	6K
3	07800h to 07FFFh	2K

5 FLASH MEMORY PROGRAMMING AND ERASURE

The FLASH memory is programmed using the PRESTO F Program Write algorithm for reliability. This algorithm provides a typical programming time of 25µs per word and erasing of 1s per bank.

Erasure of the FLASH memory is performed in the program mode using the PRESTO F Erase algo-rithm, and operates on the selected bank of the memory.

Timing of the Write/Erase cycles is automatically generated by a programmable timer and completion is indicated by a flag. A second flag indicates that the V_{PP} voltage was correct for the whole programming cycle to ensure reliability.

The FLASH memory features a typical endurance of 100 Erase/Program cycles.

6 FLASH MEMORY SECURITY

Security and reliability are enhanced by the built-in features. A key code sequence is used to enter the Write/Erase mode preventing false write cycles, while a programmable option (set by the programming board) prevent any access to the FLASH memory from the internal RAM or from External Memory. If the security option is set, the FLASH memory is accessed only from program within the FLASH memory area. This protection may be disabled by instructions executed from the FLASH memory only (when not in write/erase mode).

Figure 4. PRESTO F Program Write Algorithm

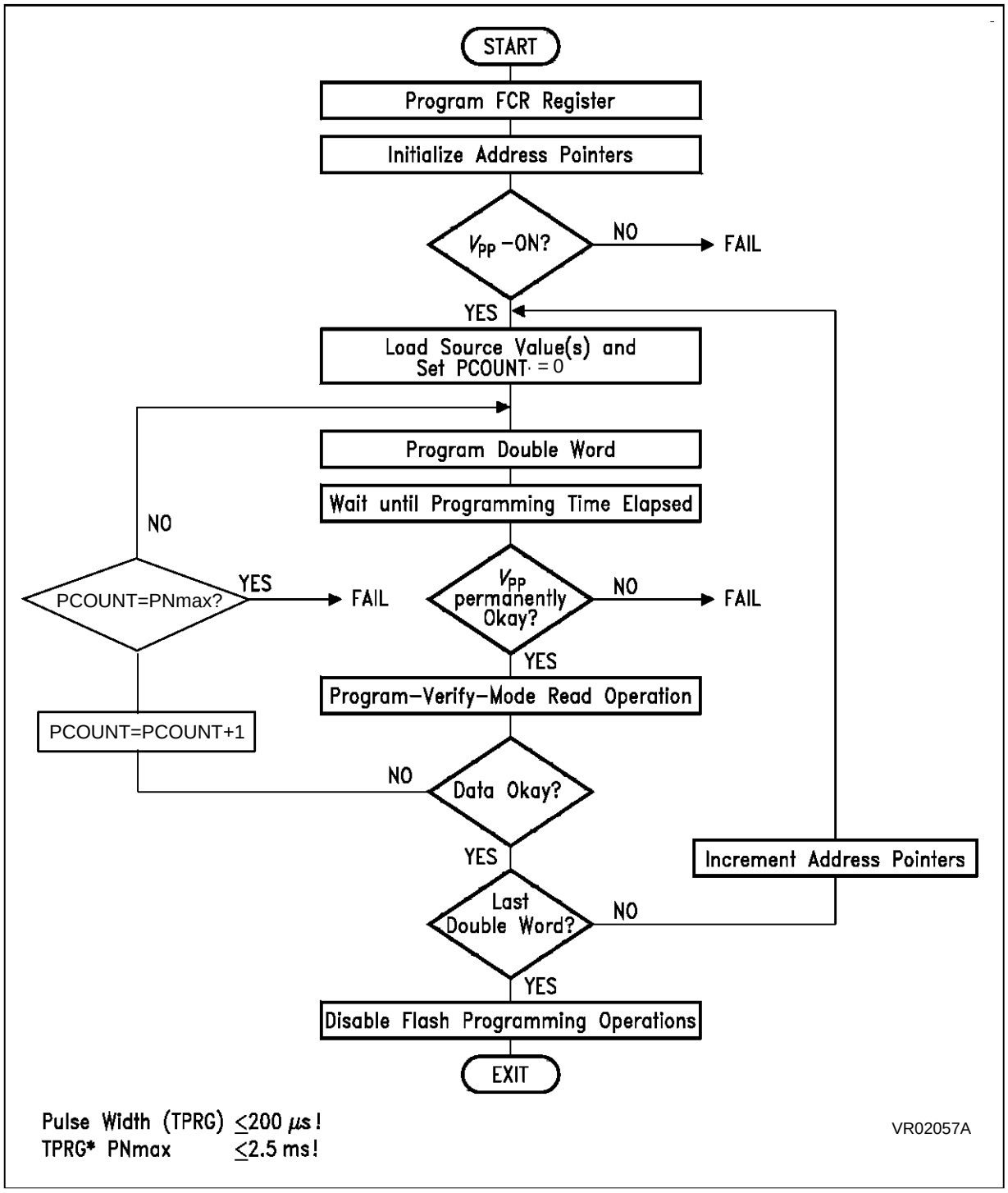
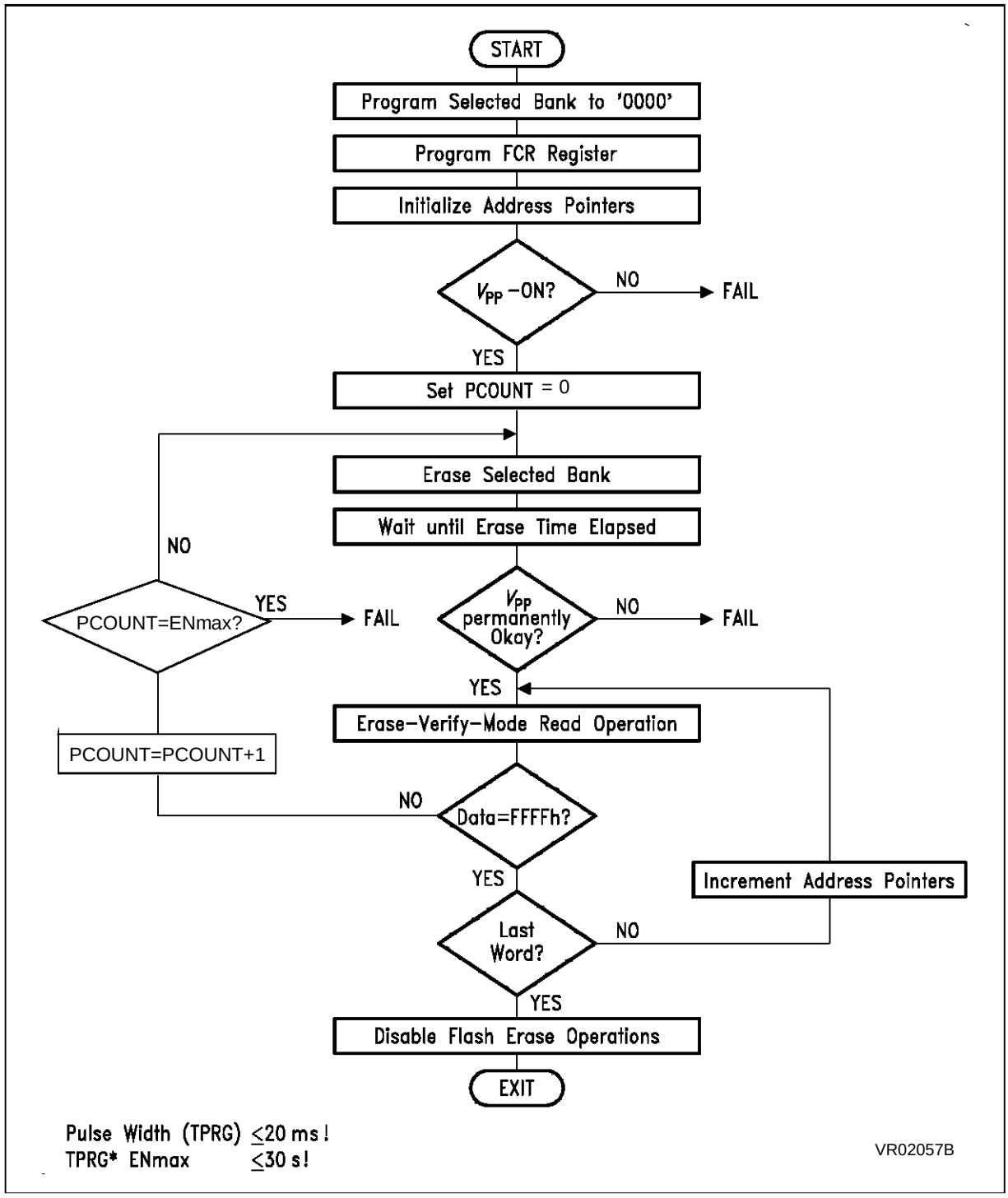


Figure 5. PRESTO F Erase Algorithm



7 CENTRAL PROCESSING UNIT (CPU)

The main core of the CPU consists of a 4-stage instruction pipeline, a 16-bit arithmetic and logic unit (ALU) and dedicated SFRs. Additional hardware provide a separate multiply and divide unit, a bit-mask generator and a barrel shifter.

Based on these hardware provisions, most of the ST10F166 instructions can be executed in just one machine cycle which requires 100 ns at 20 MHz CPU clock. For example, shift and rotate instructions are always processed during one machine cycle independent of the number of bits to be shifted. For fast execution: All multiple-cycle instructions have been optimized . A 32-/16 bit division in 1 μs, a 16 × 16 bit multiplication in 0.5 μs, and program branches in 200 ns. Another pipeline optimization, the 'Jump Cache', allows reducing the execution time of repeatedly performed jumps in a loop from 200 ns to 100 ns.

The CPU disposes of an actual register context consisting of up to 16 wordwide GPRs which are physically allocated within the on-chip RAM area. A Context Pointer (CP) register determines the base address of the active register bank to be accessed by the CPU at the time. The number of register banks is only restricted by the available internal RAM space. For easy parameter passing, register banks can also be organized to overlapping.

A system stack of up to 512 bytes is provided as a storage for temporary data. The system stack is allocated in the on-chip RAM area, and it is accessed by the CPU via the stack pointer (SP) register. Two separate SFRs, STKOV and STKUN, are implicitly compared against the stack pointer value upon each stack access for the detection of a stack overflow or underflow.

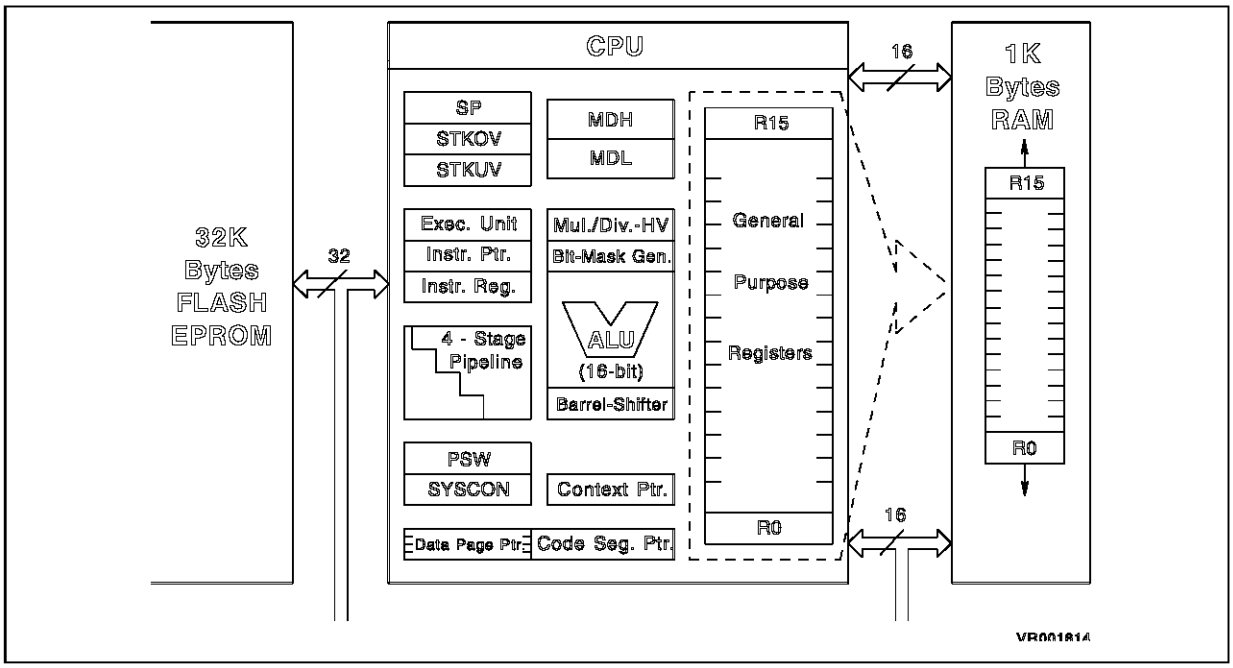
C.P.U. (Cont'd)

The high performance offered by the hardware implementation of the CPU can efficiently be used by a programmer via the highly functional ST10F166 instruction set which includes the following instruction classes:

– Arithmetic Instructions
– Logical Instructions
– Boolean Bit Manipulation Instructions
– Compare and Loop Control Instructions
– Shift and Rotate Instructions
– Prioritize Instruction
– Data Movement Instructions
– System Stack Instructions
– Jump and Call Instructions
– Return Instructions
– System Control Instructions
– Miscellaneous Instructions

The basic instruction length is either 2 or 4 bytes. Possible operand types are bits, bytes and words. A variety of direct, indirect or immediate addressing modes are provided to specify the required operands

Figure 6. CPU Block Diagram



8 INTERRUPT SYSTEM

With an interrupt response time within a range from 250 ns to 500 ns (in case of internal program execution), the ST10F166 is capable of reacting very fast to the occurance of non-deterministic events.

The architecture of the ST10F166 supports several mechanisms for fast and flexible response to service requests that can be generated from various sources internal or external to the microcontroller. Any of these interrupt requests can be programmed to being serviced by the Interrupt Controller or by the Peripheral Event Controller (PEC).

In contrast to a standard interrupt service where the current program execution is suspended and a branch to the interrupt vector table is performed, just one cycle is 'stolen' from the current CPU activity to perform a PEC service. A PEC service implies a single byte or word data transfer between any two memory locations with an optional increment of either the PEC source or the destination pointer. An individual PEC transfer counter is implicitly decremented for each PEC service except when operating in the continuous transfer mode. When this counter reaches zero, a standard interrupt is performed to the corres-ponding source related vector location.

PEC services are very well suited, for example, for supporting the transmission or reception of blocks of data, or for transferring A/D converted results to a memory table. The ST10F166 has 8 PEC chan-nels each of which offers such fast interrupt-driven data transfer capabilities.

A separate control register which contains an interrupt request flag, an interrupt enable flag and an interrupt priority bit field exists for each of the possible interrupt sources. Via its related register, each source can be programmed to one of sixteen interrupt priority levels. Once having been accepted by the CPU, an interrupt service can only be interrupted by a higher prioritized service request. For the standard interrupt processing, each of the possible interrupt sources has a dedicated vector location.

Software interrupts are supported by means of the 'TRAP' instruction in combination with an individual trap (interrupt) number.

The ST10F166 also provides an efficient mechanism to identify and to process 'HardwareTraps' exceptions or error conditions that arise during run-time. Hardware traps cause immediate non-maskable system reaction which is similar to a standard interrupt service (branching to a dedicated vector table location).

The occurrence of a hardware trap is additionally signified by an individual bit in the trap flag register (TFR).

Interrupt System (Cont'd)

The following table shows all of the possible ST10F166 interrupt sources and the corresponding hardware-related interrupt flags, vectors, vector locations and trap (interrupt) numbers:

Table 3. Interrupt Sources and Hardware Location

Source of Interrupt or PEC Service Request	Request Flag	Enable Flag	Interrupt Vector	Vector Location	Trap Number
CAPCOM Register 0	CC0IR	CC0IE	CC0INT	40h	10h
CAPCOM Register1	CC1IR	CC1IE	CC1INT	44h	11h
CAPCOM Register 2	CC2IR	CC2IE	CC2INT	48h	12h
CAPCOM Register 3	CC3IR	CC3IE	CC3INT	4Ch	13h
CAPCOM Register 4	CC4IR	CC4IE	CC4INT	50h	14h
CAPCOM Register 5	CC5IR	CC5IE	CC5INT	54h	15h
CAPCOM Register 6	CC6IR	CC6IE	CC6INT	58h	16h
CAPCOM Register 7	CC7IR	CC7IE	CC7INT	5Ch	17h
CAPCOM Register 8	CC8IR	CC8IE	CC8INT	60h	18h
CAPCOM Register 9	CC9IR	CC9IE	CC9INT	64h	19h
CAPCOM Register 10	CC10IR	CC10IE	CC10INT	68h	1Ah
CAPCOM Register 11	CC11IR	CC11IE	CC11INT	6Ch	1Bh
CAPCOM Register 12	CC12IR	CC12IE	CC12INT	70h	1Ch
CAPCOM Register 13	CC13IR	CC13IE	CC13INT	74h	1Dh
CAPCOM Register 14	CC14IR	CC14IE	CC14INT	78h	1Eh
CAPCOM Register 15	CC15IR	CC15IE	CC15INT	7Ch	1Fh
CAPCOM Timer 0	T0IR	T0IE	T0INT	80h	20h
CAPCOM Timer 1	T1IR	T1IE	T1INT	84h	21h
GPT 1 Timer 2	T2IR	T2IE	T2INT	88h	22h
GPT 1 Timer 3	T3IR	T3IE	T3INT	8Ch	23h
GPT 1 Timer 4	T4IR	T4IE	T4INT	90h	24h
GPT 1 Timer 5	T5IR	T5IE	T5INT	94h	25h
GPT 1 Timer 6	T6IR	T6IE	T6INT	98h	26h
GPT 2 CAPREL Register	CRIR	CRIE	CRINT	9Ch	27h
A/D Conversion Complete	ADCIR	ADCIE	ADCINT	A0h	28h
A/D Overrun Error	ADEIR	ADEIE	ADEINT	A4h	29h
Serial Channel 0 Transmit	S0TIR	S0TIE	S0TINT	A8h	2Ah
Serial Channel 0 Receive	S0RIR	S0RIE	S0RINT	ACh	2Bh
Serial Channel 0 Error	S0EIR	S0EIE	S0EINT	B0h	2Ch
Serial Channel 1 Transmit	S1TIR	S1TIE	S1TINT	B4h	2Dh
Serial Channel 1 Receive	S1RIR	S1RIE	S1RINT	B8h	2Eh
Serial Channel 1 Error	S1EIR	S1EIE	S1EINT	BCh	2Fh

Interrupt System (Cont'd)

Except when another higher prioritized trap service being in progress, a hardware trap will interrupt any actual program execution. In turn, hardware trap services can normally not be interrupted by standard or PEC interrupts.

The following table shows all of the possible exceptions or error conditions that can arise during run-time:

Table 4. Exceptions and Errors during Runtime

Exception Condition	Trap Flag	Trap Vector	Vector Location	Trap Number	Trap priority
Reset Functions:					
Hardware Reset		RESET	0h	0h	III
Software Reset		RESET	0h	0h	III
Watchdog Timer Overflow		RESET	0h	0h	III
Class A Hardware Traps:					
Non-Maskable Interrupt	NMI	NMITRAP	08h	2h	II
Stack Overflow	STKOF	STOP-TRAP	10h	4h	II
Stack Underflow	STKUF	STUTRAP	18h	6h	II
Class B Hardware Traps:					
Undefined Opcode	UNDOPC	BTRAP	28h	Ah	I
Protected Instruction Fault	PRTFLT	BTRAP	28h	Ah	I
Illegal Word Operand Access	ILLOPA	BTRAP	28h	Ah	I
Illegal Instruction Access	ILLINA	BTRAP	28h	Ah	I
Illegal External Bus Access	ILLBUS	BTRAP	28h	Ah	I
Reserved			[2Ch - 3Ch]	[Bh - Fh]	
Software Traps TRAP Instruction			Any [0h - 1FCh] in steps of 4h	Any [0h - 7Fh]	Current CPU Priority

9 A/D CONVERTER

For analog signal measurement, a 10-bit A/D converter with 10 multiplexed input channels, a sample and hold circuit has been integrated on-chip. It uses the method of successive approximation which returns the conversion result for an analog channel within 9.75 µs (@fosc = 40 MHz).

Overrun error detection capability is provided for the conversion result register (ADDAT): an interrupt request will be generated when the result of a previous conversion has not been read from the result register at the time the next conversion is complete.

For applications which require less than 10 analog input channels, the remaining channels can be used as digital input port pins.

The A/D converter of the ST10F166 supports four different conversion modes. In the standard Single Channel conversion mode, the analog level on a specified channel is once sampled and converted into a digital result. In the Single Channel Continuous mode, the analog level is repeatedly sampled and converted without software intervention. In the Auto Scan mode, the analog levels on a prespecified number of channels are sequentially sampled and converted. In the Auto Scan Continuous mode, the number of prespecified channels is repeatedly sampled and converted.

The Peripheral Event Controller (PEC) may be used to automatically store the conversion results into a table in memory for later evaluation, without requiring the overhead of entering and exiting interrupt routines for each data transfer.

10 SERIAL CHANNELS

Serial communication with other microcontrollers, processors, terminals, or external peripheral components is provided by two serial interfaces with identical functionality, Serial Channel 0 (ASC0) and Serial Channel 1 (ASC1).

They support full-duplex asynchronous communication up to 625 Kbaud and half-duplex synchronous communication up to 2.5 Mbaud.

Two dedicated baud rate generators allow to set up all standard baud rates without oscillator tuning. For transmission, reception, and erroneous reception 3 separate interrupt vectors are provided for each serial channel.

In the synchronous mode, one data byte is transmitted or received synchronously to a shift clock which is generated by the ST10F166. In the asynchronous mode, an 8- or 9-bit data frame is transmitted or received, preceded by a start bit and terminated by one or two stop bits. For multiprocessor communication, a mechanism to distinguish address from data bytes has been included (8-bit data + wake up bit mode), and a loop back option is available for testing purposes.

A number of optional hardware error detection capabilities has been included to increase the reliability of data transfers. A parity bit can automatically be generated on transmission or be checked on reception. Framing error detection allows to recognize data frames with missing stop bits. An overrun error will be generated if the last character received has not been read out of the receive buffer register at the time the reception of a new character is complete.

11 WATCHDOG TIMER

The Watchdog Timer of the ST10F166 represents one of the fail-safe mechanisms which have been implemented to prevent the controller from malfunctioning for longer periods of time.

The Watchdog Timer of the ST10F166 is always enabled after a reset of the chip, and can only be disabled in the time interval until the EINIT (end of initialization) instruction has been executed. Thus, the chip's start-up procedure is always monitored. When the software has been designed to service the Watchdog Timer before it overflows, the Watchdog Timer times out if the program does not progress properly due to hardware or software related failures. When the Watchdog Timer overflows, it generates an internal hardware reset and pulls the $\overline{\text{RSTOUT}}$ pin low in order to allow external hardware components to reset.

The Watchdog Timer of the ST10F166 is a 16-bit timer which can either be clocked with fosc/4 or fosc/256. The high byte of the Watchdog Timer register can be set to a prespecified reload value (stored in WDTREL) in order to allow further variation of the monitored time interval. Each time it is serviced by the application software, the high byte of the Watchdog Timer is reloaded. Thus, time intervals between 25 µs and 420 ms can be monitored (@fosc = 40 MHz). The default Watch-dog Timer interval after reset is 6.55 ms.

12 PARALLEL PORTS

The ST10F166 provides 76 I/O lines which are organized into four 16-bit I/O ports (Port 0 through 3), one 2-bit I/O port (Port 4), and one 10-bit input port (Port 5). All port lines are bit addressable, and all lines of Port 0 through 4 are individually bit programmable as inputs or outputs via direction registers. The I/O ports are true bidirectional ports which are switched to the high impedance state when configured as inputs. During the internal reset, all port pins are configured as inputs.

Each port line has one programmable alternate input or output function associated with it. Ports 0 and 1 may be used as address and data lines when accessing external memory, while Port 4 outputs the additional segment address bits A16 and A17 in systems where segmentation is enabled to access more than 64 Kbytes of memory. Port 2 is associated with the capture inputs/compare outputs of the CAPCOM unit, and Port 3 includes alternate functions of timers, serial interfaces, optional bus control signals ($\overline{\text{WR}}$, $\overline{\text{BHE}}$, $\overline{\text{READY}}$), and the system clock output (CLKOUT). Port 5 is used for the analog input channels to the A/D converter. When none of the alternate functions is not used, the respective port line may be used as general purpose I/O line.

13 CAPTURE/COMPARE UNIT (CAPCOM)

The CAPCOM unit supports generation and control of timing sequences on up to 16 channels, with a maximum resolution of 400 ns. The CAPCOM unit is typically used to handle high speed I/O tasks such as pulse and waveform generation, pulse width modulation (PWM), Digital to Analog (D/A) conversion, software timing, or time recording relative to external events.

Two 16-bit timers (T0/T1) with reload registers provide two independent time bases for the capture/compare register array.

The input clock for the timers is programmable to several prescaled values of the internal system clock, or may be derived from an overflow/underflow of timer T6 in module GPT2. This provides a wide range of variation for the timer period and resolution and allows precise adjustment to the application specific requirements. In addition, an external count input for CAPCOM timer T0 allows event scheduling for the capture/compare registers relative to external events.

The capture/compare register array contains 16 dual purpose capture/compare registers, each of which may be individually allocated to either CAPCOM timer T0 or T1, and programmed for capture or compare function. Each register has one port pin associated with it which serves as an input pin for triggering the capture function, or as an output pin to indicate the occurrence of a compare event.

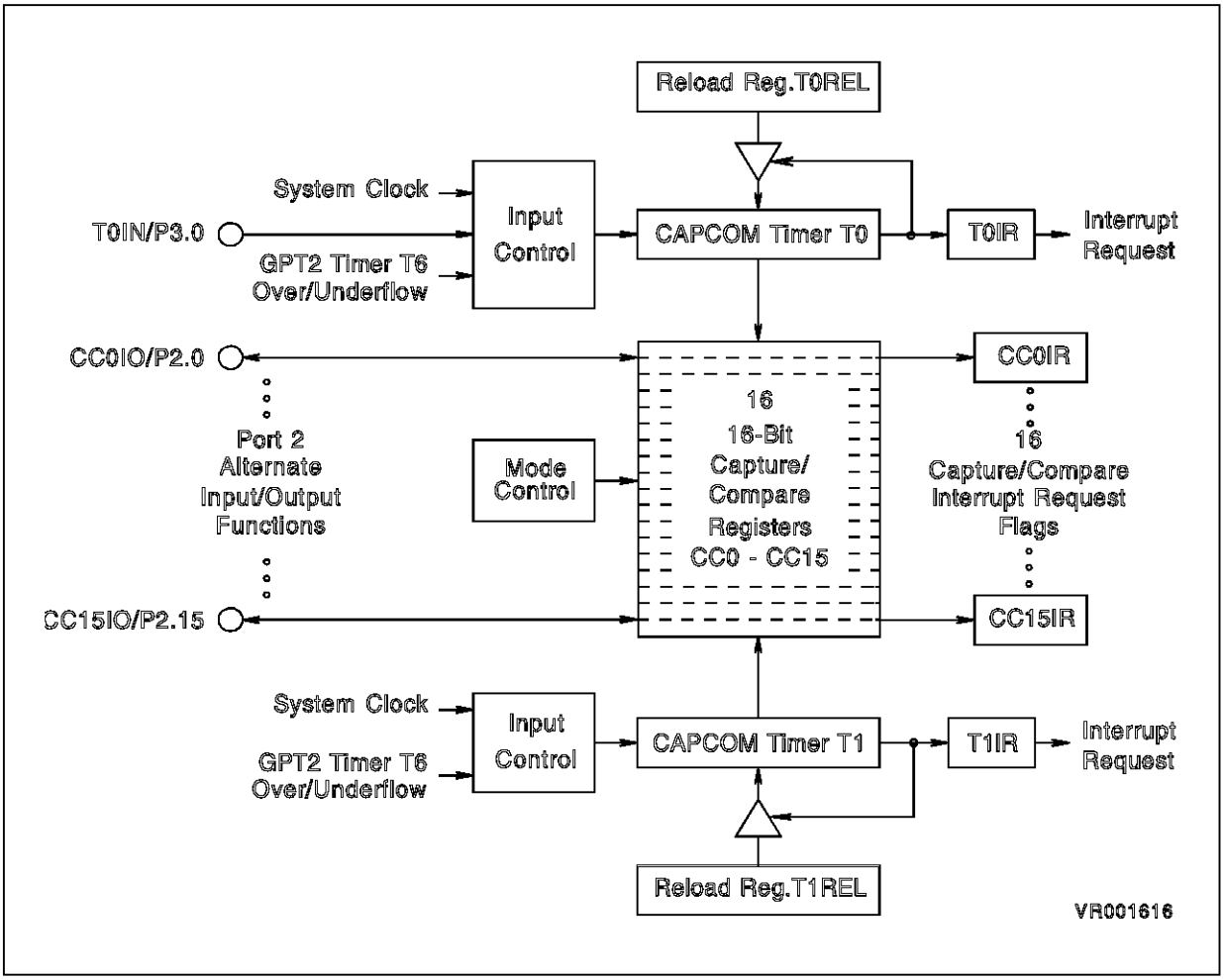
When a capture/compare register has been selected for capture mode, the current contents of the allocated timer will be latched ('captured') into the capture/compare register in response to an external event at the port pin which is associated with this register. In addition, a specific interrupt request for this capture/compare register is generated. Either a positive, a negative, or both a positive and a negative external signal transition at the pin can be selected as the triggering event. The contents of all registers which have been selected for one of the five compare modes are continuously compared with the contents of the allocated timers. When a match occurs between the timer value and the value in a capture/compare register, specific actions will be taken based on the selected compare mode.

CAPCOM (Cont'd)

Table 5. Compare Modes

Compare Modes	Functions
Mode 0	Interrupt-only compare mode; several compare interrupts per timer period are possible
Mode 1	Pin toggles on each compare match; several compare events per timer period are possible
Mode 2	Interrupt-only compare mode; only one compare interrupt per timer period is generated
Mode 3	Pin set to '1' on match; pin reset to '0' on compare timer overflow; only one compare event per timer period is generated
Double Register Mode	Two registers operate on one pin; pin toggles on each compare match; several compare events per timer period are possible.

Figure 7. CAPCOM Block Diagram



14 GENERAL PURPOSE TIMER (GPT) UNIT

The GPT unit represents a very flexible multifunctional timer counter structure which may be used for many different time related tasks such as event timing and counting, pulse width and duty cycle measurements, pulse generation, or pulse multiplication.

The GPT unit incorporates five 16-bit timers which are organized in two separate modules, GPT1 and GPT2. Each timer in each module may operate independently in a number of different modes, or may be concatenated with another timer of the same module.

Each of the three timers T2, T3, T4 of the GPT1 module can be configured individually for one of three basic modes of operation, which are Timer, Gated Timer, and Counter Mode. In Timer Mode, the input clock for a timer is derived from the internal system clock, divided by a programmable prescaler, while Counter Mode allows a timer to be clocked in reference to external events.

Pulse width or duty cycle measurement is supported in Gated Timer Mode, where the operation of a timer is controlled by the 'gate' level on an external input pin. For these purposes, each timer has one associated port pin (T2IN, T3IN, T4IN) which serves as gate or clock input. The maximum resolution of the timers in the GPT1 module is 400 ns (@f_{osc} = 40 MHz).

The count direction (up/down) for each timer is programmable by software. For timer T3, the count direction may additionally be altered dynamically by an external signal on a port pin (T3EUD) to facilitate functions such as position tracking.

Timer T3 has an output toggle latch (T3OTL) which changes its state on each timer overflow/underflow. The state of this latch may be output on a port pin (T3OUT) e. g. for time out monitoring of external hardware components, or may be used internally to clock timers T2 and T4 for measuring long time periods with high resolution.

G.P.T. (Cont'd)

In addition to their basic operating modes, timers T2 and T4 may be configured as reload or capture registers for timer T3. When used as capture or reload registers, timers T2 and T4 are stopped. The contents of timer T3 are captured into T2 or T4 in response to a signal at their associated input pins (T2IN, T4IN). Timer T3 is reloaded with the contents of T2 or T4 either by an external signal or by a selectable state transition of its toggle latch T3OTL. When both T2 and T4 are configured to alternately reload T3 on opposite state transitions of T3OTL with the low and high times of a PWM signal, this signal can be constantly generated without software intervention.

With its maximum resolution of 200 ns (@f_{OSC} = 40 MHz), the GPT2 module provides precise event control and time measurement. It includes two timers (T5, T6) and a capture/reload register (CAPREL). Both timers can independently count up or down, clocked with an input clock which is derived from a programmable prescaler.
Concatenation of the timers is supported via the output toggle latch (T6OTL) of timer T6, which changes its state on each timer overflow/underflow.

The state of this latch may be used to clock timer T5, or it may be output on a port pin (T6OUT). The overflows/underflows of timer T6 can additionally be used to clock the CAPCOM timers T0 or T1, and to cause a reload from the CAPREL register. The CAPREL register may capture the contents of timer T5 based on an external signal transition on the corresponding port pin (CAPIN), and timer T5 may optionally be cleared after the same signal transition. This allows absolute time differences to be measured or pulse multiplication to be performed without software overhead.

G.P.T. (Cont'd)

Figure 8. GPT1 Block Diagram

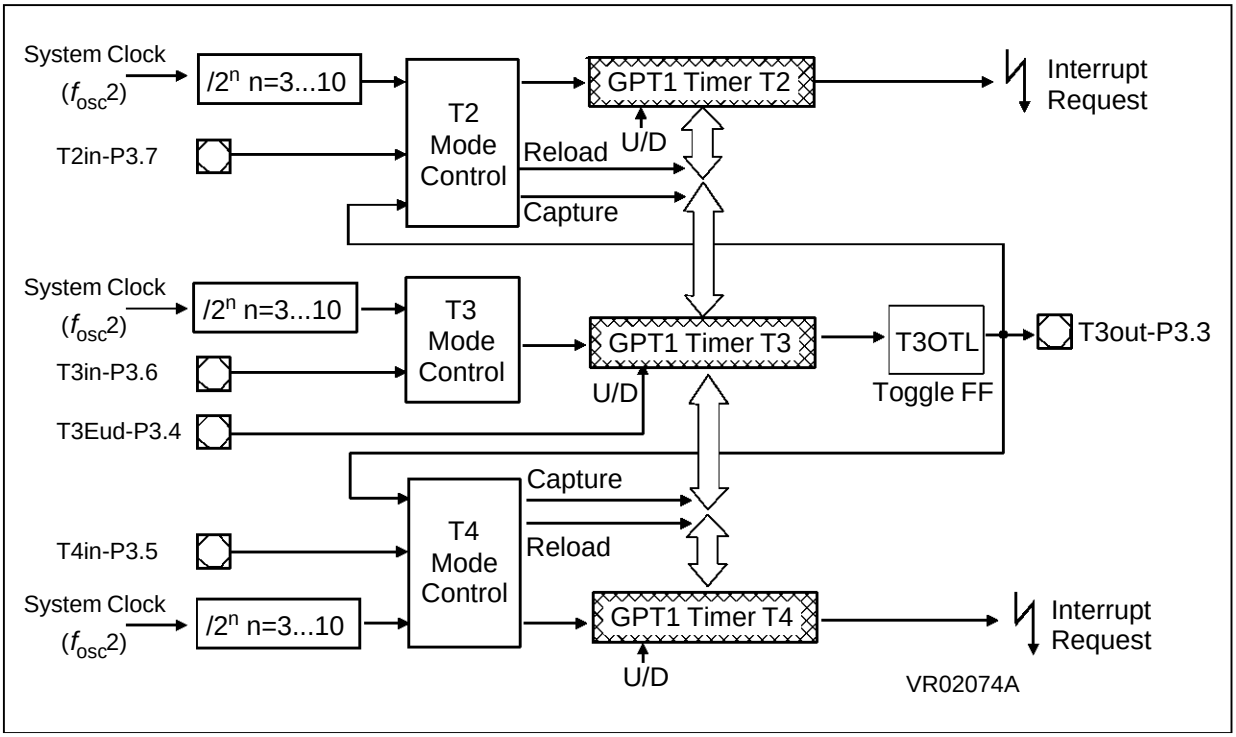
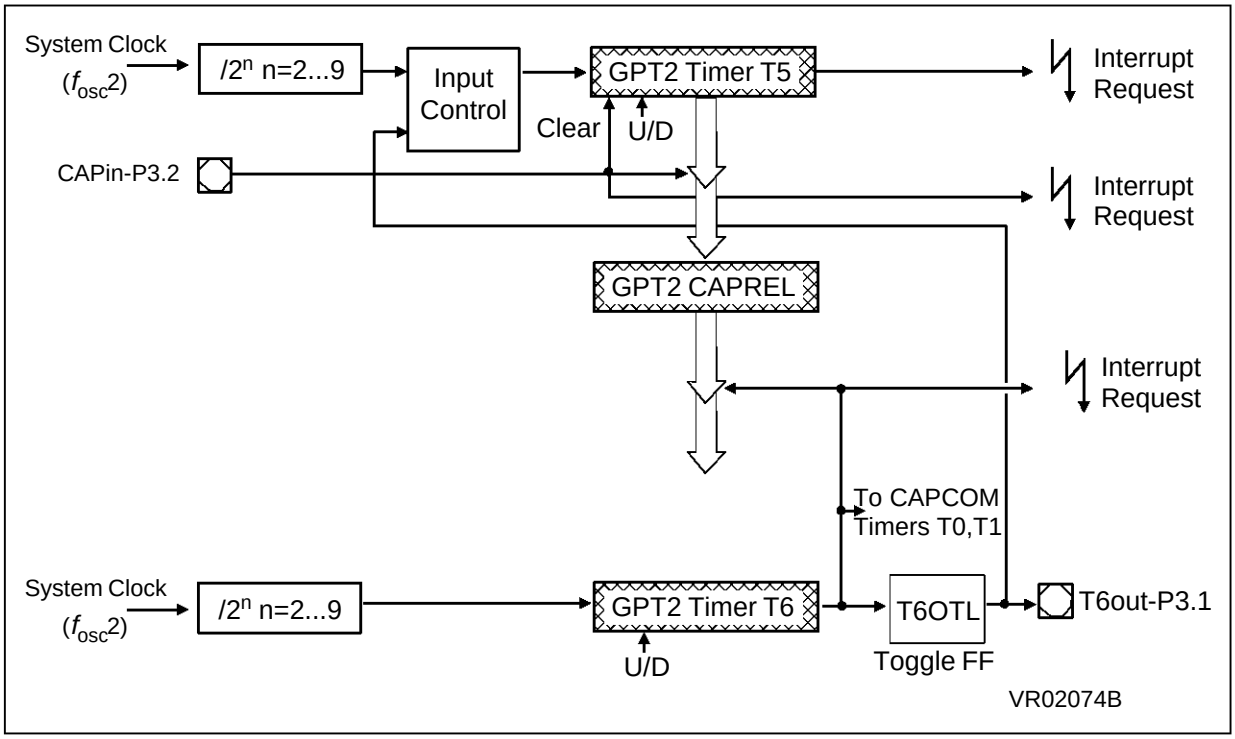


Figure 9. GPT2 Block Diagram



15 SOFTWARE DESCRIPTION

Addressing Modes

The ST10F166 offers different powerful addressing modes to facilitate rapid access on word, byte and bit data, or to specify the destination address of a branch instruction. The addressing modes are subdivided in six different categories as follows.

Short addressing modes: an implicit base offset address is used to specify a physical 18-bit address.

EA = Base Address + k Short Address.
k = 1 or 2
EA = Effective Address

This mode allows direct access to any GPR or SFR and any word in the bit-addressable memory space. (in case of a byte operation on an SFR, only the low byte can be accessed via ‘reg’).

Long addressing modes: one of the four DPP registers, selected by bit 15 and 14 of the 16-bit address, is used to specify a physical 18-bit address.

EA = Contents of DPPi + Page Offset Address
i: specified by bit 15, 14 of the 16 bit address.
Page Offset Address: bit 13 to 0 of the 16 bit address.

In this mode, any word or byte data within the entire memory space can be accessed directly . Word accesses may not be performed on odd byte addresses, otherwise a hardware trap will occur.

Indirect addressing modes: a 16-bit long address is specified indirectly by the contents of a word GPR which is specified directly by a short address. Any word GPR can be used, except for arithmetic, logical and compare instructions, where only R0 to R3 are allowed. There are also certain modes which allow decrementing or incrementing the indirect address pointers by a data-type-dependent value.

Long Address = [GPR Address] + Constant

EA = Contents of DPPi + Page Offset Address
i: specified by bit 15, 14 of the Long Address.
Page Offset Address: bit 13 to 0 of the long address
Long Address Long Address
bit15,14 specify i bit 13 to 0

Immediate data: these data are represented in the instruction formats by either 3,4,8 or 16 bits.

Branch target addressing modes: to specify the destination address and segment of jump or call instructions, relative, absolute and indirect modes can be used to update the Instruction Pointer (IP) register while the Code Segment Pointer (CSP) register can be updated only with absolute values.

Condition Flags:

The condition flags of the PSW register (N,C,V,Z,E) indicate the ALU status due to the last performed ALU operation. They are set by most of the instructions due to specific rules which depend on the ALU or data movement operation performed by an instruction. If the PSW register is the destination operand of an instruction, the PSW flags do NOT represent the condition flags of this instruction as usual.

E: End of a table in a table search operation

Z: Zero

V: Overflow

C: Carry

N: Negative

Software Description (Cont'd)

Table 6. Addressing Mode Summary

Addressing Mode	Notation
3 bit Immediate Data	#data3
4 bit Immediate Data	#data4
8 bit Immediate Data	#data8
16 bit Immediate Data	#data16
8 bit Immediate Mask	#mask
GPR register direct	Rw Rb
SFR or GPR register direct	reg
Memory direct	Mem
Memory indirect	[Rw]
Memory indirect with Post-increment	[Rw+]
Memory indirect with Pre-decrement	[-Rw]
Memory indirect with a 16-bit cinstant	[Rw+#data16]
Direct Word Offset	bitoff
Bit Address	bitaddr.b

Table 7. Condition Code Summary

UC	Unconditional	1=1
Z	Zero	Z=1
NZ	No Zero	Z=0
V	Overflow	V=1
NV	No Overflow	V=0
N	Negative	N=1
NN	Not Negative	N=0
C	Carry	C=1
NC	No Carry	C=0
EQ	Equal	Z=1
NE	Not Equal	Z=0
ULT	Unsigned Less Than	C=1
UGE	Unsigned Greater Than or Equal	C=0
ULE	Unsigned Less Than or Equal	(Z or C)=1
UGT	Unsigned Greater Than	(Z or C)=0
SLT	Signed Less Than	(N xor V)=1
SGE	Signed Greater Than or Equal	(N xor V)=0
SLE	Signed Less Than or Equal	(Z or (N xor V))=1
SGT	Signed Greater Than	(Z or (N xor V))=0
NET	Not Equal AND Not End of Table	(Z or E)=0

16 INSTRUCTION SET SUMMARY

The table below lists the instructions of the ST10F166 in a condensed way.
The various addressing modes that can be used with a specific instruction, the operation of the instructions, parameters for conditional execution of instructions, and the opcodes for each instruction can be found in the **"ST10 Programming Manual"**.

This document also provides a detailed description of each instruction.

Mnemonic	Description	Bytes
ADD(B)	Add word (byte) operands	2 / 4
ADDC(B)	Add word (byte) operands with Carry	2 / 4
SUB(B)	Subtract word (byte) operands	2 / 4
SUBC(B)	Subtract word (byte) operands with Carry	2 / 4
MUL(U)	(Un)Signed multiply direct GPR by direct GPR (16-16-bit)	2
DIV(U)	(Un)Signed divide register MDL by direct GPR (16-/16-bit)	2
DIVL(U)	(Un)Signed long divide reg. MD by direct GPR (32-/16-bit)	2
CPL(B)	Complement direct word (byte) GPR	2
NEG(B)	Negate direct word (byte) GPR	2
AND(B)	Bitwise AND, (word/byte operands)	2 / 4
OR(B)	Bitwise OR, (word/byte operands)	2 / 4
XOR(B)	Bitwise XOR, (word/byte operands)	2 / 4
BCLR	Clear direct bit	2
BSET	Set direct bit	2
BMOV(N)	Move (negated) direct bit to direct bit	4
BAND, BOR, BXOR	AND/OR/XOR direct bit with direct bit	4
BCMP	Compare direct bit to direct bit	4
BFLDH/L	Bitwise modify masked high/low byte of bit-addressable direct word memory with immediate data	4
CMP(B)	Compare word (byte) operands	2 / 4
CMPD1/2	Compare word data to GPR and decrement GPR by 1/2	2 / 4
CMPI1/2	Compare word data to GPR and increment GPR by 1/2	2 / 4
PRIOR	Determine number of shift cycles to normalize direct word GPR and store result in direct word GPR	2
SHL / SHR	Shift left/right direct word GPR	2
ROL / ROR	Rotate left/right direct word GPR	2
ASHR	Arithmetic (sign bit) shift right direct word GPR	2
MOV(B)	Move word (byte) data	2 / 4

Instruction Set Summary (Cont'd)

Mnemonic	Description	Bytes
MOVBS	Move byte operand to word operand with sign extension	2 / 4
MOVBZ	Move byte operand to word operand. with zero extension	2 / 4
JMPA, JMPI, JMPR	Jump absolute/indirect/relative if condition is met	4
JMPS	Jump absolute to a code segment	4
J(N)B	Jump relative if direct bit is (not) set	4
JBC	Jump relative and clear bit if direct bit is set	4
JNBS	Jump relative and set bit if direct bit is not set	4
CALLA, CALLI, CALLR	Call absolute/indirect/relative subroutine if condition is met	4
CALLS	Call absolute subroutine in any code segment	4
PCALL	Push direct word register onto system stack and call absolute subroutine	4
TRAP	Call interrupt service routine via immediate trap number	2
PUSH, POP	Push/pop direct word register onto/from system stack	2
SCXT	Push direct word register onto system stack and update register with word operand	4
RET	Return from intra-segment subroutine	2
RETS	Return from inter-segment subroutine	2
RETP	Return from intra-segment subroutine and pop direct word register from system stack	2
RETI	Return from interrupt service subroutine	2
SRST	Software Reset	4
IDLE	Enter Idle Mode	4
PWRDN	Enter Power Down Mode (supposes $\overline{\text{NMI}}$-pin being low)	4
SRVWDT	Service Watchdog Timer	4
DISWDT	Disable Watchdog Timer	4
EINIT	Signify End-of-Initialization on RSTOUT-pin	4
NOP	Null operation	2

17 SPECIAL FUNCTION REGISTER OVERVIEW

The following table lists all SFRs which are implemented in the ST10F166 in alphabetical order.

Bit-addressable SFRs are marked with the letter "**b**" in column "Name".

An SFR can be specified via its individual mnemonic name. Depending on the selected addressing mode, an SFR can be accessed via its physical address (using the Data Page Pointers), or via its short 8-bit address (without using the Data Page Pointers).

Name	Physical Address	8-Bit Address	Description	Reset Value
ADCIC b	FF98h	CCh	A/D Converter End of Conversion Interrupt Control Register	0000h
ADCON b	FFA0h	D0h	A/D Converter Control Register	0000h
ADDAT	FEA0h	50h	A/D Converter Result Register	0000h
ADDRSEL1	FE18h	0Ch	Address Select Register	0000h
ADEIC b	FF9Ah	CDh	A/D Converter Overrun Error Interrupt Control Register	0000h
BUSCON1 b	FF14h	8Ah	Bus Configuration Register	0000h
CAPREL	FE4Ah	25h	GPT2 Capture/Reload Register	0000h
CC0	FE80h	40h	CAPCOM Register 0	0000h
CC0IC b	FF78h	BCh	CAPCOM Register 0 Interrupt Control Register	0000h
CC1	FE82h	41h	CAPCOM Register 1	0000h
CC1IC b	FF7Ah	BDh	CAPCOM Register 1 Interrupt Control Register	0000h
CC2	FE84h	42h	CAPCOM Register 2	0000h
CC2IC b	FF7Ch	BEh	CAPCOM Register 2 Interrupt Control Register	0000h
CC3	FE86h	43h	CAPCOM Register 3	0000h
CC3IC b	FF7Eh	BFh	CAPCOM Register 3 Interrupt Control Register	0000h
CC4	FE88h	44h	CAPCOM Register 4	0000h
CC4IC b	FF80h	C0h	CAPCOM Register 4 Interrupt Control Register	0000h
CC5	FE8Ah	45h	CAPCOM Register 5	0000h
CC5IC b	FF82h	C1h	CAPCOM Register 5 Interrupt Control Register	0000h
CC6	FE8Ch	46h	CAPCOM Register 6	0000h
CC6IC b	FF84h	C2h	CAPCOM Register 6 Interrupt Control Register	0000h
CC7	FE8Eh	47h	CAPCOM Register 7	0000h
CC7IC b	FF86h	C3h	CAPCOM Register 7 Interrupt Control Register	0000h
CC8	FE90h	48h	CAPCOM Register 8	0000h
CC8IC b	FF88h	C4h	CAPCOM Register 8 Interrupt Control Register	0000h

Special Function Register Overview (Cont'd)

Name	Physical Address	8-Bit Address	Description	Reset Value
CC9	FE92h	49h	CAPCOM Register 9	0000h
CC9IC b	FF8Ah	C5h	CAPCOM Register 9 Interrupt Control Register	0000h
CC10	FE94h	4Ah	CAPCOM Register 10	0000h
CC10IC b	FF8Ch	C6h	CAPCOM Register 10 Interrupt Control Register	0000h
CC11	FE96h	4Bh	CAPCOM Register 11	0000h
CC11IC b	FF8Eh	C7h	CAPCOM Register 11 Interrupt Control Register	0000h
CC12	FE98h	4Ch	CAPCOM Register 12	0000h
CC12IC b	FF90h	C8h	CAPCOM Register 12 Interrupt Control Register	0000h
CC13	FE9Ah	4Dh	CAPCOM Register 13	0000h
CC13IC b	FF92h	C9h	CAPCOM Register 13 Interrupt Control Register	0000h
CC14	FE9Ch	4Eh	CAPCOM Register 14	0000h
CC14IC b	FF94h	CAh	CAPCOM Register 14 Interrupt Control Register	0000h
CC15	FE9Eh	4Fh	CAPCOM Register 15	0000h
CC15IC b	FF96h	CBh	CAPCOM Register 15 Interrupt Control Register	0000h
CCM0 b	FF52h	A9h	CAPCOM Mode Control Register 0	0000h
CCM b	FF54h	AAh	CAPCOM Mode Control Register 1	0000h
CCM2 b	FF56h	ABh	CAPCOM Mode Control Register 2	0000h
CCM3 b	FF58h	ACh	CAPCOM Mode Control Register 3	0000h
CP	FE10h	08h	CPU Context Pointer Register	FC00h
CRIC b	FF6Ah	B5h	GPT2 CAPREL Interrupt Control Register	0000h
CSP	FE08h	04h	CPU Code Segment Pointer Register (2 bits, read only)	0000h
DP0 b	FF02h	81h	Port 0 Direction Control Register	0000h
DP1 b	FF06h	83h	Port 1 Direction Control Register	0000h
DP2 b	FFC2h	E1h	Port 2 Direction Control Register	0000h
DP3 b	FFC6h	E3h	Port 3 Direction Control Register	0000h
DP4 b	FF0Ah	85h	Port 4 Direction Control Register (2 bits)	0000h
DPP0	FE00h	00h	CPU Data Page Pointer 0 Register (4 bits)	0000h
DPP1	FE02h	01h	CPU Data Page Pointer 1 Register (4 bits)	0001h
DPP2	FE04h	02h	CPU Data Page Pointer 2 Register (4 bits)	0002h
DPP3	FE06h	03h	CPU Data Page Pointer 3 Register (4 bits)	0003h
MDC b	FF0Eh	87h	CPU Multiply Divide Control Register	0000h
MDH	FE0Ch	06h	CPU Multiply Divide Register – High Word	0000h
MDL	FE0Eh	07h	CPU Multiply Divide Register – Low Word	0000h
ONES	FF1Eh	8Fh	Constand Value 1's Register (read only)	FFFFh
P0 b	FF00h	80h	Port 0 Register	0000h

Special Function Register Overview (Cont'd)

Name	Physical Address	8-Bit Address	Description	Reset Value
P1 b	FF04h	82h	Port 1 Register	0000h
P2 b	FFC0h	E0h	Port 2 Register	0000h
P3 b	FFC4h	E2h	Port 3 Register	0000h
P4 b	FF08h	84h	Port 4 Register (2 bits)	0000h
P5 b	FFA2h	D1h	Port 5 Register (10 bits, read only)	XXXXh
PECC0	FEC0h	60h	PEC Channel 0 Control Register	0000h
PECC1	FEC2h	61h	PEC Channel 1 Control Register	0000h
PECC2	FEC4h	62h	PEC Channel 2 Control Register	0000h
PECC3	FEC6h	63h	PEC Channel 3 Control Register	0000h
PECC4	FEC8h	64h	PEC Channel 4 Control Register	0000h
PECC5	FECAh	65h	PECChannel 5 Control Register	0000h
PECC6	FECCh	66h	PEC Channel 6 Control Register	0000h
PECC7	FECEh	67h	PEC Channel 7 Control Register	0000h
PSW b	FF10h	88h	CPU Program Status Word	0000h
S0BG	FEB4h	5Ah	Serial Channel 0 Baud Rate Generator Reload Register	0000h
S0CON b	FFB0h	D8h	Serial Channel 0 Control Register	0000h
S0EIC b	FF70h	B8h	Serial Channel 0 Error Interrupt Control Register	0000h
S0RBUF	FEB2h	59	Serial Channel 0 Receive Buffer Register (read only)	XXXXh
S0RIC b	FF6Eh	B7h	Serial Channel 0 Receive Interrupt Control Register	0000h
S0TBUF	FEB0h	58h	Serial Channel 0 Transmit Buffer Register (write only)	0000h
S0TIC b	FF6Ch	B6h	Serial Channel 0 Transmit Interrupt Control Register	0000h
S1BG	FEBCh	5Eh	Serial Channel 1 Baud Rate Generator Reload Register	0000h
S1CON b	FFB8h	DCh	Serial Channel 1 Control Register	0000h
S1EIC b	FF76h	BBh	Serial Channel 1 Error Interrupt Control Register	0000h
S1RBUF	FEBAh	5Dh	Serial Channel 1 Receive Buffer Register (read only)	XXXXh
S1RIC b	FF74h	BAh	Serial Channel 1 Receive Interrupt Control Register	0000h
S1TBUF	FEB8h	5Ch	Serial Channel 1 Transmit Buffer Register (write only)	0000h
S1TIC b	FF72h	B9h	Serial Channel 1 Transmit Interrupt Control Register	0000h
SP	FE12h	09h	CPU System Stack Pointer Register	FC00h
STKOV	FE14h	0Ah	CPU Stack Overflow Pointer Register	FA00h
STKUN	FE16h	0Bh	CPU Stack Underflow Pointer Register	FC00h
SYSCON b	FF0Ch	86h	CPU System Configuration Register	0XX0h*)
T0	FE50h	28h	CAPCOM Timer 0 Register	0000h
T01CON b	FF50h	A8h	CAPCOM Timer 0 and Timer 1 Control Register	0000h

Special Function Register Overview (Cont'd)

Name	Physical Address	8-Bit Address	Description	Reset Value
T0IC b	FF9Ch	CEh	CAPCOM Timer 0 Interrupt Control Register	0000h
T0REL	FE54h	2Ah	CAPCOM Timer 0 Reload Register	0000h
T1	FE52h	29h	CAPCOM Timer 1 Register	0000h
T1IC b	FF9Eh	CFh	CAPCOM Timer 1 Interrupt Control Register	0000h
T1REL	FE56h	2Bh	CAPCOM Timer 1 Reload Register	0000h
T2	FE40h	20h	GPT1 Timer 2 Register	0000h
T2CON b	FF40h	A0h	GPT1 Timer 2 Control Register	0000h
T2IC b	FF60h	B0h	GPT1 Timer 2 Interrupt Control Register	0000h
T3	FE42h	21h	GPT1 Timer 3 Register	0000h
T3CON b	FF42h	A1h	GPT1 Timer 3 Control Register	0000h
T3IC b	FF62h	B1h	GPT1 Timer 3 Interrupt Control Register	0000h
T4	FE44h	22h	GPT1 Timer 4 Register	0000h
T4CON b	FF44h	A2h	GPT1 Timer 4 Control Register	0000h
T4IC b	FF64h	B2h	GPT1 Timer 4 Interrupt Control Register	0000h
T5	FE46h	23h	GPT2 Timer 5 Register	0000h
T5CON b	FF46h	A3h	GPT2 Timer 5 Control Register	0000h
T5IC b	FF66h	B3h	GPT2 Timer 5 Interrupt Control Register	0000h
T6	FE48h	24h	GPT2 Timer 6 Register	0000h
T6CON b	FF48h	A4h	GPT2 Timer 6 Control Register	0000h
T6IC b	FF68h	B4h	GPT2 Timer 6 Interrupt Control Register	0000h
TFR b	FFACh	D6h	Trap Flag Register	0000h
WDT	FEAEh	57h	Watchdog Timer Register (read only)	0000h
WDTCON	FFAEh	D7h	Watchdog Timer Control Register	0000h
ZEROS b	FF1Ch	8Eh	Constant Value 0's Register (read only)	0000h

*) The system configuration is selected during reset.

18 ELECTRICAL CHARACTERISTICS

18.1 Absolute Maximum Ratings

Ambient temperature under bias (T_A): . . . . . 0 to +70 °C
Storage temperature (T_{ST}) . . . . . – 65 to +125 °C
Voltage on V_{CC} pins with respect to ground (V_{SS}). . . . . –0.5 to +6.5 V
Voltage on any pin with respect to ground (V_{SS}) . . . . . –0.3 to V_{CC} +0.3 V
Input current on any pin during overload condition . . . . . -10 to +10 mA.
Absolute sum of all input currents during overload condition . . . . . .100 mA.
Power dissipation . . . . . .1.5 W
Flash programming voltage (V_{PP}). . . . . – 0.3 to + 13.5 V

Note: Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. During overload conditions (V_{IN}>V_{CC} or V_{IN}<V_{SS}) the voltage on pins with respect to ground (V_{SS}) must not exceed the values defined by the Absolute Maximum Ratings.

18.2 Parameter Interpretation

The parameters listed in the following partly represent the characteristics of the ST10R165 and partly its demands on the system. To aid in interpreting the parameters right, when evaluating them for a design, they are marked in column “Symbol”:

CC (**C**ontroller **C**haracteristics):
The logic of the ST10R165 will provide signals with the respective timing characteristics.

SR (**S**ystem **R**equirement):
The external system must provide signals with the respective timing characteristics to the ST10R165.

18.3 DC Characteristics

V_{CC} = 5 V ± 10 %; V_{SS} = 0 V; f_{CPU} = 20 MHz
T_A = 0 to +70 °C for ST10F166/166-16

Parameter	Symbol	Limit Values		Unit	Test Condition
		min.	max.		
Input low voltage EBC1/V_{PP}	V_{IL1} SR	– 0.3	0.2 V_{CC} – 0.1	V	–
Input low voltage (all except EBC1/V_{PP})	V_{IL2} SR	– 0.5	0.2 V_{CC} – 0.1	V	–
Input high voltage (all except $\overline{RSTIN}$ and XTAL1)	V_{IH} SR	0.2 V_{CC} + 0.9	V_{CC} + 0.5	V	–
Input high voltage $\overline{RSTIN}$	V_{IH1} SR	0.6 V_{CC}	V_{CC} + 0.5	V	–
Input high voltage XTAL1	V_{IH2} SR	0.7 V_{CC}	V_{CC} + 0.5	V	–
Output low voltage (Port 0, Port 1, Port 4, ALE, $\overline{RD}$, $\overline{WR}$, $\overline{BHE}$, CLKOUT, $\overline{RSTOUT}$)	V_{OL} CC	–	0.45	V	I_{OL} = 2.4 mA
Output low voltage (all other outputs)	V_{OL1} CC	–	0.45	V	I_{OL1} = 1.6 mA
Output high voltage (Port 0, Port 1, Port 4, ALE, $\overline{RD}$, $\overline{WR}$, $\overline{BHE}$, CLKOUT, $\overline{RSTOUT}$)	V_{OH} CC	0.9 V_{CC} 2.4	–	V V	I_{OH} = – 500 µA I_{OH} = – 2.4 mA
Output high voltage (all other outputs)	V_{OH1} CC	0.9 V_{CC} 2.4	–	V V	I_{OH} = – 250 µA I_{OH} = – 1.6 mA
Input leakage current (Port 5) [1]	I_{OZ1} CC	–	±500[8]	nA	0 V < V_{IN} < V_{CC}
Input leakage current (all other)	I_{OZ2} CC	–	±1[8]	µA	0 V < V_{IN} < V_{CC}
V_{PP} leakage current EBC1/V_{PP}	I_{PPS} CC	–	±100	µA	0 ≤ V_{PP} ≤ V_{CC}
$\overline{RSTIN}$ pullup resistor [6]	R_{RST} CC	50	150	kΩ	–
Read inactive current [5]	I_{RH} [3]	–	-40	µA	V_{OUT} = V_{OHmin}
Read active current [5]	I_{RL} [4]	-500	–	µA	V_{OUT} = V_{OLmax}
ALE inactive current [5]	I_{ALEL} [3]	–	150	µA	V_{OUT} = V_{OLmax}
ALE active current [5]	I_{ALEH} [4]	2100	–	µA	V_{OUT} = V_{OHmin}
XTAL1 input current	I_{IL} CC	–	±20	µA	0 V < V_{IN} < V_{CC}

DC Characteristics (Cont'd)

Parameter	Symbol	Limit Values		Unit	Test Condition
		min.	max.		
Pin capacitance [6] (digital inputs/outputs)	C_{IO} CC	–	10	pF	f = 1 MHz T_A = 25 °C
Power supply current	I_{CC}	–	80 + 5 * f_{CPU}	mA	$\overline{RSTIN}$ = V_{IL2} f_{CPU} in [MHz] [7]
Idle mode supply current	I_{ID}	–	35 + 1.5 * f_{CPU}	mA	$\overline{RSTIN}$ = V_{IH1} f_{CPU} in [MHz] [7]
Power-down mode supply current	I_{PD}	TBD	TBD	µA	–
V_{PP} read current [6]	I_{PPR}	–	200	µA	V_{PP} > V_{CC}
V_{PP} write current [6]	I_{PPW}	–	50	mA	1/TCL = 40 MHz 32-bit program-ming V_{PP} = 12 V
V_{PP} during write/read	V_{PP}	11.4	12.6	V	

Notes:

1) This specification does not apply to the analog input (Port 5.x) which is currently converted.

3) The maximum current may be drawn while the respective signal line remains inactive.

4) The minimum current must be drawn in order to drive the respective signal line active.

5) This specification is only valid during Reset, or during Hold-mode.

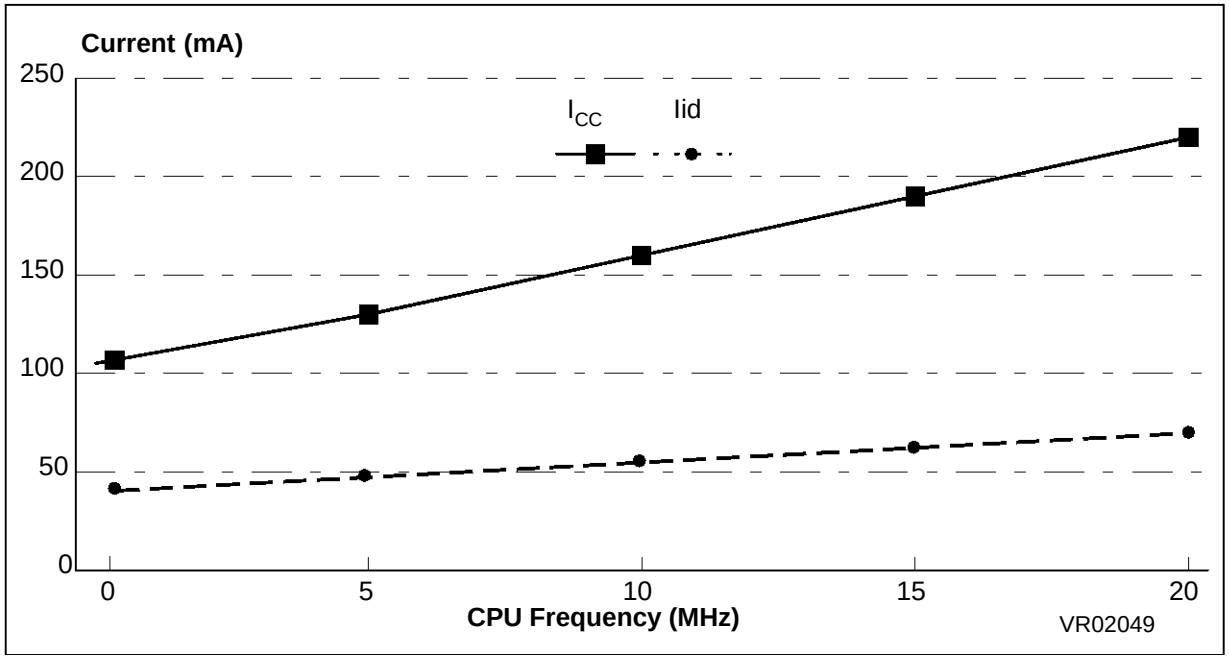
6) Not 100% tested, guaranteed by design characterization.

7) The supply current is a function of the operating frequency. This dependency is illustrated in the figure below.
These parameters are tested at V_{CCmax} and 20 MHz CPU clock with all outputs disconnected and all inputs at V_{IL} or V_{IH}.

8) This value is guaranteed also after ESD qualification trials at 25 degrees

DC Characteristics (Cont'd)

Figure 10. Supply/Idle Current as a Function of Operating Frequency



18.4 A/D Converter Characteristics

V_{CC} = 5 V ± 10 %; V_{SS} = 0 V
T_A = 0 to +70 °C for ST10F166/166-16
4.0 V ≤ V_{AREF} ≤ V_{CC}+0.1 V; V_{SS}-0.1 V ≤ V_{AGND} ≤ V_{SS}+0.2 V

Parameter	Symbol		Limit Values		Unit	Test Condition
			min.	max.		
Analog input voltage range	V_{AIN}	SR	V_{AGND}	V_{AREF}	V	1)
Sample time	t_S	CC	–	2 t_{SC}		2) 4)
Conversion time	t_C	CC	–	10 t_{CC} + t_S + 4TCL		3) 4)
Total unadjusted error	TUE	CC	–	± 3	LSB	5)
Internal resistance of reference voltage source 7)	R_{AREF}	CC	–	t_{CC} / 250 - 0.25	kΩ	t_{CC} in [ns] 6) 7)
Internal resistance of analog source 7)	R_{ASRC}	CC	–	t_S / 500 - 0.25	kΩ	t_S in [ns] 2) 7)
ADC input capacitance 7)	C_{AIN}	CC	–	50	pF	7)
V_{AREF} Supply Current	I_{REF}		–	5	mA	

Notes:

1) V_{AIN} may exceed V_{AGND} or V_{AREF} up to the absolute maximum ratings. However, the conversion result in these cases will be $X000_H$ or $X3FF_H$, respectively.

2) During the sample time the input capacitance C_I can be charged/discharged by the external source. The internal resistance of the analog source must allow the capacitors to reach their final voltage level within t_S. After the end of the sample time t_S, changes of the analog input voltage have no effect on the conversion result.
The value for the sample clock is t_{SC} = TCL * 32.

3) This parameter includes the sample time t_S, the time for determining the digital result and the time to load the result register with the conversion result.
The value for the conversion clock is t_{CC} = TCL * 32.

4) This parameter depends on the ADC control logic. It is not a real maximum value, but rather a fixum.

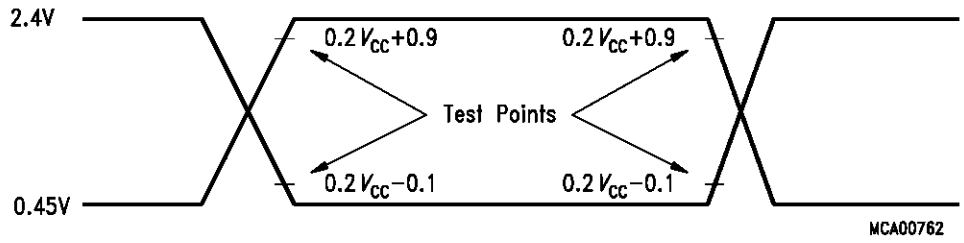
5) TUE is tested at V_{AREF}=5.0V, V_{AGND}=0V, V_{CC}=4.8V. It is guaranteed by design characterization for all other voltages within the defined voltage range.

6) During the conversion the ADC's capacitance must be repeatedly charged or discharged. The internal resistance of the reference voltage source must allow the capacitors to reach their respective voltage level within t_{CC}. The maximum internal resistance results from the CPU clock period.

7) Not 100% tested, guaranteed by design characterization.

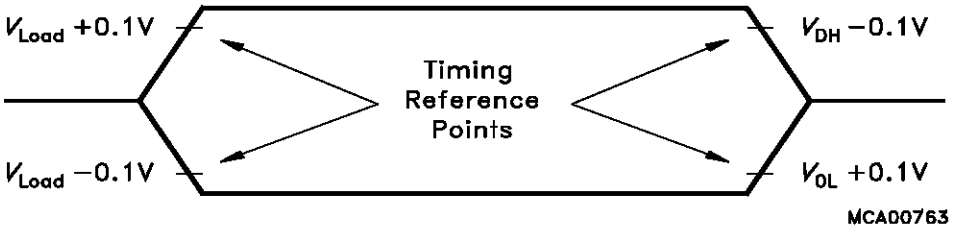
18.5 Testing Waveforms

Figure 11. Input Output Waveforms



AC inputs during testing are driven at 2.4 V for a logic '1' and 0.4 V for a logic '0'. Timing measurements are made at V_{IH} min for a logic '1' and V_{IL} max for a logic '0'.

Figure 12. Float Waveforms



For timing purposes a port pin is no longer floating when a 100 mV change from load voltage occurs, but begins to float when a 100 mV change from the loaded V_{OH}/V_{OL} level occurs (I_{OH}/I_{OL} = 20 mA).

18.6 Memory Cycle Variables

The timing tables below use three variables which are derived from registers SYSCON and BUSCON1 and represent the special characteristics of the programmed memory cycle. The following table describes, how these variables are to be computed.

Description	Symbol	Values
ALE Extension	t_A	TCL * <ALECTL>
Memory Cycle Time Waitstates	t_C	2TCL * (15 - <MCTC>)
Memory Tristate Time	t_F	2TCL * (1 - <MTTC>)

18.7 AC Characteristics

The specification of the timings depends on the CPU clock signal that is used in the respective device. In this regard the specification for the ST10F166 and the ST10F166-16 are different. While the ST10F166-16 directly uses the clock signal fed to XTAL1 and therefore has to take into account the duty cycle variation of this signal, the ST10F166 derives its CPU clock from the XTAL1 signal via a 2:1 prescaler and therefore is independant from these variations.

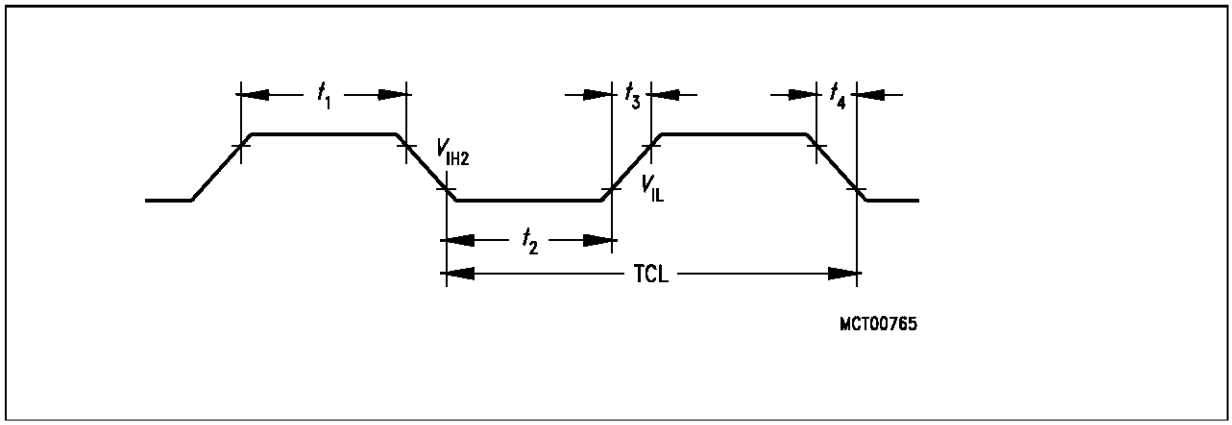
For these reasons the following pages provide the timing specifications for ST10F166 and for ST10F166-16 separately (where applicable).

External Clock Drive XTAL1 for the ST10F166

V_{CC} = 5 V ± 10 %; V_{SS} = 0 V
T_A = 0 to +70 °C

Parameter	Symbol		Max. CPU Clock = 20 MHz		Variable CPU Clock 1/2TCL = 1 to 20 MHz		Unit
			min.	max.	min.	max.	
Oscillator period	TCL	SR	25	25	25	500	ns
High time	t_1	SR	6	–	6	–	ns
Low time	t_2	SR	6	–	6	–	ns
Rise time	t_3	SR	–	5	–	5	ns
Fall time	t_4	SR	–	5	–	5	ns

Figure 13. External Clock Drive XTAL1



AC Characteristics (Cont'd)

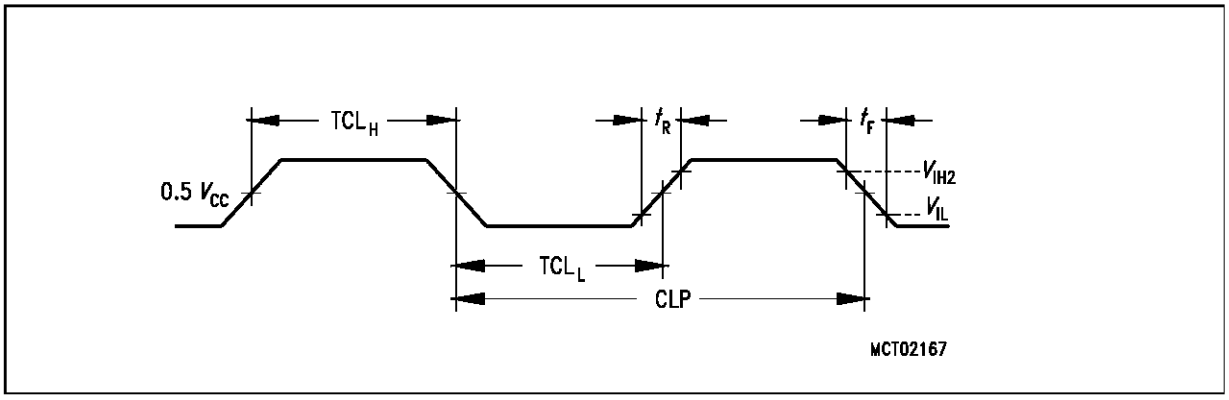
External Clock Drive XTAL1 for the ST10F166-16

V_{CC} = 5 V ± 10 %;V_{SS} = 0 V
T_A = 0 to +70 °C

Parameter	Symbol		CPU Clock = 16 MHz Duty cycle 0.4 to 0.6		Variable CPU Clock 1/CLP = 1 to 20 MHz		Unit
			min.	max.	min.	max.	
Oscillator period	CLP	SR	62.5	62.5	50	1000	ns
High time	TCL_H	SR	25	–	25	CLP-TCL_L	ns
Low time	TCL_L	SR	25	–	25	CLP-TCL_H	ns
Rise time	t_R	SR	–	10	–	10	ns
Fall time	t_F	SR	–	10	–	10	ns
Oscillator duty cycle	DC	SR	0.4	0.6	25 / CLP	1 - 25 / CLP	
Clock cycle	TCL	SR	25	37.5	CLP * DC_{min}	CLP * DC_{max}	ns

Note: In order to run the ST10F166-16 at a CPU clock of 20 MHz the duty cycle of the oscillator clock must be 0.5, ie. the relation between the oscillator high and low phases must be 1:1. So the variation of the duty cycle of the oscillator clock limits the maximum operating speed of the device.
The 16 MHz values in the tables are given as an example for a typical duty cycle variation of the oscillator clock from 0.4 to 0.6.

Figure 14. External Clock Drive XTAL1



AC Characteristics (Cont'd)

Multiplexed Bus for the ST10F166

V_{CC} = 5 V ± 10 %;V_{SS} = 0 V
T_A = 0 to +70 °C

C_L (for Port 0, Port 1, Port 4, ALE, $\overline{RD}$, $\overline{WR}$, $\overline{BHE}$, CLKOUT) = 100 pF
ALE cycle time = 6 TCL + 2t_A + t_C + t_F (150 ns at 20-MHz CPU clock without waitstates)

Parameter	Symbol		Max. CPU Clock = 20 MHz		Variable CPU Clock 1/2TCL = 1 to 20 MHz		Unit
			min.	max.	min.	max.	
ALE high time	t_5	CC	15 + t_A	–	TCL - 10 + t_A	–	ns
Address setup to ALE	t6	CC	10 + t_A	–	TCL - 15 + t_A	–	ns
Address hold after ALE	t7	CC	15 + t_A	–	TCL - 10 + t_A	–	ns
ALE falling edge to $\overline{RD}$, $\overline{WR}$ (with RW-delay)	t8	CC	15 + t_A	–	TCL - 10 + t_A	–	ns
ALE falling edge to $\overline{RD}$, $\overline{WR}$ (no RW-delay)	t9	CC	-10 + t_A	–	-10 + t_A	–	ns
Address float after $\overline{RD}$, $\overline{WR}$ (with RW-delay)	t10	CC	–	5	–	5	ns
Address float after $\overline{RD}$, $\overline{WR}$ (no RW-delay)	t11	CC	–	30	–	TCL + 5	ns
$\overline{RD}$, $\overline{WR}$ low time (with RW-delay)	t_{12}	CC	40 + t_C	–	2TCL - 10 + t_C	–	ns
$\overline{RD}$ $\overline{WR}$ low time (no RW-delay)	t_{13}	CC	65 + t_C	–	3TCL - 10 + t_C	–	ns
$\overline{RD}$ to valid data in (with RW-delay)	t_{14}	SR	–	30 + t_C	–	2TCL - 20 + t_C	ns
$\overline{RD}$ to valid data in (no RW-delay)	t_{15}	SR	–	55 + t_C	–	3TCL - 20 + t_C	ns
ALE low to valid data in	t_{16}	SR	–	55 + t_A + t_C	–	3TCL - 20 + t_A + t_C	ns
Address to valid data in	t_{17}	SR	–	75 + 2t_A + t_C	–	4TCL - 25 + 2t_A + t_C	ns
Data hold after $\overline{RD}$ rising edge	t_{18}	SR	0	–	0	–	ns
Data float after $\overline{RD}$	t_{19}	SR	–	35 + t_F	–	2TCL - 15 + t_F	ns
Data valid to $\overline{WR}$	t_{22}	CC	35 + t_C	–	2TCL - 15 + t_C	–	ns
Data hold after $\overline{WR}$	t_{23}	CC	35 + t_F	–	2TCL - 15 + t_F	–	ns
ALE rising edge after $\overline{RD}$, $\overline{WR}$	t_{25}	CC	35 + t_F	–	2TCL - 15 + t_F	–	ns
Address hold after $\overline{RD}$, $\overline{WR}$	t_{27}	CC	35 + t_F	–	2TCL - 15 + t_F	–	ns

AC Characteristics (Cont'd)

Multiplexed Bus for the ST10F166-16

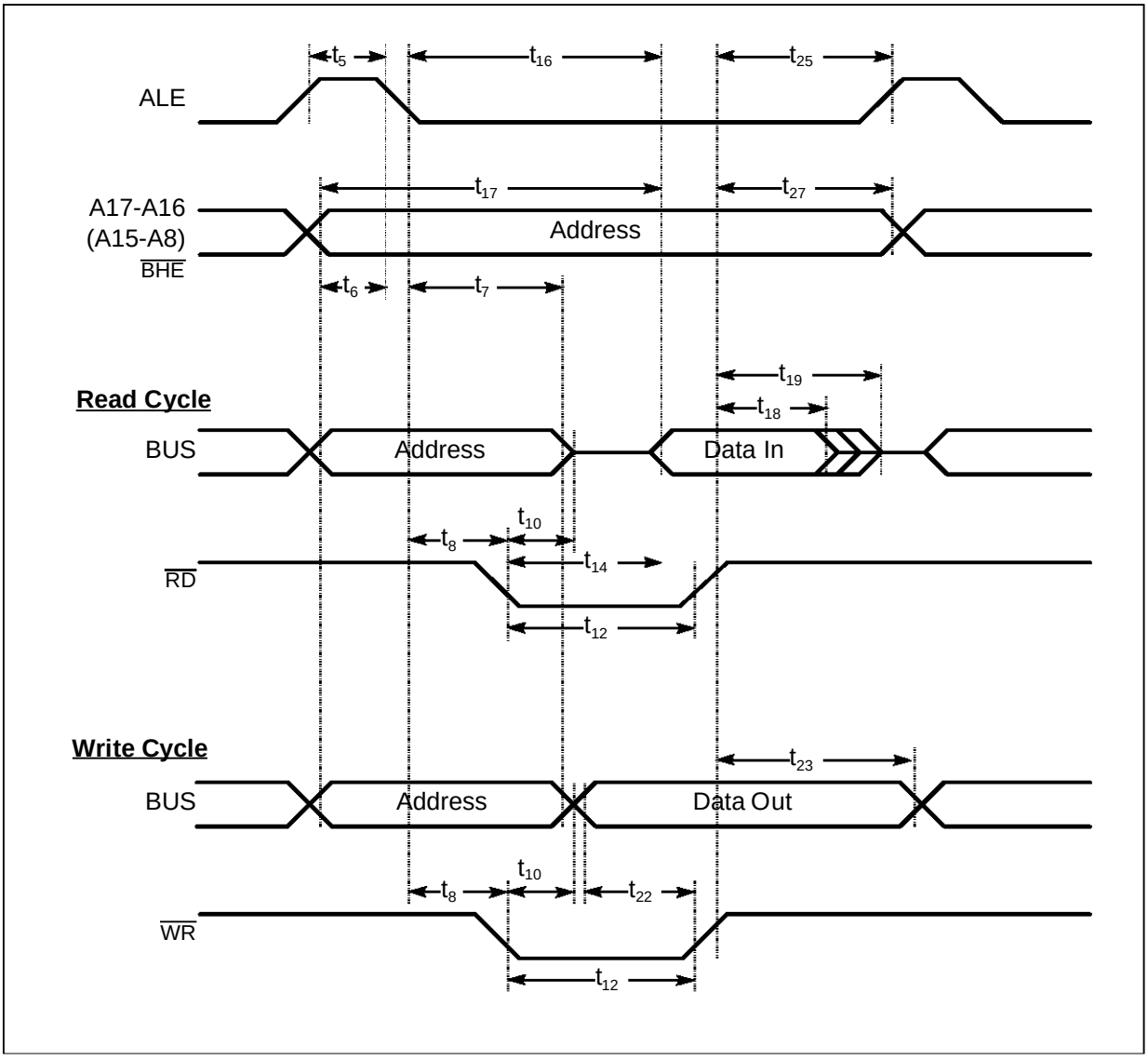
V_{CC} = 5 V ± 10 %; V_{SS} = 0 V T_A = 0 to +70 °C

C_L (for Port 0, Port 1, Port 4, ALE, $\overline{RD}$, $\overline{WR}$, $\overline{BHE}$, CLKOUT) = 100 pF
ALE cycle time = 6 TCL + $2t_A$ + t_C + t_F (150 ns at 20-MHz CPU clock without wait-states)

Parameter	Symbol	CPU Clock = 16 MHz Duty cycle 0.4 to 0.6		Variable CPU Clock 1/CLP = 1 to 20 MHz		Unit
		min.	max.	min.	max.	
ALE high time	t_5 CC	15 + t_A	–	TCL_{min} - 10 + t_A	–	ns
Address setup to ALE	t6 CC	10 + t_A	–	TCL_{min} - 15 + t_A	–	ns
Address hold after ALE	t7 CC	15 + t_A	–	TCL_{min} - 10 + t_A	–	ns
ALE falling edge to $\overline{RD}$, $\overline{WR}$ (with RW-delay)	t8 CC	15 + t_A	–	TCL_{min} - 10 + t_A	–	ns
ALE falling edge to $\overline{RD}$, $\overline{WR}$ (no RW-delay)	t9 CC	-10 + t_A	–	-10 + t_A	–	ns
Address float after $\overline{RD}$, $\overline{WR}$ (with RW-delay)	t10 CC	–	5	–	5	ns
Address float after $\overline{RD}$, $\overline{WR}$ (no RW-delay)	t11 CC	–	42.5	–	TCL_{max} + 5	ns
$\overline{RD}$, $\overline{WR}$ low time (with RW-delay)	t_{12} CC	52.5 + t_C	–	CLP - 10 + t_C	–	ns
$\overline{RD}$ $\overline{WR}$ low time (no RW-delay)	t_{13} CC	77.5 + t_C	–	CLP+TCL_{min} - 10 + t_C	–	ns
$\overline{RD}$ to valid data in (with RW-delay)	t_{14} SR	–	47.5 + t_C	–	CLP - 20 + t_C	ns
$\overline{RD}$ to valid data in (no RW-delay)	t_{15} SR	–	72.5 + t_C	–	CLP+TCL_{min} - 20 + t_C	ns
ALE low to valid data in	t_{16} SR	–	72.5 + t_A + t_C	–	CLP+TCL_{min} - 20 + t_C	ns
Address to valid data in	t_{17} SR	–	100 + $2t_A$ + t_C	–	2CLP - 25 + $2t_A$ + t_C	ns
Data hold after $\overline{RD}$ rising edge	t_{18} SR	0	–	0	–	ns
Data float after $\overline{RD}$	t_{19} SR	–	47.5 + t_F	–	CLP - 15 + t_F	ns
Data valid to $\overline{WR}$	t_{22} CC	47.5 + t_C	–	CLP - 15 + t_C	–	ns
Data hold after $\overline{WR}$	t_{23} CC	47.5 + t_F	–	CLP - 15 + t_F	–	ns
ALE rising edge after $\overline{RD}$, $\overline{WR}$	t_{25} CC	47.5 + t_F	–	CLP - 15 + t_F	–	ns
Address hold after $\overline{RD}$, $\overline{WR}$	t_{27} CC	47.5 + t_F	–	CLP - 15 + t_F	–	ns

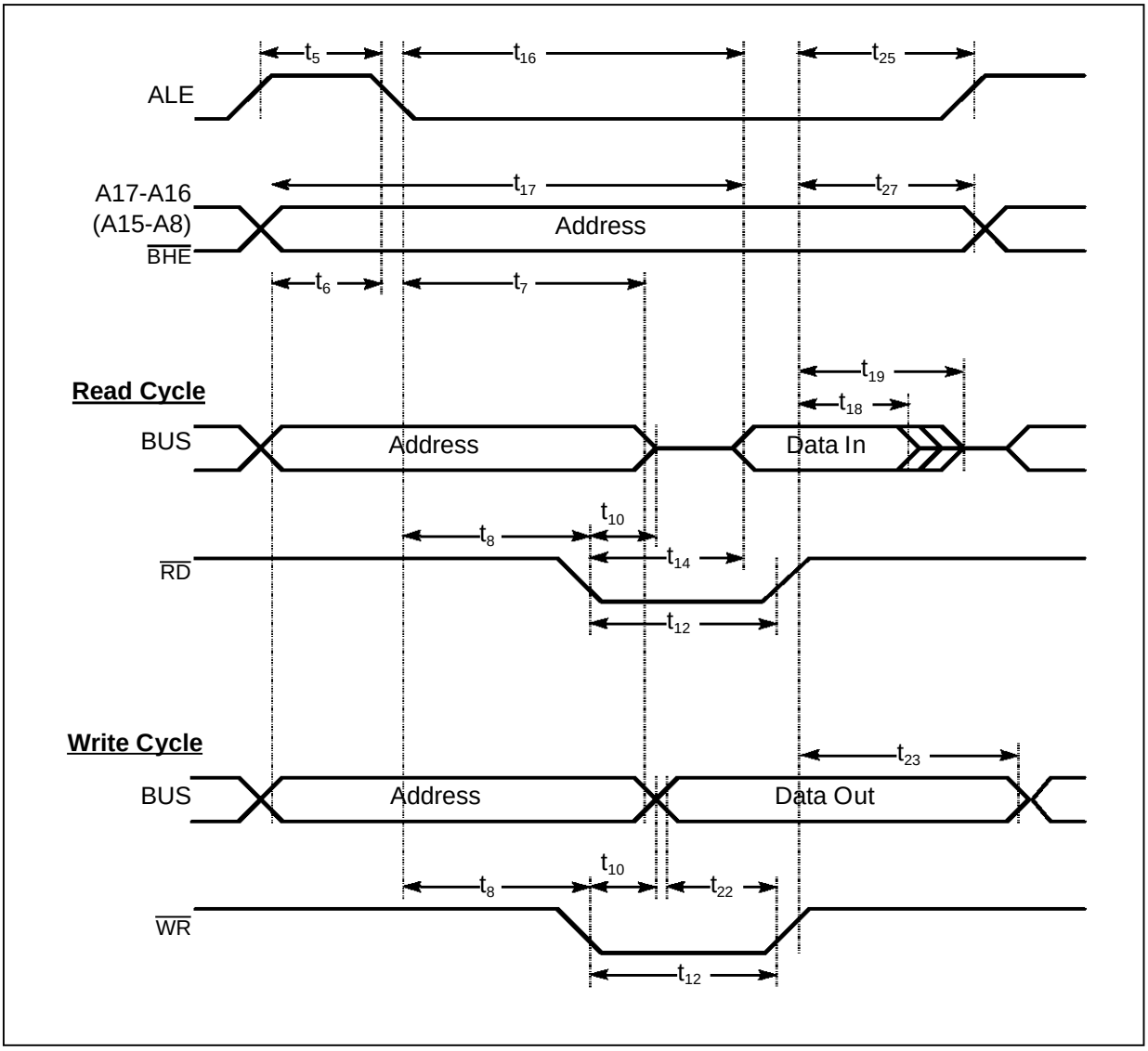
AC Characteristics (Cont'd)

Figure 15. External Memory Cycle: Multiplexed Bus, With Read/Write Delay, Normal ALE



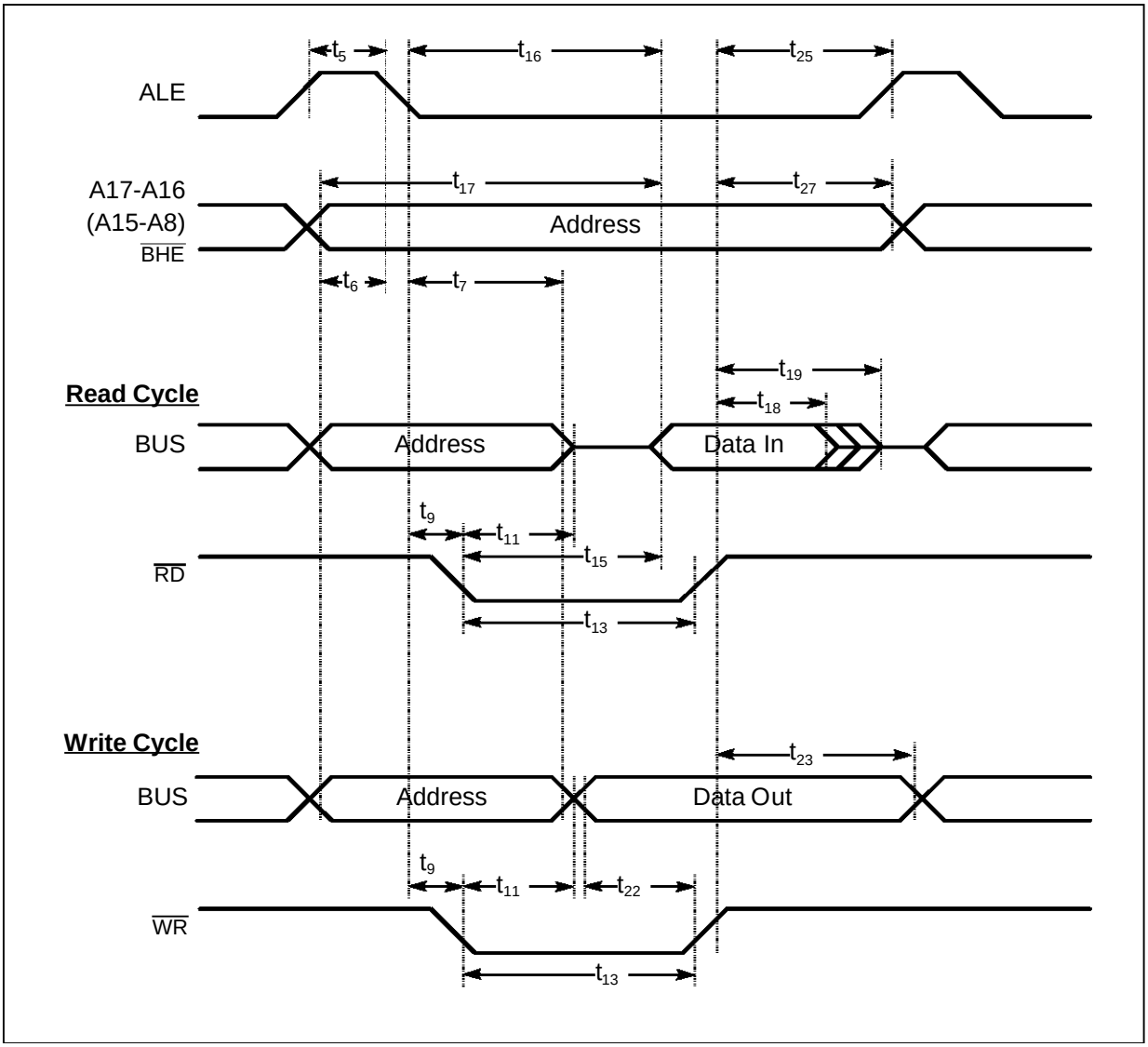
AC Characteristics (Cont'd)

Figure 16. Ext. Memory Cycle: Multiplexed Bus, With Read/Write Delay, Extended ALE



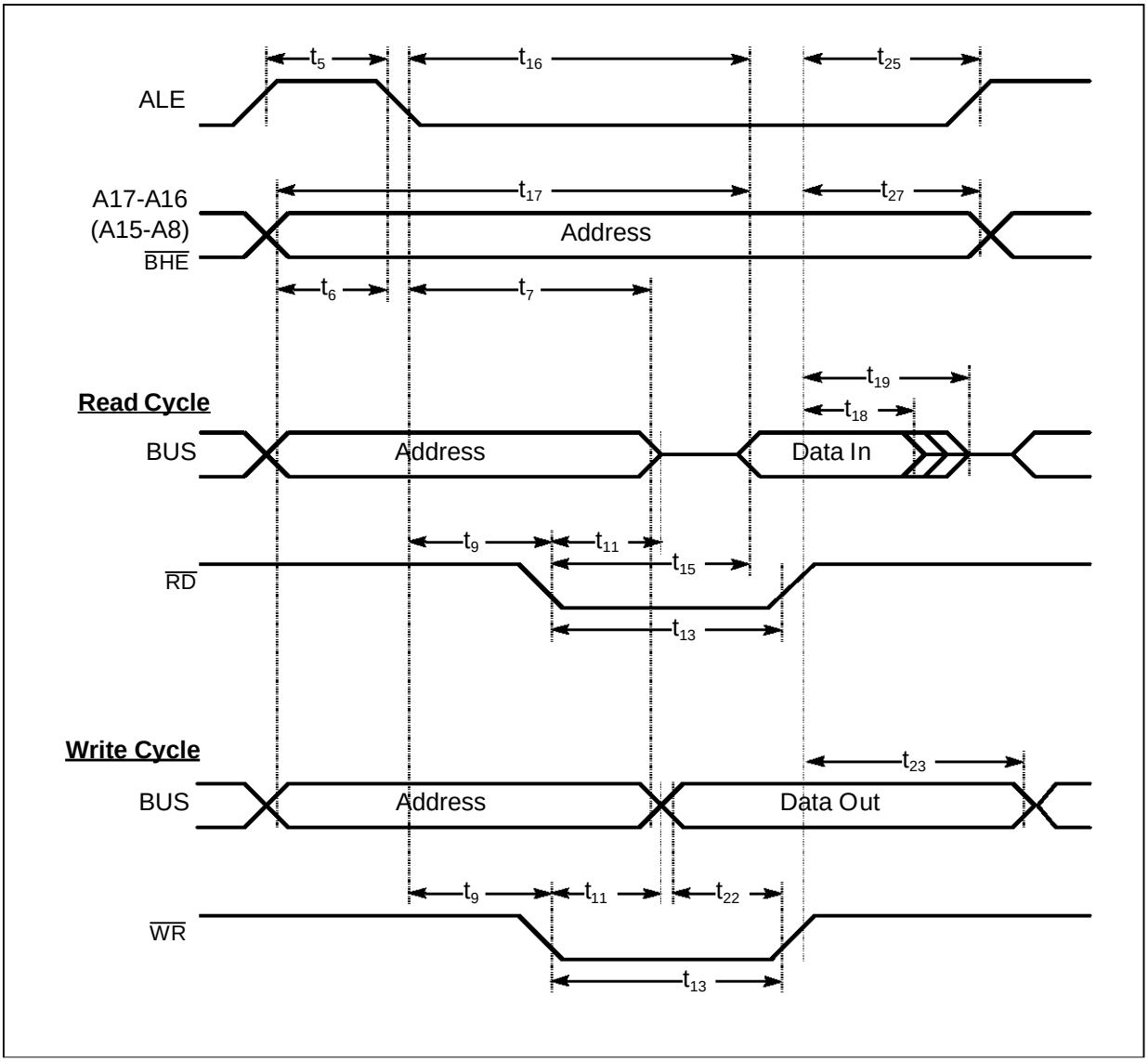
AC Characteristics (Cont'd)

Figure 17. External Memory Cycle: Multiplexed Bus, No Read/Write Delay, Normal ALE



AC Characteristics (Cont'd)

Figure 18. Ext. Memory Cycle: Multiplexed Bus, No Read/Write Delay, Extended ALE



AC Characteristics (Cont'd)

Demultiplexed Bus for the ST10F166

V_{CC} = 5 V ± 10 %; V_{SS} = 0 V
T_A = 0 to +70 °C
C_L (for Port 0, Port 1, Port 4, ALE, $\overline{RD}$, $\overline{WR}$, $\overline{BHE}$, CLKOUT) = 100 pF
ALE cycle time = 4 TCL + $2t_A$ + t_C + t_F (100 ns at 20-MHz CPU clock without wait-states)

Parameter	Symbol	Max. CPU Clock = 20 MHz		Variable CPU Clock 1/2TCL = 1 to 20 MHz		Unit
		min.	max.	min.	max.	
ALE high time	t_5 CC	15 + t_A	–	TCL - 10 + t_A	–	ns
Address setup to ALE	t6 CC	10 + t_A	–	TCL - 15 + t_A	–	ns
ALE falling edge to $\overline{RD}$, $\overline{WR}$ (with RW-delay)	t8 CC	15 + t_A	–	TCL - 10 + t_A	–	ns
ALE falling edge to $\overline{RD}$, $\overline{WR}$ (no RW-delay)	t9 CC	-10 + t_A	–	-10 + t_A	–	ns
$\overline{RD}$, $\overline{WR}$ low time (with RW-delay)	t_{12} CC	40 + t_C	–	2TCL - 10 + t_C	–	ns
$\overline{RD}$, $\overline{WR}$ low time (no RW-delay)	t_{13} CC	65 + t_C	–	3TCL - 10 + t_C	–	ns
$\overline{RD}$ to valid data in (with RW-delay)	t_{14} SR	–	30 + t_C	–	2TCL - 20 + t_C	ns
$\overline{RD}$ to valid data in (no RW-delay)	t_{15} SR	–	55 + t_C	–	3TCL - 20 + t_C	ns
ALE low to valid data in	t_{16} SR	–	55 + t_A + t_C	–	3TCL - 20 + t_A + t_C	ns
Address to valid data in	t_{17} SR	–	75 + $2t_A$ + t_C	–	4TCL - 25 + $2t_A$ + t_C	ns
Data hold after $\overline{RD}$ rising edge	t_{18} SR	0	–	0	–	ns
Data float after $\overline{RD}$ rising edge (with RW-delay)	t_{20} SR	–	35 + t_F	–	2TCL - 15 + t_F	ns
Data float after $\overline{RD}$ rising edge (no RW-delay)	t_{21} SR	–	15 + t_F	–	TCL - 10 + t_F	ns
Data valid to $\overline{WR}$	t_{22} CC	35 + t_C	–	2TCL - 15 + t_C	–	ns
Data hold after $\overline{WR}$	t_{24} CC	15 + t_F	–	TCL - 10 + t_F	–	ns
ALE rising edge after $\overline{RD}$, $\overline{WR}$	t_{26} CC	-10 + t_F	–	-10 + t_F	–	ns
Address hold after $\overline{RD}$, $\overline{WR}$	t_{28} CC	0 + t_F	–	0 + t_F	–	ns

AC Characteristics (Cont'd)

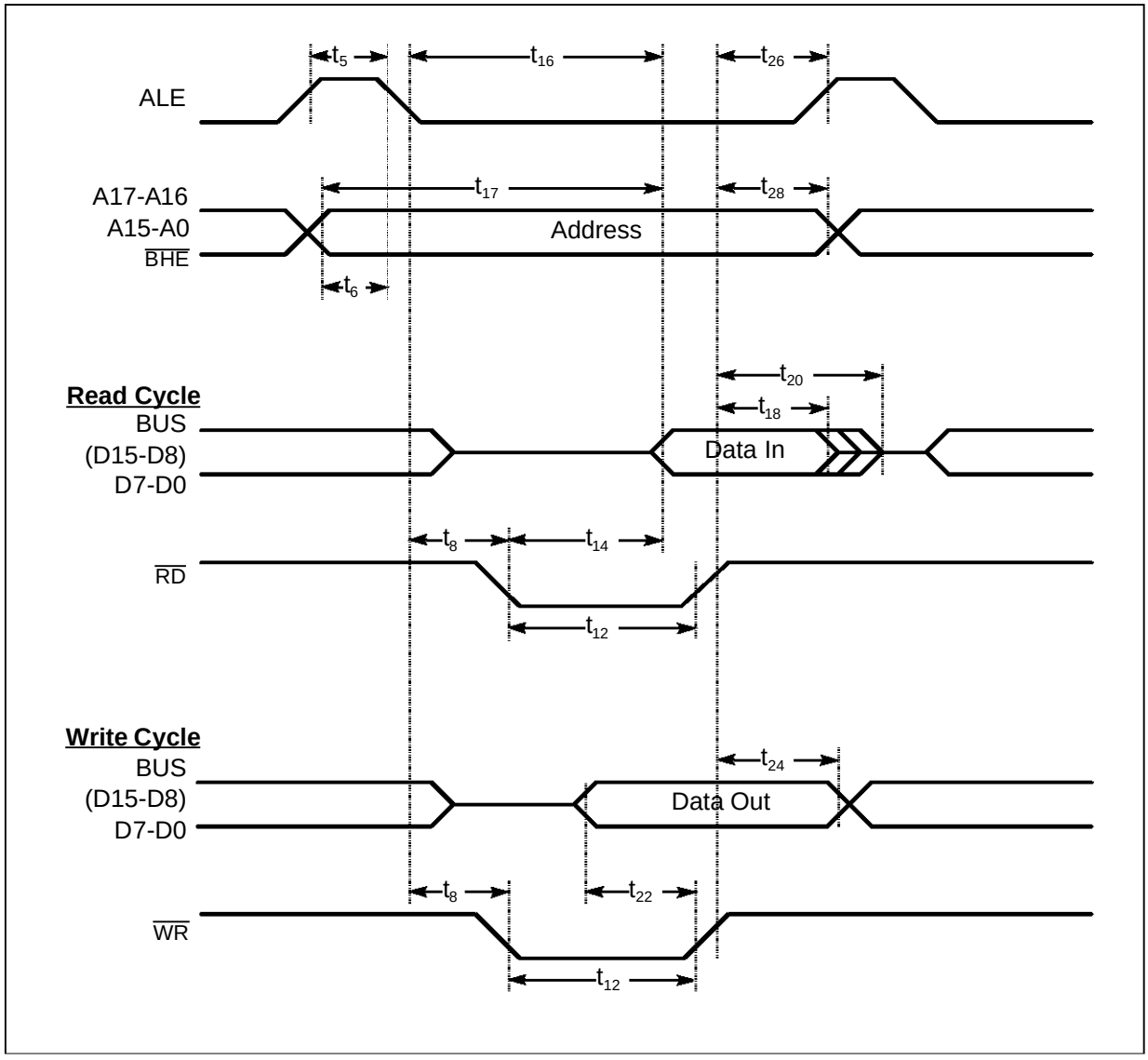
Demultiplexed Bus for the ST10F166-16

V_{CC} = 5 V ± 10 %; V_{SS} = 0 V
T_A = 0 to +70 °C
C_L (for Port 0, Port 1, Port 4, ALE, $\overline{RD}$, $\overline{WR}$, $\overline{BHE}$, CLKOUT) = 100 pF
ALE cycle time = 4 TCL + $2t_A$ + t_C + t_F (100 ns at 20-MHz CPU clock without wait-states)

Parameter	Symbol	CPU Clock = 16 MHz Duty cycle 0.4 to 0.6		Variable CPU Clock 1/CLP = 1 to 20 MHz		Unit
		min.	max.	min.	max.	
ALE high time	t_5 CC	15 + t_A	–	TCL_{min} - 10 + t_A	–	ns
Address setup to ALE	$t6$ CC	10 + t_A	–	TCL_{min} - 15 + t_A	–	ns
ALE falling edge to $\overline{RD}$, $\overline{WR}$ (with RW-delay)	$t8$ CC	15 + t_A	–	TCL_{min} - 10 + t_A	–	ns
ALE falling edge to $\overline{RD}$, $\overline{WR}$ (no RW-delay)	$t9$ CC	-10 + t_A	–	-10 + t_A	–	ns
$\overline{RD}$, $\overline{WR}$ low time (with RW-delay)	t_{12} CC	52.5 + t_C	–	CLP - 10 + t_C	–	ns
$\overline{RD}$, $\overline{WR}$ low time (no RW-delay)	t_{13} CC	77.5 + t_C	–	CLP+TCL_{min} - 10 + t_C	–	ns
$\overline{RD}$ to valid data in (with RW-delay)	t_{14} SR	–	47.5 + t_C	–	CLP - 20 + t_C	ns
$\overline{RD}$ to valid data in (no RW-delay)	t_{15} SR	–	72.5 + t_C	–	CLP+TCL_{min} - 20 + t_C	ns
ALE low to valid data in	t_{16} SR	–	72.5 + t_A + t_C	–	CLP+TCL_{min} - 20 + t_A + t_C	ns
Address to valid data in	t_{17} SR	–	100 + $2t_A$ + t_C	–	2CLP - 25 + $2t_A$ + t_C	ns
Data hold after $\overline{RD}$ rising edge	t_{18} SR	0	–	0	–	ns
Data float after $\overline{RD}$ rising edge (with RW-delay)	t_{20} SR	–	47.5 + t_F	–	CLP - 15 + t_F	ns
Data float after $\overline{RD}$ rising edge (no RW-delay)	t_{21} SR	–	15 + t_F	–	TCL_{min} - 10 + t_F	ns
Data valid to $\overline{WR}$	t_{22} CC	47.5 + t_C	–	CLP - 15 + t_C	–	ns
Data hold after $\overline{WR}$	t_{24} CC	15 + t_F	–	TCL_{min} - 10 + t_F	–	ns
ALE rising edge after $\overline{RD}$, $\overline{WR}$	t_{26} CC	-10 + t_F	–	-10 + t_F	–	ns
Address hold after $\overline{RD}$, $\overline{WR}$	t_{28} CC	0 + t_F	–	0 + t_F	–	ns

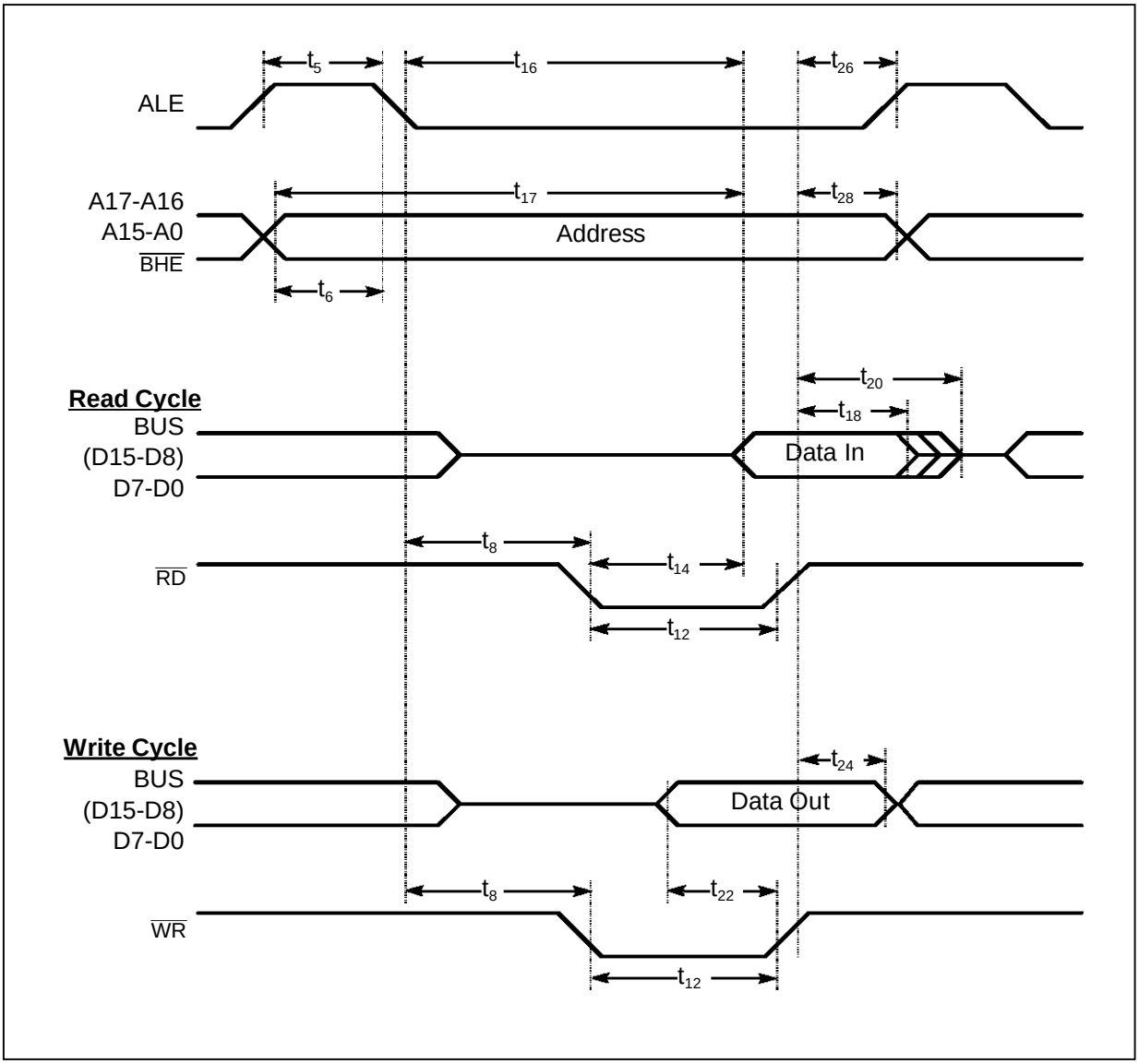
AC Characteristics (Cont'd)

Figure 19. Ext. Memory Cycle: Demultiplexed Bus, With Read/Write Delay, Normal ALE



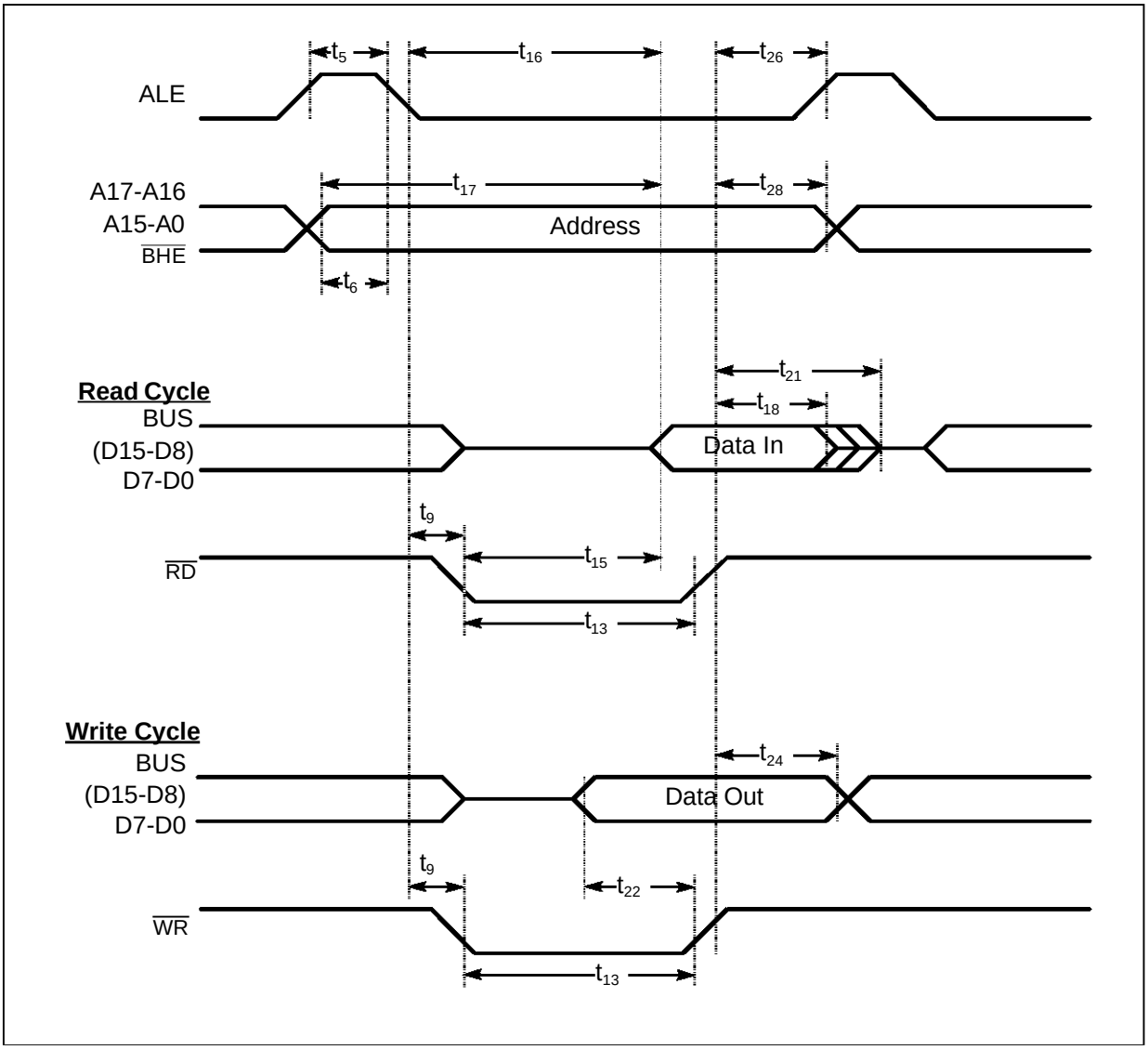
AC Characteristics (Cont'd)

Figure 20. Ext. Mem. Cycle: Demultiplexed Bus, With Read/Write Delay, Extended ALE



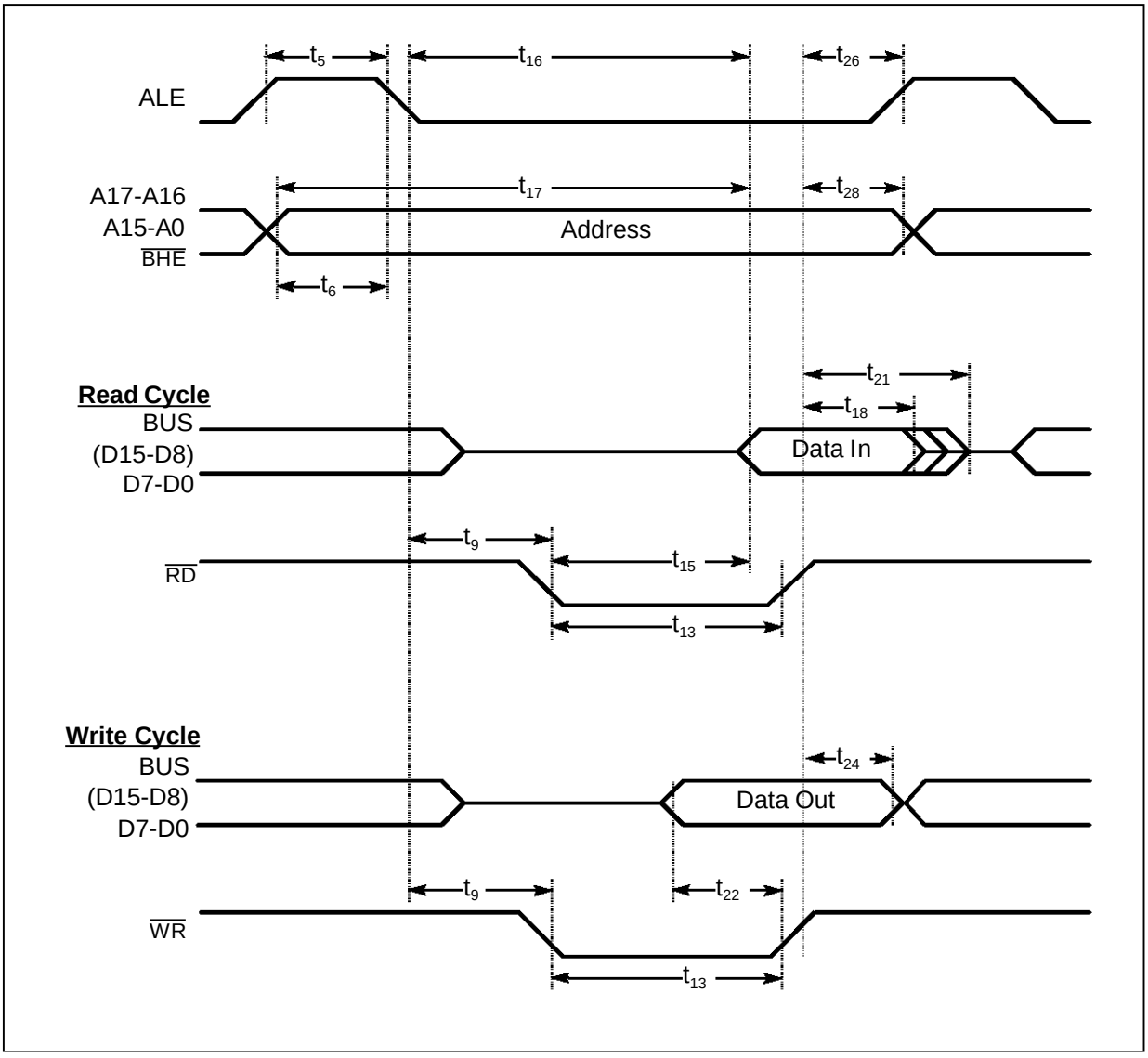
AC Characteristics (Cont'd)

Figure 21. Ext. Memory Cycle: Demultiplexed Bus, No Read/Write Delay, Normal ALE



AC Characteristics (Cont'd)

Figure 22. Ext. Memory Cycle: Demultiplexed Bus, No Read/Write Delay, Extended ALE



AC Characteristics (Cont'd)

CLKOUT and $\overline{\text{READY}}$ for ST10F166,

V_{CC} = 5 V ± 10 %; V_{SS} = 0 V
T_A = 0 to +70 °C
C_L (for Port 0, Port 1, Port 4, ALE, $\overline{\text{RD}}$, $\overline{\text{WR}}$, $\overline{\text{BHE}}$, CLKOUT) = 100 pF

Parameter	Symbol	Max. CPU Clock = 20 MHz		Variable CPU Clock 1/2TCL = 1 to 20 MHz		Unit
		min.	max.	min.	max.	
CLKOUT cycle time	t_{29} CC	50	50	2TCL	2TCL	ns
CLKOUT high time	t30 CC	15	–	TCL – 10	–	ns
CLKOUT low time	t31 CC	15	–	TCL – 10	–	ns
CLKOUT rise time	t_{32} CC	–	5	–	5	ns
CLKOUT fall time	t_{33} CC	–	5	–	5	ns
CLKOUT rising edge to ALE falling edge	t_{34} CC	$0 + t_A$	$10 + t_A$	$0 + t_A$	$10 + t_A$	ns
Synchronous $\overline{\text{READY}}$ setup time to CLKOUT	t_{35} SR	10	–	10	–	ns
Synchronous $\overline{\text{READY}}$ hold time after CLKOUT	t_{36} SR	10	–	10	–	ns
Asynchronous $\overline{\text{READY}}$ low time	t_{37} SR	65	–	2TCL + 15	–	ns
Asynchronous $\overline{\text{READY}}$ setup time [1]	t58 SR	20	–	20	–	ns
Asynchronous $\overline{\text{READY}}$ hold time [1]	t59 SR	0	–	0	–	ns
Async. $\overline{\text{READY}}$ hold time after $\overline{\text{RD}}$, $\overline{\text{WR}}$ high (Demultiplexed Bus) [2]	t60 SR	0	$0 + 2t_A + t_F$ [2]	0	TCL - 25 $+ 2t_A + t_F$ [2]	ns

Notes:

1) These timings are given for test purposes only, in order to assure recognition at a specific clock edge.

2) Demultiplexed bus is the worst case. For multiplexed bus 2TCL are to be added to the maximum values. This adds even more time for deactivating $\overline{\text{READY}}$.

AC Characteristics (Cont'd)

CLKOUT and $\overline{READY}$ for ST10F166-16

V_{CC} = 5 V ± 10 %; V_{SS} = 0 V
T_A = 0 to +70 °C
C_L (for Port 0, Port 1, Port 4, ALE, $\overline{RD}$, $\overline{WR}$, $\overline{BHE}$, CLKOUT) = 100 pF

Parameter	Symbol	CPU Clock = 16 MHz Duty cycle 0.4 to 0.6		Variable CPU Clock 1/CLP = 1 to 20 MHz		Unit
		min.	max.	min.	max.	
CLKOUT cycle time	t_{29} CC	62.5	62.5	CLP	CLP	ns
CLKOUT high time	t30 CC	15	–	TCL_{min} – 10	–	ns
CLKOUT low time	t31 CC	15	–	TCL_{min} – 10	–	ns
CLKOUT rise time	t_{32} CC	–	5	–	5	ns
CLKOUT fall time	t_{33} CC	–	5	–	5	ns
CLKOUT rising edge to ALE falling edge	t_{34} CC	0 + t_A	10 + t_A	0 + t_A	10 + t_A	ns
Synchronous $\overline{READY}$ setup time to CLKOUT	t_{35} SR	10	–	10	–	ns
Synchronous $\overline{READY}$ hold time after CLKOUT	t_{36} SR	10	–	10	–	ns
Asynchronous $\overline{READY}$ low time	t_{37} SR	77.5	–	CLP + 15	–	ns
Asynchronous $\overline{READY}$ setup time [1]	t58 SR	20	–	20	–	ns
Asynchronous $\overline{READY}$ hold time [1]	t59 SR	0	–	0	–	ns
Async. $\overline{READY}$ hold time after $\overline{RD}$, $\overline{WR}$ high (Demultiplexed Bus) [2]	t60 SR	0	0 + $2t_A$ + t_F [2]	0	TCL - 25 + $2t_A$ + t_F [2]	ns

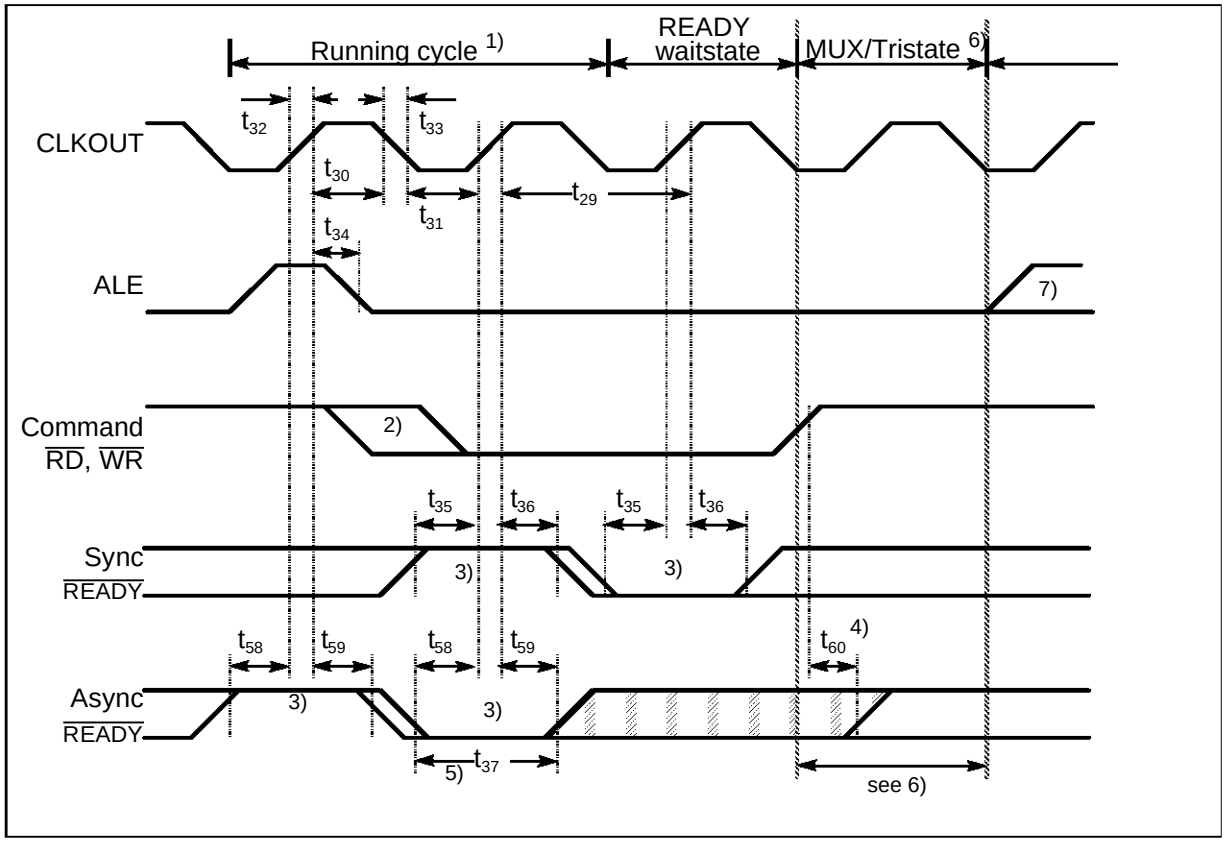
Notes:

1) These timings are given for test purposes only, in order to assure recognition at a specific clock edge.

2) Demultiplexed bus is the worst case. For multiplexed bus 2TCL are to be added to the maximum values. This adds even more time for deactivating $\overline{READY}$.
The $2t_A$ refer to the next following bus cycle.

AC Characteristics (Cont'd)

Figure 23. CLKOUT and $\overline{\text{READY}}$



Notes:

1) Cycle as programmed, including MCTC waitstates (Example shows 0 MCTC WS).

2) The leading edge of the respective command depends on RW-delay.

3) $\overline{\text{READY}}$ sampled HIGH at this sampling point generates a READY controlled waitstate, $\overline{\text{READY}}$ sampled LOW at this sampling point terminates the currently running bus cycle.

4) $\overline{\text{READY}}$ may be deactivated in response to the trailing (rising) edge of the corresponding command ($\overline{\text{RD}}$ or $\overline{\text{WR}}$).

5) If the Asynchronous $\overline{\text{READY}}$ signal does not fulfill the indicated setup and hold times with respect to CLKOUT (eg. because CLKOUT is not enabled), it must fulfill t_{37} in order to be safely synchronized. This is guaranteed, if $\overline{\text{READY}}$ is removed in reponse to the command (see Note 4)).

6) Multiplexed bus modes have a MUX waitstate added after a bus cycle, and an additional MTTC waitstate may be inserted here.
For a multiplexed bus with MTTC waitstate this delay is 2 CLKOUT cycles, for a demultiplexed bus without MTTC waitstate this delay is zero.

7) The next external bus cycle may start here

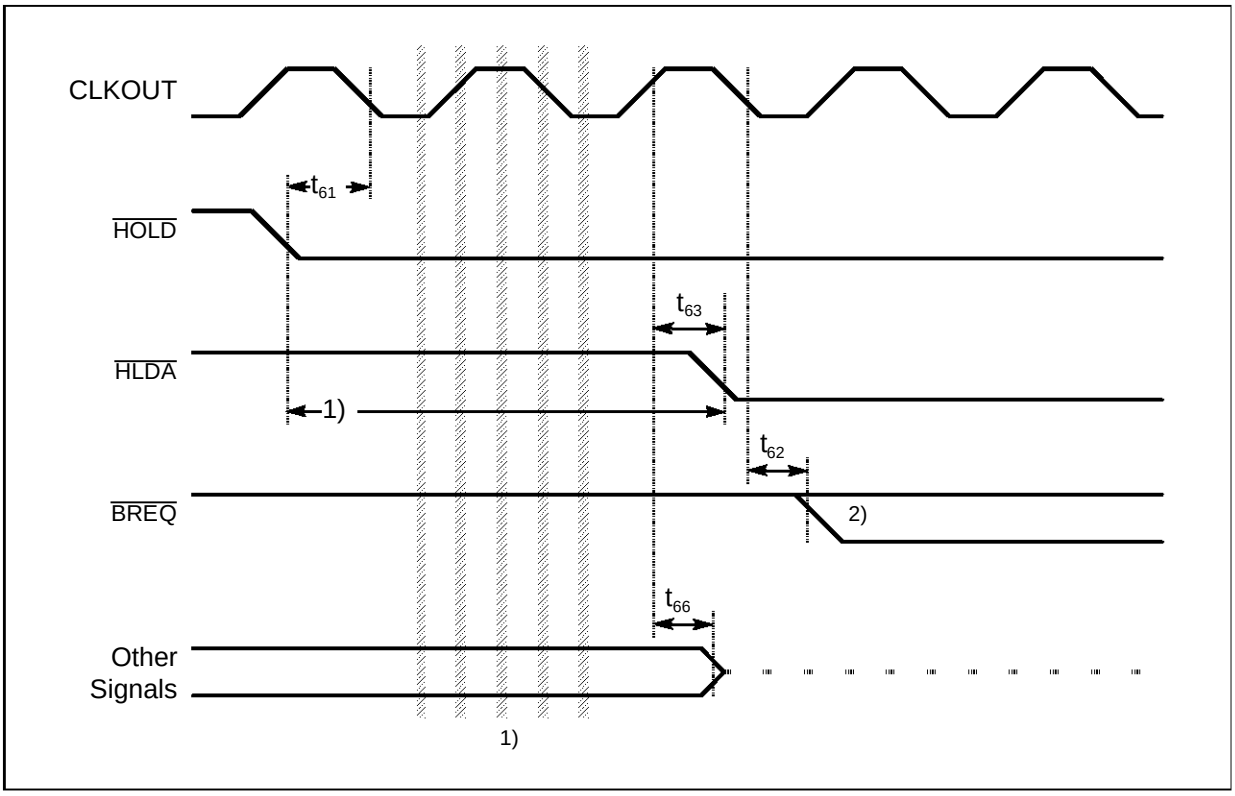
AC Characteristics (Cont'd)

External Bus Arbitration

V_{CC} = 5 V ± 10 %; V_{SS} = 0 V
T_A = 0 to +70 °C for ST10R165
C_L (for Port 0, Port 1, Port 4, ALE, $\overline{RD}$, $\overline{WR}$, $\overline{BHE}$, CLKOUT) = 100 pF

Parameter	Symbol	Max. CPU Clock = 20 MHz		Variable CPU Clock 1/2TCL = 1 to 20 MHz		Unit
		min.	max.	min.	max.	
$\overline{HOLD}$ input setup time to CLKOUT	t_{61} SR	20	–	20	–	ns
CLKOUT to $\overline{HLDA}$ high or $\overline{BREQ}$ low delay	t_{62} CC	–	30	–	30	ns
CLKOUT to $\overline{HLDA}$ low or $\overline{BREQ}$ high delay	t_{63} CC	–	30	–	30	ns
Other signals release	t66 CC	–	25	–	25	ns
Other signals drive	t67 CC	-5	35	-5	35	ns

Figure 24. External Bus Arbitration, Releasing the Bus



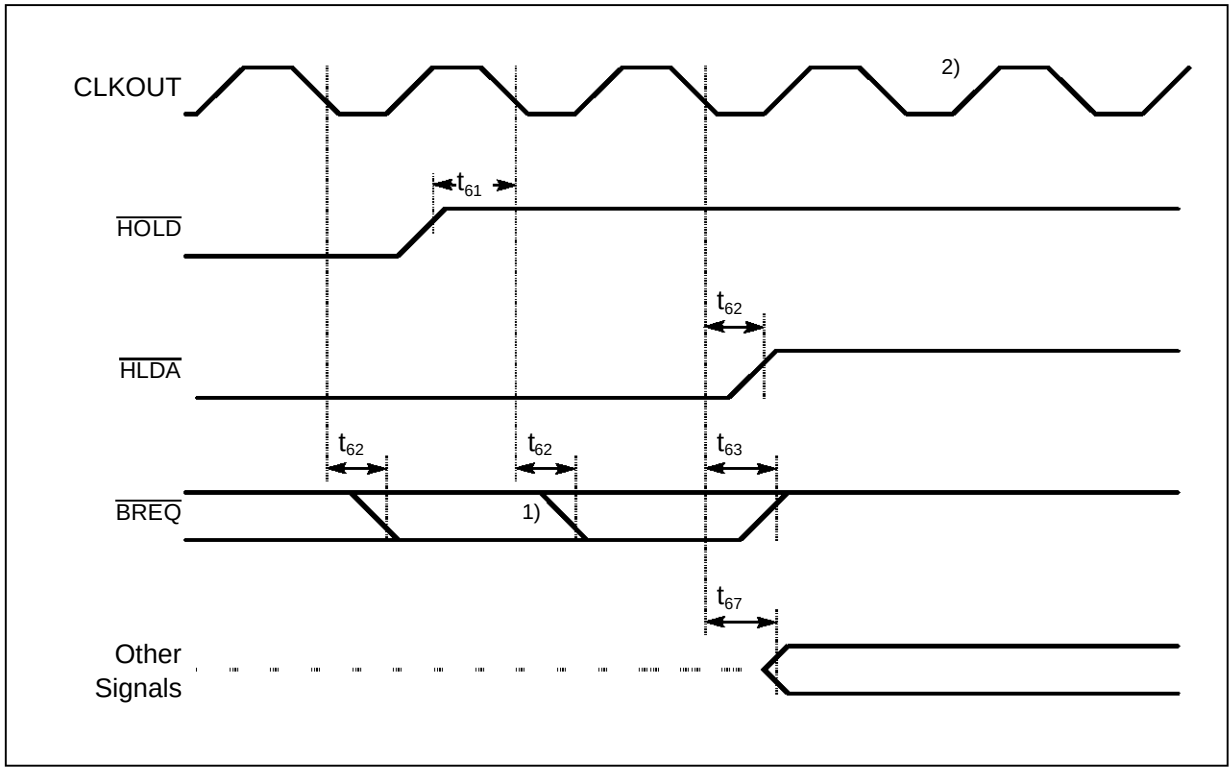
Notes:

1) The ST10R165 will complete the currently running bus cycle before granting bus access.

2) This is the first possibility for $\overline{BREQ}$ to get active.

AC Characteristics (Cont'd)

Figure 25. External Bus Arbitration, (Regaining the Bus)



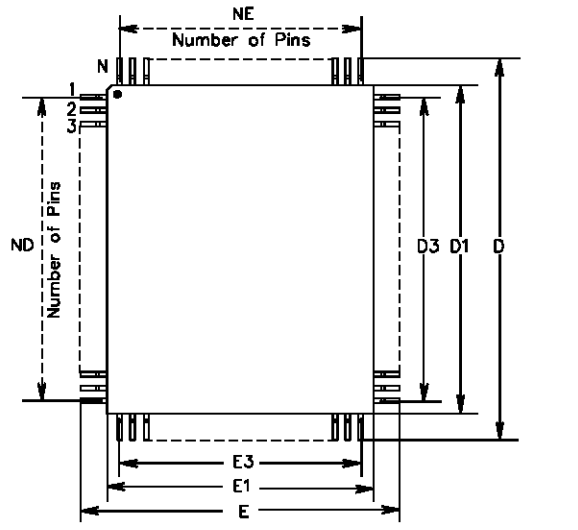
Notes:

1) This is the last chance for BREQ to trigger the indicated regain-sequence.
Even if BREQ is activated earlier, the regain-sequence is initiated by HOLD going high.
Please note that HOLD may also be deactivated without the ST10R165 requesting the bus.

2) The next ST10R165 driven bus cycle may start here.

19 GENERAL INFORMATION

Figure 26. Package Outline PQFP100 (14 x 20 mm)



Dim	mm			inches		
	Min	Typ	Max	Min	Typ	Max
A			3.40			0.134
A2	2.55	2.80	3.05	0.100	0.110	0.120
D	22.95	23.20	23.45	0.931	0.913	0.923
D1	19.90	20.00	20.10	0.783	0.787	0.791
D3		18.85			0.742	
E	16.95	17.20	17.45	0.695	0.667	0.687
E1	13.90	14.00	14.10	0.547	0.551	0.555
E3		12.35			0.486	
e		0.65			0.026	

Number of Pins	
ND	30
NE	20
N	100

Table 8. Ordering Information

Type	Package	Function
ST10F166BQ1	PQFP-100	16-bit microcontroller, 0 °C to +70 °C, 1 KByte RAM, 32 KByte Flash EPROM
ST10F166BQ1-16		16-bit microcontroller, 0 °C to +70°C, w/o Prescaler, 1 KByte RAM, 32 KByte Flash EPROM