

### Analog Peripherals

#### 12-Bit ADC, 5 V input signal; up to 25 external inputs

- $\pm 1$  LSB INL; guaranteed monotonic
- Programmable throughput up to 200 ksp/s
- Data-dependent windowed interrupt generator
- Programmable gain maximizes input signal span

#### Built-in Temperature Sensor ( $\pm 3$ °C)

#### Two Comparators

#### Precision Internal Voltage Reference

#### V<sub>DD</sub> Monitor/Brown-out Detector

#### On-Chip Debug

- On-chip debug circuitry facilitates full speed, non-intrusive in-system debug (no emulator required)
- Provides breakpoints, single stepping, watch-points
- Inspect/modify memory, registers, and stack
- Superior performance to emulation systems using ICE-chips, target pods, and sockets

#### Temperature Range: -40 to +125 °C

#### Operating Voltage: 1.8 to 5.25 V

- Multiple power saving sleep and shutdown modes

#### Development Kit: C8051F560DK

### High-Speed 8051 $\mu$ C Core

- Pipelined instruction architecture; executes 70% of instructions in one or two system clocks
- Up to 50 MIPS throughput

### Memory

- 16 kB Flash; in-system programmable; flexible security features
- 2304 bytes data RAM (256 + 2 kB)

### CAN 2.0B

- 32 message objects

### Digital Peripherals

- Up to 25 digital I/O; all are 5 V push-pull
- Hardware I<sup>2</sup>C, SPI™, and UART serial ports available concurrently
- Programmable 16-bit counter array with six capture/compare modules
- Four general-purpose 16-bit counter/timers

### Clock Sources

- Internal programmable  $\pm 0.5\%$  oscillator: Up to 50 MHz
- External oscillator: Crystal, RC, C, or CMOS Clock

### Ordering Part Numbers

- C8051F565-IM, 32-Pin QFN (RoHS-compliant), 5 x 5 mm<sup>2</sup>
- C8051F565-IQ, 32-Pin QFP (RoHS-compliant), 9 x 9 mm<sup>2</sup>

