C8051F530

25 MIPS, 8 kB Flash, 12-Bit ADC, 20-Pin Automotive MCU

Analog Peripherals

12-Bit ADC, 5 V input signal; up to 16 external inputs

- ±1 LSB INL; guaranteed monotonic
- Programmable throughput up to 200 ksps
- Data-dependent windowed interrupt generator
- Programmable gain maximizes input signal span

Built-in Temperature Sensor (±3 °C)

One Comparator

Internal Voltage Reference

Precision V_{DD} Monitor/Brown-out Detector

On-Chip Debug

- On-chip debug circuitry facilitates full speed, non-intrusive in-system debug (no emulator required)
- Provides breakpoints, single stepping, watch-points
- Inspect/modify memory, registers, and stack
- Superior performance to emulation systems using ICE-chips, target pods, and sockets

Supply Voltage: 2.7 to 5.25 V

- Typical operating current: 7 mA at 25 MHz at 5.0 V
- Multiple power saving sleep and shutdown modes

Temperature Range: –40 to +125 °C

High-Speed 8051 µC Core

- Pipelined instruction architecture; executes 70% of instructions in 1 or 2 system clocks
- Up to 25 MIPS throughput with 25 MHz system clock
- Expanded interrupt handler

Memory

- 8 kB Flash; in-system programmable; flexible security features
- 256 bytes data RAM

LIN 2.0

- Master or slave operation using dedicated hardware (not software implementation with UART)

Digital Peripherals

- Up to 16 digital I/O; all are 5 V push-pull
- Programmable 16-bit counter array with three capture/compare modules
- Three general-purpose 16-bit counter/timers
- Dedicated watchdog timer; bidirectional reset
- Real-time clock mode using timer 3 or PCA

Clock Sources

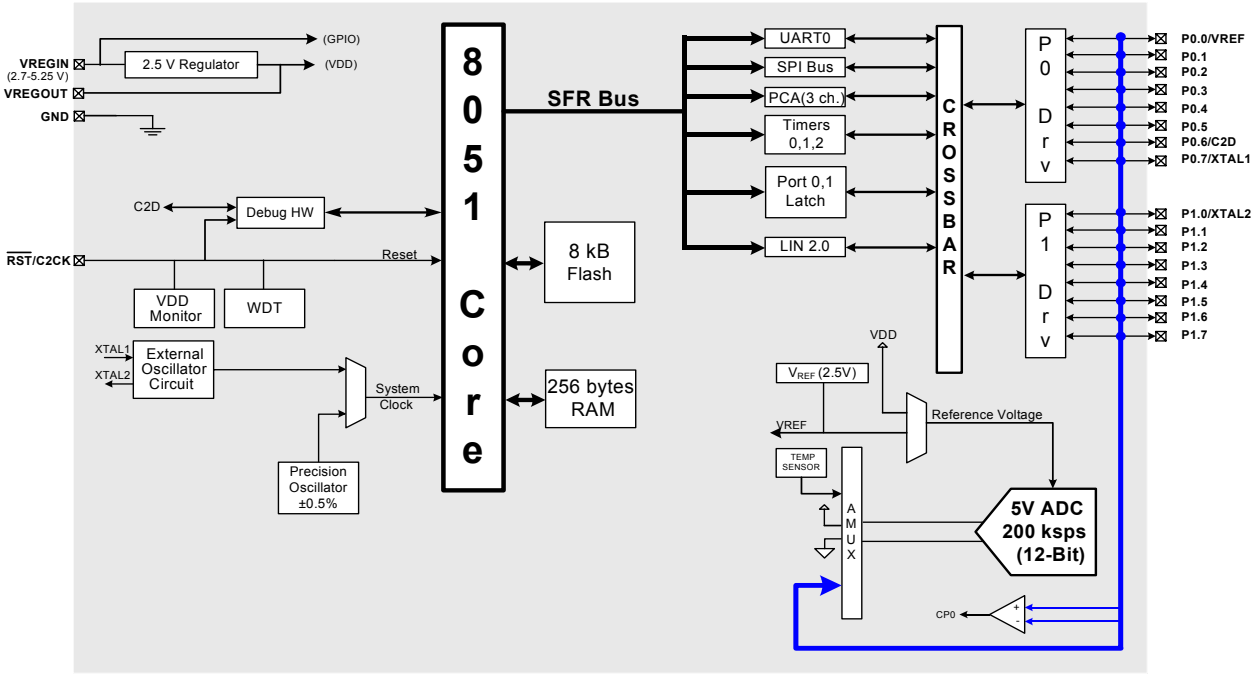
- High-precision internal programmable oscillator up to 25 MHz
- External oscillator: Crystal, RC, C, or Clock

Packages

- 20-Pin TSSOP and 20-Pin QFN (4x4 mm)

Ordering Part Numbers

- C8051F530-IT (TSSOP)
- C8051F530-IM (QFN)

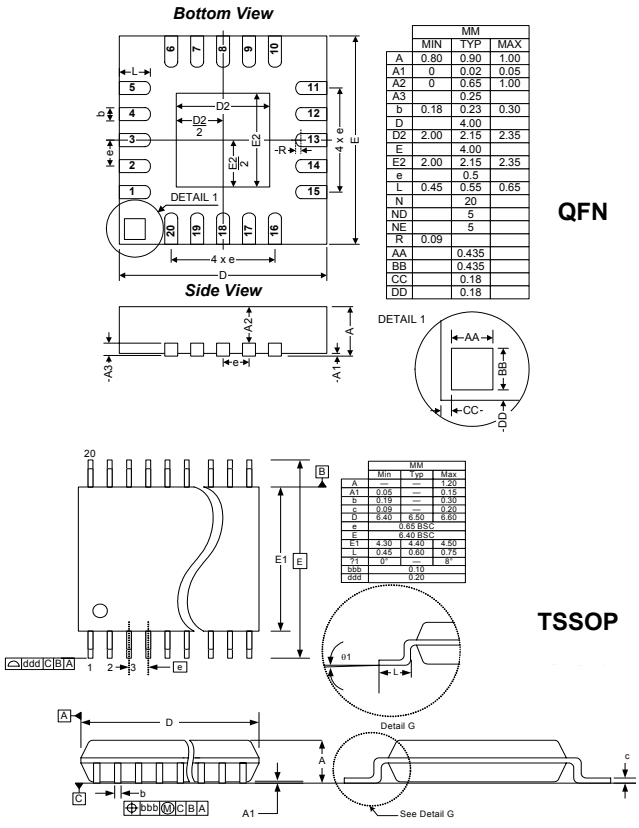


Selected Electrical Specifications

(T_A = –40 to +125 C°, V_{REGIN} = 2.7 V unless otherwise specified)

Parameter	Conditions	Min	Typ	Max	Units
Global Characteristics					
Supply Voltage (V_{REGIN})		2.7	—	5.25	V
Supply Current (CPU active) V_{REGIN} = 2.7–5.0 V	Clock = 25 MHz Clock = 1 MHz Clock = 32 kHz; V_{DD} monitor enabled	— — —	7 0.8 33	— — —	mA mA µA
Supply Current (shutdown)	Oscillator not running; V_{DD} monitor disabled	—	0.2	—	µA
Clock Frequency Range		dc	—	25	MHz
A/D Converter					
Resolution			12		bits
Integral Nonlinearity		—	—	±1	LSB
Differential Nonlinearity	Guaranteed monotonic	—	—	±1	LSB
Signal-to-Noise Plus Distortion		—	68	—	dB
Throughput Rate		—	—	200	ksps
Input Voltage Range		0	—	V_{REF}	V
Flash					
Endurance		40K	150K	—	E/W cycles
Erase Cycle Time		10	12	14	ms
Write Cycle Time		40	50	60	µs

Package Information



	MM		
	MIN	TYP	MAX
A	0.80	0.90	1.00
A1	0	0.02	0.05
A2	0	0.65	1.00
A3		0.25	
b	0.18	0.23	0.30
D		4.00	
D2	2.00	2.15	2.35
E		4.00	
E2	2.00	2.15	2.35
e		0.5	
L	0.45	0.55	0.65
N		20	
ND		5	
NE		5	
R	0.09		
AA		0.435	
BB		0.435	
CC		0.18	
DD		0.18	

QFN

TSSOP

C8051F530DK Development Kit