

Analog Peripherals

Two Comparators

- Programmable hysteresis and response time
- Configurable to generate interrupts or reset
- Low current

On-Chip Debug

- On-chip debug circuitry facilitates full speed, non-intrusive in-system debug (no emulator required)
- Provides breakpoints, single stepping, watchpoints
- Inspect/modify memory, registers, and stack
- Superior performance to emulation systems using ICE-chips, target pods, and sockets

Supply Voltage: 2.7 to 3.6 V

Temperature Range: -40 to +85 °C

High-Speed 8051 µC Core

- Pipelined instruction architecture; executes 70% of instructions in 1 or 2 system clocks
- Up to 100 MIPS throughput with 100 MHz system clock
- 16 x 16 multiply/accumulate engine (2-cycle)

Memory

- 1280 bytes data RAM
- 32 kB Flash; in-system programmable in 512 byte sectors (512 bytes are reserved)

Digital Peripherals

- 24 port I/O; all are 5 V tolerant
- Hardware SMBus™ (I2C™ compatible), SPI™, and UART serial ports available concurrently
- Programmable 16-bit counter/timer array with six capture/compare modules, WDT
- 4 general-purpose 16-bit counter/timers
- Real-time clock mode using PCA or timer and external clock source

Clock Sources

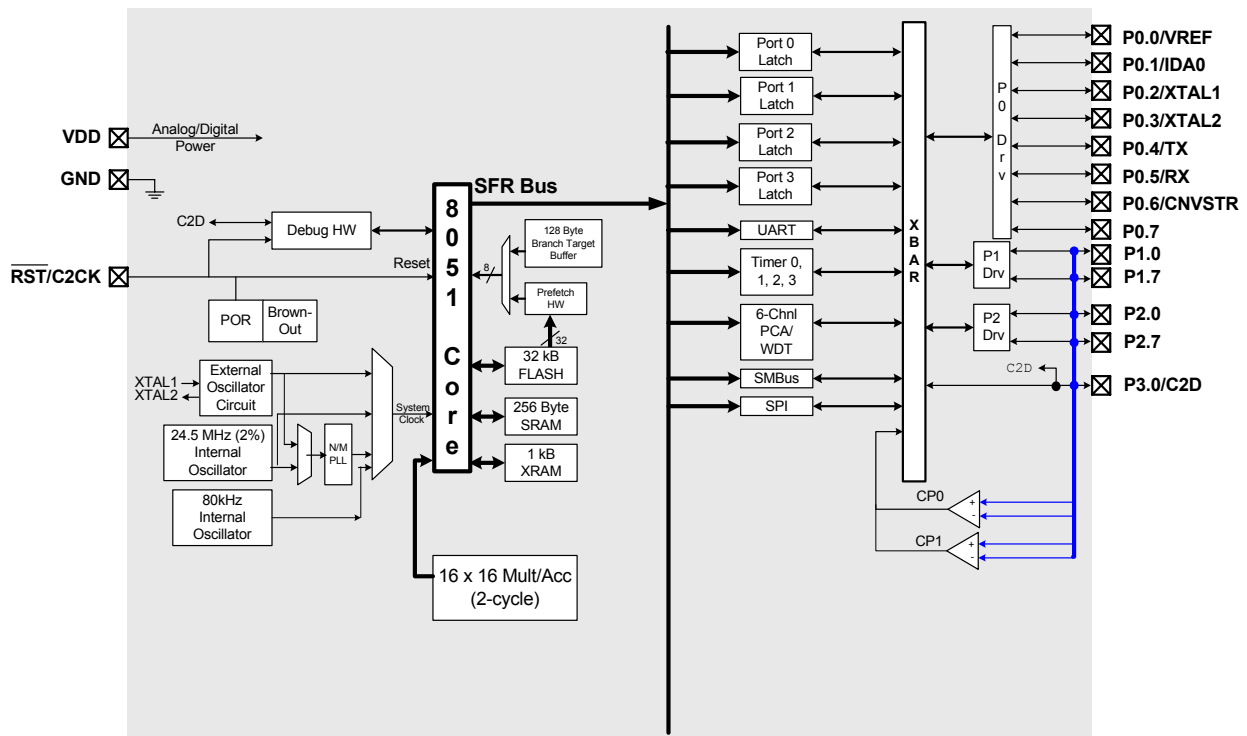
- Two internal oscillators:
 - 24.5 MHz, 2% accuracy supports UART operation
 - 80 kHz low frequency, low-power
- External oscillator: Crystal, RC, C, or Clock (1 or 2 pin modes)
- On-Chip programmable PLL: up to 100 MHz

Package

- 28-pin QFN
- Pin compatible with C8051F311

Ordering Part Number

- C8051F365-GM

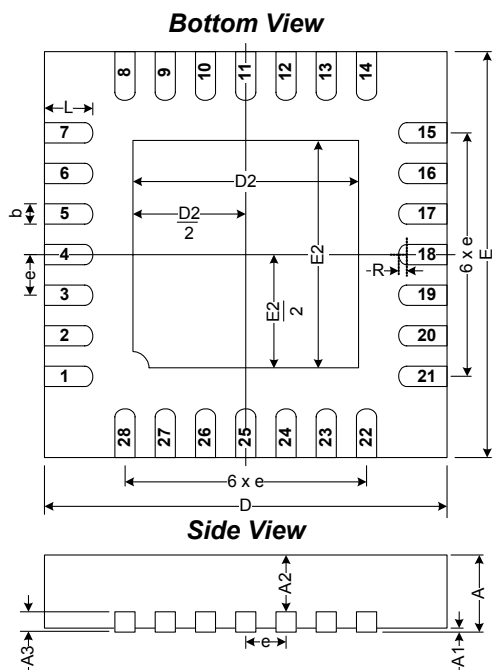


Selected Electrical Specifications

($T_A = -40$ to $+85$ C°, $V_{DD} = 2.7$ V unless otherwise specified)

| Parameter | Conditions | Min | Typ | Max | Units |
|--------------------------------|--|------|------|------|-------|
| Global Characteristics | | | | | |
| Supply Voltage | | 2.7 | — | 3.6 | V |
| Supply Current with CPU active | Clock = 100 MHz | — | TBD | — | mA |
| | Clock = 25 MHz | — | TBD | — | mA |
| | Clock = 1 MHz | — | TBD | — | μA |
| | Clock = 80 kHz; V_{DD} Monitor Disabled | — | TBD | — | μA |
| Supply Current (shutdown) | Oscillator off; V_{DD} Monitor Disabled | — | <0.1 | — | μA |
| Clock Frequency Range | | DC | — | 100 | MHz |
| Internal Oscillators | | | | | |
| Frequency (OSC0) | | 24.0 | 24.5 | 25.0 | MHz |
| Frequency (OSC1) | OSC1 can be calibrated in 2.5% steps using an internal calibration register. | — | 80 | — | kHz |
| Comparator | | | | | |
| Response Time Mode0 | (CP+) – (CP-) = 100 mV | — | 100 | — | ns |
| Current Consumption Mode0 | | — | TBD | — | μA |
| Response Time Mode1 | (CP+) – (CP-) = 100 mV | — | 175 | — | ns |
| Current Consumption Mode1 | | — | TBD | — | μA |
| Response Time Mode2 | (CP+) – (CP-) = 100 mV | — | 320 | — | ns |
| Current Consumption Mode2 | | — | TBD | — | μA |
| Response Time Mode3 | (CP+) – (CP-) = 100 mV | — | 1050 | — | ns |
| Current Consumption Mode3 | | — | TBD | — | μA |

Package Information



C8051F360DK Development Kit

