LPC3180

16/32-bit ARM microcontroller; hardware floating-point coprocessor, USB On-The-Go, and SDRAM memory interface

Rev. 01 — 21 February 2006 Preliminary data sheet

1. General description

The LPC3180 is an ARM9-based microcontroller for embedded applications requiring high performance combined with low power dissipation. It achieves these objectives through the combination of Philips' state-of-the-art 90 nanometer technology with an ARM926EJ-S CPU core with a Vector Floating Point (VFP) coprocessor and a large array of standard peripherals including USB On-The-Go.

The microcontroller can operate at over 200 MHz CPU frequency (about 220 MIPS per ARM Inc.). The ARM926EJ-S CPU incorporates a 5-stage pipeline and has a Harvard architecture with separate 32 kB Instruction and Data caches, a demand paged MMU, DSP instruction extensions with a single cycle MAC, and Jazelle Java Bytecode execution hardware. A block diagram of the microcontroller is shown in Figure 1.

Power optimization in this microcontroller is done through process and technology development (Intrinsic Power), and architectural means (Managed Power).

The LPC3180 also incorporates an SDRAM interface, NAND flash interfaces, USB 2.0 Full-speed interface, seven UARTs, two I^2C interfaces, two SPI ports, a Secure Digital (SD) interface, and a 10-bit ADC in addition to many other features.

2. Features

2.1 Key features

- ARM926EJ-S processor with 32 kB instruction cache and 32 kB data cache, running at up to 208 MHz.
- 64 kB of SRAM.
- High-performance multilayer AHB bus system provides a separate bus for CPU data and instruction fetch, two data buses for the DMA controller, and another for the USB controller.
- External memory interfaces: One supports DDR and SDR SDRAM, another supports single-level and multi-level NAND flash devices and can serve as an 8-bit parallel interface.
- General purpose DMA controller that can be used with the SD card and SPI interfaces, as well as for memory-to-memory transfers.
- USB 2.0 Full-speed device, host (OHCI compliant), and OTG block. A dedicated PLL provides the 48 MHz USB clock.
- Multiple serial interfaces, including seven UARTs, two SPI controllers, and two single master I^2C interfaces.
- SD memory card interface.

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- Up to 55 General Purpose (GP) input, output, and I/O pins. Includes 12 GP input pins, 24 GP output pins, and six GP I/O pins.
- 10-bit ADC with input multiplexing from three pins.
- Real Time Clock (RTC) with separate power supply and power domain, clocked by a dedicated 32 kHz oscillator. Includes a 128 byte scratch pad memory. The RTC may remain active when the rest of the chip is not powered.
- 32-bit general purpose high-speed timer with 16-bit pre-scaler with capture and compare capability
- 32-bit millisecond timer driven from the RTC clock. Interrupts may be generated using two match registers.
- Watchdog timer.
- Two PWM blocks with an output rate up to 50 kHz.
- Keyboard scanner function provides automatic scanning of up to an 8 × 8 key matrix.
- Standard ARM Test/Debug interface for compatibility with existing tools.
- Emulation trace buffer with 2k × 24 bit RAM allows trace via JTAG.
- On-chip crystal oscillator.
- Stop mode saves power, while allowing many peripheral functions to restart CPU activity.
- On-chip PLL allows CPU operation up to the maximum CPU rate without the need for a high frequency crystal.
- Boundary scan for simplified board testing.

3. Ordering information

Table 1: Ordering information

Type number	Package		
	Name	Description	Version
LPC3180FEL320 [1]	LFBGA320	plastic low profile fine-pitch ball grid array package; 320 balls; body 13 × 13 × 0.9 mm	SOT824-1

[1] F = −40 to +85 °C temperature range

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4. Block diagram

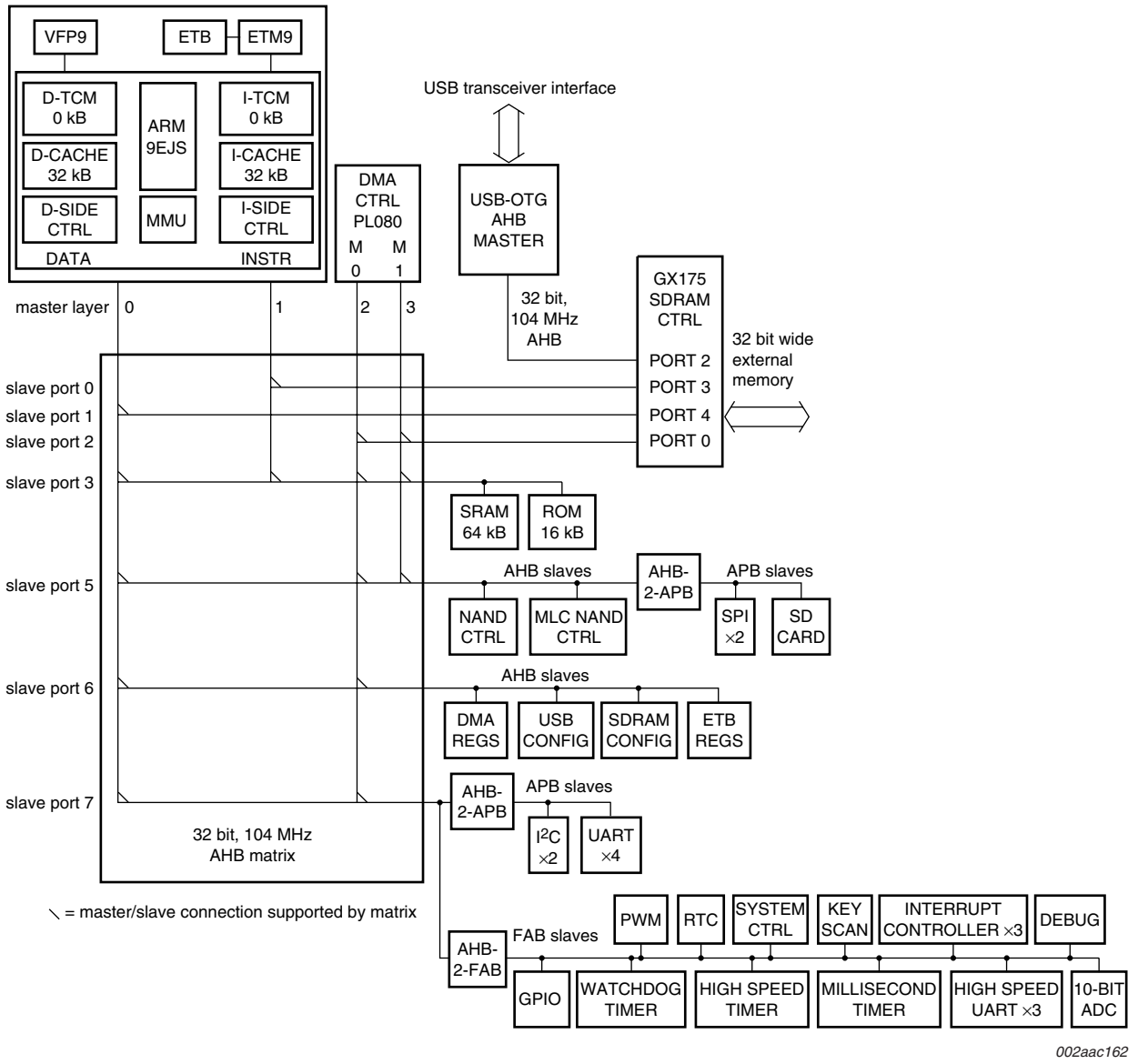

Fig 1. Block diagram

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5. Pinning information

5.1 Pinning

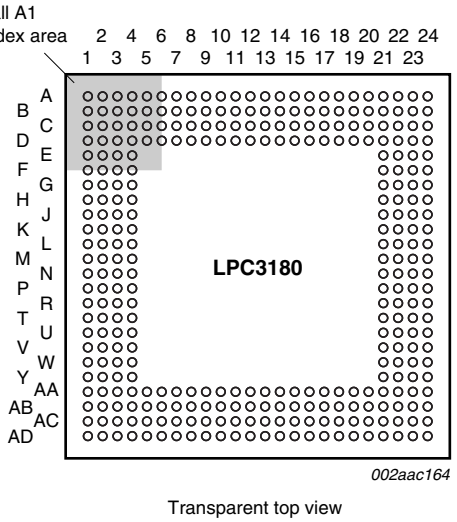

Fig 2. LPC3180 package

Table 2: Pin allocation table

Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol
Row A							
1	U6_IRRX / PIO_INP[21]	2	U5_RX / PIO_INP[20]	3	HIGHCORE	4	JTAG1_TDO
5	JTAG1_TMS	6	JTAG1_RTCK	7	U3_TX	8	VSS
9	VSS	10	VSSio1828_02	11	GPO_23 / U2_HRTS	12	GPI_05
13	RTCX_OUT	14	RTCX_IN	15	VSS	16	VDD28
17	VDD28	18	i.c. [1]	19	VDD28	20	VSS
21	VDD12	22	VDDpllHCLK-12	23	SYSX_IN	24	i.c. [1]
Row B							
1	KEY_COL5	2	U7_HCTS / PIO_INP[22]	3	U7_TX	4	VDDio1828_02
5	JTAG1_TCK	6	JTAG1_TDI	7	VDDio1828_01	8	U2_HCTS / PIO_INP[16]
9	U1_RX / PIO_INP[15]	10	U1_TX	11	VSS	12	GPO_17
13	VSSrtccore	14	VDD12	15	VSS	16	VSS
17	i.c. [1]	18	i.c. [1]	19	VDD12	20	VSSpllUSB
21	VSSosc	22	VDDpllUSB-12	23	SYSX_OUT	24	i.c. [1]
Row C							
1	KEY_COL2	2	KEY_COL3	3	U7_RX / PIO_INP[23]	4	U5_TX
5	SYSCLKEN	6	U3_RX / PIO_INP[18]	7	U2_RX / PIO_INP[17]	8	VSS
9	VSS	10	VDDcorefixed12_01	11	VDDrtccore12	12	VDDrtc12

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Table 2: Pin allocation table *...continued*

Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol
13	VSSrtcosc	14	VDDrtcosc12	15	i.c. [1]	16	VSS
17	VDD28	18	i.c. [1]	19	VSS	20	VSScore_01
21	PLL397_LOOP	22	VDDpll397-12	23	VSSpll397	24	ADIN0
Row D							
1	KEY_ROW4	2	KEY_COL0	3	TEST	4	VSSio1828_01
5	U6_IRTX	6	VDDcore12_02	7	JTAG1_NTRST	8	VSScore_02
9	U2_TX	10	GPI_11	11	VSS	12	ONSW
13	RESET_N	14	VDD28	15	VSS	16	VSScore_03
17	VSS	18	VDDcorefixed12_02	19	VSSpllHCLK	20	VDDosc12
21	i.c. [1]	22	VSSad	23	ADIN2	24	VDDad28
Row E							
1	KEY_ROW2	2	KEY_ROW5	3	VSSio28_01	4	KEY_COL4
21	VDDad28	22	ADIN1	23	RAM_D[30] / PIO_SD[11]	24	RAM_D[31] / PIO_SD[12]
Row F							
1	VSSio28_02	2	KEY_ROW1	3	KEY_ROW3	4	KEY_COL1
21	RAM_D[29] / PIO_SD[10]	22	VDDsdram18_02	23	VSSsdram_01	24	RAM_D[28] / PIO_SD[09]
Row G							
1	i.c. [1]	2	i.c. [1]	3	KEY_ROW0	4	VDDio28_02
21	VDDsdram18_01	22	VSSsdram_02	23	RAM_D[24] / PIO_SD[05]	24	RAM_D[27] / PIO_SD[08]
Row H							
1	GPI_00	2	i.c. [1]	3	PWM_OUT2	4	i.c. [1]
21	RAM_D[19] / PIO_SD[00]	22	RAM_D[23] / PIO_SD[04]	23	RAM_D[26] / PIO_SD[07]	24	RAM_D[21] / PIO_SD[02]
Row J							
1	GPI_07	2	PWM_OUT1	3	GPI_02	4	VSScore_04
21	RAM_D[25] / PIO_SD[06]	22	VDDsdram18_03	23	VSSsdram_03	24	RAM_D[20] / PIO_SD[01]
Row K							
1	GPI_10 / U4_RX	2	GPI_08 / KEY_COL6 / SPI2_BUSY	3	GPI_01 / SERVICE_N	4	GPI_04 / SPI1_BUSY
21	VDDcore12_03	22	VDDsdram18_04	23	RAM_D[22] / PIO_SD[03]	24	RAM_D[18] / DDR_nCLK
Row L							
1	GPO_03	2	GPI_09 / KEY_COL7	3	VDDcore12_05	4	GPO_02
21	RAM_D[17] / DDR_DQS1	22	RAM_D[13]	23	RAM_D[16] / DDR_DQS0	24	RAM_D[15]
Row M							
1	GPO_08	2	GPO_10	3	GPO_07	4	GPO_06
21	VSSsdram_04	22	RAM_D[10]	23	RAM_D[14]	24	RAM_D[12]
Row N							

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Table 2: Pin allocation table *...continued*

Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol
1	GPO_13	2	GPO_16	3	VSSio28_03	4	GPO_09
21	RAM_D[07]	22	VSSsdram_05	23	RAM_D[11]	24	RAM_D[09]
Row P							
1	GPO_18	2	GPO_22 / U7_HRTS	3	GPO_12	4	GPO_21 / U4_TX
21	RAM_D[04]	22	VDDsdram18_05	23	RAM_D[08]	24	RAM_D[06]
Row R							
1	GPIO_01	2	GPIO_05	3	VSScore_05	4	GPO_15
21	VSScore_06	22	VSSsdram_06	23	RAM_D[05]	24	RAM_D[03]
Row T							
1	GPIO_03 / KEY_ROW7	2	GPIO_04	3	GPIO_00	4	SPI2_DATIN
21	RAM_CLKIN	22	RAM_D[01]	23	RAM_D[00]	24	RAM_D[02]
Row U							
1	i.c. [1]	2	MS_DIO1	3	GPIO_02 / KEY_ROW6	4	VDDio28_01
21	RAM_RAS_N	22	VDDsdram18_06	23	RAM_CLK	24	RAM_CKE
Row V							
1	SPI1_DATIN	2	SPI2_DATIO	3	SPI2_CLK	4	MS_DIO3
21	RAM_DQM[2]	22	RAM_WR_N	23	RAM_CAS_N	24	RAM_CS_N
Row W							
1	SPI1_DATIO	2	MS_DIO0	3	SPI1_CLK	4	VSS
21	RAM_A[14]	22	VSSsdram_07	23	RAM_DQM[1]	24	RAM_DQM[3]
Row Y							
1	MS_BS	2	MS_DIO2	3	GPO_04	4	I2C1_SCL
21	VDDsdram18_07	22	RAM_A[10]	23	RAM_A[12]	24	RAM_DQM[0]
Row AA							
1	MS_SCLK	2	VDDcore12_01	3	GPI_06 / HSTIM_CAPTURE	4	VDD1828
5	VSScore_07	6	VSS	7	USB_ATX_INT_N	8	USB_DAT_VP / U5_RX
9	I2C2_SDA	10	VSScore_08	11	GPI_03	12	VDDcore12_06
13	i.c. [1]	14	i.c. [1]	15	VDDio18_02	16	FLASH_ALE
17	FLASH_RD_N	18	VSSsdram_10	19	VDDio18_01	20	VDDsdram18_09
21	RAM_A[05]	22	VSSsdram_08	23	RAM_A[09]	24	RAM_A[13]
Row AB							
1	GPO_11	2	VSS	3	TST_CLK2	4	VSS
5	VSS	6	VDDcore12_07	7	USB_SE0_VM / U5_TX	8	VSSio18_04
9	GPO_00 / TST_CLK1	10	GPO_05	11	VDDio18_03	12	RESOUT_N
13	i.c. [1]	14	i.c. [1]	15	i.c. [1]	16	i.c. [1]
17	VSScore_09	18	VDDcore12_08	19	FLASH_IO[04]	20	RAM_A[01]
21	VSSsdram_09	22	RAM_A[07]	23	RAM_A[08]	24	RAM_A[11]

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Table 2: Pin allocation table *...continued*

Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol
Row AC							
1	I2C1_SDA	2	VSS	3	VSS	4	VSS
5	VSS	6	VSS	7	VDDio18_04	8	USB_I2C_SCL
9	GPO_01	10	GPO_19	11	VSS	12	VSSio18_03
13	i.c. [1]	14	i.c. [1]	15	FLASH_CLE	16	VSSio18_01
17	FLASH_IO[06]	18	FLASH_RDY	19	FLASH_IO[02]	20	FLASH_IO[03]
21	FLASH_CE_N	22	RAM_A[04]	23	RAM_A[06]	24	VDDsdram18_08
Row AD							
1	VSS	2	i.c. [1]	3	VSS	4	VDD1828
5	VSS	6	USB_OE_TP_N	7	USB_I2C_SDA	8	I2C2_SCL
9	GPO_14	10	GPO_20	11	VSS	12	i.c. [1]
13	i.c. [1]	14	i.c. [1]	15	VSSio18_02	16	i.c. [1]
17	FLASH_WR_N	18	FLASH_IO[07]	19	FLASH_IO[05]	20	FLASH_IO[01]
21	FLASH_IO[00]	22	RAM_A[00]	23	RAM_A[02]	24	RAM_A[03]

[1] These pins are connected internally and must be left unconnected in an application.

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5.2 Pin description

Table 3: Pin description

Symbol	Pin	Type	Description
ADIN0	C24	I	input 0 to the ADC
ADIN1	E22	I	input 1 to the ADC
ADIN2	D23	I	input 2 to the ADC
FLASH_ALE	AA16	O	address latch enable for NAND flash
FLASH_CE_N	AC21	O	chip enable for NAND flash
FLASH_CLE	AC15	O	command latch enable for NAND flash
FLASH_IO[00] to FLASH_IO[07]	AD21, AD20, AC19, AC20, AB19, AD19, AC17, AD18	I/O	NAND flash data bus
FLASH_RD_N	AA17	O	read strobe for NAND flash
FLASH_RDY	AC18	I	ready status from NAND flash
FLASH_WR_N	AD17	O	write strobe for NAND flash
GPI_00	H1	I	general purpose input 00
GPI_01/ SERVICE_N	K3	I	**GPI_01 —** general purpose input 01
		I	**SERVICE_N —** boot select input
GPI_02	J3	I	general purpose input 02
GPI_03	AA11	I	general purpose input 03
GPI_04/ SPI1_BUSY	K4	I	**GPI_04 —** general purpose input 04
		I	**SPI1_BUSY —** busy input for SPI1
GPI_05	A12	I	general purpose input 05
GPI_06/ HSTIM_CAPTURE	AA3	I	**GPI_06 —** general purpose input 06
		I	**HSTIM_CAPTURE —** capture input trigger for the high-speed timer
GPI_07	J1	I	general purpose input 07
GPI_08/ KEY_COL6/ SPI2_BUSY	K2	I	**GPI_08 —** general purpose input 08
		I	**KEY_COL6 —** keyboard scan column input 6
		I	**SPI2_BUSY —** busy input for SPI2
GPI_09/ KEY_COL7	L2	I	**GPI_09 —** general purpose input 09
		I	**KEY_COL7 —** keyboard scan column input 7
GPI_10/ U4_RX	K1	I	**GPI_10 —** general purpose input 10
		I	**U4_RX —** UART 4 receive data input
GPI_11	D10	I	general purpose input 11
GPIO_00	T3	I/O	general purpose input/output 00
GPIO_01	R1	I/O	general purpose input/output 01
GPIO_02/ KEY_ROW6	U3	I/O	**GPIO_02 —** general purpose input/output 02
		O	**KEY_ROW6 —** keyboard scan row output 6
GPIO_03/ KEY_ROW7	T1	I/O	**GPIO_03 —** general purpose input/output 03
		O	**KEY_ROW7 —** keyboard scan row output 7
GPIO_04	T2	I/O	general purpose input/output 04
GPIO_05	R2	I/O	general purpose input/output 05

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Table 3: Pin description *...continued*

Symbol	Pin	Type	Description
GPO_00/ TST_CLK1	AB9	O	**GPO_00 —** general purpose output 00
		O	**TST_CLK1 —** Clock test output 1, controlled by the TEST_CLK register
GPO_01	AC9	O	general purpose output 01
GPO_02	L4	O	general purpose output 02
GPO_03	L1	O	general purpose output 03
GPO_04	Y3	O	general purpose output 04
GPO_05	AB10	O	general purpose output 05
GPO_06	M4	O	general purpose output 06
GPO_07	M3	O	general purpose output 07
GPO_08	M1	O	general purpose output 08
GPO_09	N4	O	general purpose output 09
GPO_10	M2	O	general purpose output 10
GPO_11	AB1	O	general purpose output 11
GPO_12	P3	O	general purpose output 12
GPO_13	N1	O	general purpose output 13
GPO_14	AD9	O	general purpose output 14
GPO_15	R4	O	general purpose output 15
GPO_16	N2	O	general purpose output 16
GPO_17	B12	O	general purpose output 17
GPO_18	P1	O	general purpose output 18
GPO_19	AC10	O	general purpose output 19
GPO_20	AD10	O	general purpose output 20
GPO_21/ U4_TX	P4	O	**GPO_21 —** general purpose output 21
		O	**U4_TX —** UART 4 transmit data output
GPO_22/ U7_HRTS	P2	O	**GPO_22 —** general purpose output 22
		O	**U7_HRTS —** UART 7 hardware flow control (RTS) output
GPO_23/ U2_HRTS	A11	O	**GPO_23 —** general purpose output 23
		O	**U2_HRTS —** UART 2 hardware flow control (RTS) output
HIGHCORE	A3	O	core voltage select output
I2C1_SCL	Y4	I/O	serial clock for I^2C1
I2C1_SDA	AC1	I/O	serial data for I^2C1
I2C2_SCL	AD8	I/O	serial clock for I^2C2
I2C2_SDA	AA9	I/O	serial data for I^2C2
JTAG1_NTRST	D7	I	JTAG reset input
JTAG1_RTCK	A6	O	JTAG return clock output
JTAG1_TCK	B5	I	JTAG clock input
JTAG1_TDI	B6	I	JTAG data input
JTAG1_TDO	A4	O	JTAG data output
JTAG1_TMS	A5	I	JTAG test mode select input

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Table 3: Pin description *...continued*

Symbol	Pin	Type	Description
KEY_COL0 to KEY_COL5	D2, F4, C1, C2, E4, B1	I	keyboard scan column inputs
KEY_ROW0 to KEY_ROW5	G3, F2, E1, F3, D1, E2	O	keyboard scan row outputs 0 through 5
MS_BS	Y1	I/O	SD card command input/output (SD_CMD)
MS_DIO0 to MS_DIO3	W2, U2, Y2, V4	I/O	SD card data bus (SD_D0 to SD_D3)
MS_SCLK	AA1	O	SD card clock output (SD_CLK)
ONSW	D12	O	VCCon output signal
PLL397_LOOP	C21	I/O	loop filter pin for PLL397; requires external components if PLL397 is used
PWM_OUT1	J2	O	output of Pulse Width Modulator 1
PWM_OUT2	H3	O	output of Pulse Width Modulator 2
RAM_A[00] to RAM_A[14]	AD22, AB20, AD23, AD24, AC22, AA21, AC23, AB22, AB23, AA23, Y22, AB24, Y23, AA24, W21	O	SDRAM address bus
RAM_CAS_N	V23	O	SDRAM column address strobe output
RAM_CKE	U24	O	SDRAM clock enable output
RAM_CLK	U23	O	SDRAM clock output
RAM_CLKIN	T21	I	SDRAM clock return input
RAM_CS_N	V24	O	SDRAM chip select output
RAM_D[00] to RAM_D[15]	T23, T22, T24, R24, P21, R23, P24, N21, P23, N24, M22, N23, M24, L22, M23, L24	I/O	SDRAM data bus, pins 00 to 15
RAM_D[16]/ DDR_DQS0	L23	I/O	**RAM_D[16] —** SDRAM data bus, pin 16
		O	**DDR_DQS0 —** SDRAM data strobe output for lower byte
RAM_D[17]/ DDR_DQS1	L21	I/O	**RAM_D[17] —** SDRAM data bus, pin 17
		O	**DDR_DQS1 —** SDRAM data strobe output for upper byte
RAM_D[18]/ DDR_nCLK	K24	I/O	**RAM_D[18] —** SDRAM data bus, pin 18
		O	**DDR_nCLK —** inverted SDRAM clock output for DDR
RAM_D[19] to RAM_D[31] / PIO_SD[00] to PIO_SD[12]	H21, J24, H24, K23, H22, G23, J21, H23, G24, F24, F21, E23, E24	I/O	**RAM_D[19] to RAM_D[31] —** SDRAM data bus, pins 19 to 31
		I/O	**PIO_SD[00] to PIO_SD[12] —** general purpose input/output; details may be found in Section 6.10 “General purpose parallel I/O” on page 18
RAM_DQM[0] to RAM_DQM[3]	Y24, W23, V21, W24	O	SDRAM byte write mask outputs
RAM_RAS_N	U21	O	SDRAM row address strobe output
RAM_WR_N	V22	O	SDRAM write strobe output
RESET_N	D13	I	system reset input
RESOUT_N	AB12	O	reset output signal
RTCX_IN	A14	I	RTC oscillator input
RTCX_OUT	A13	O	RTC oscillator output

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Table 3: Pin description *...continued*

Symbol	Pin	Type	Description
SPI1_CLK	W3	O	clock output for SPI1
SPI1_DATIN	V1	I	data input for SPI1
SPI1_DATIO	W1	I/O	data input/output for SPI1
SPI2_CLK	V3	O	clock output for SPI2
SPI2_DATIN	T4	I	data input for SPI2
SPI2_DATIO	V2	I/O	data input/output for SPI2
SYSCLKEN	C5	I/O	system clock request
SYSX_IN	A23	I	main oscillator input
SYSX_OUT	B23	O	main oscillator output
TEST	D3	I	test input; internally pulled down, should be left floating in an application
TST_CLK2	AB3	O	clock test output 2, controlled by the TEST_CLK
U1_RX/ PIO_INP[15]	B9	I	**U1_RX —** UART 1 receive data input
		I	**PIO_INP[15] —** general purpose input to PIO_INP_STATE register
U1_TX	B10	O	UART 1 transmit data output
U2_HCTS/ PIO_INP[16]	B8	I	**U2_HCTS —** UART 2 hardware flow control (CTS) input
		I	**PIO_INP[16] —** general purpose input to PIO_INP_STATE register
U2_RX/ PIO_INP[17]	C7	I	**U2_RX —** UART 2 receive data input
		I	**PIO_INP[17] —** general purpose input to PIO_INP_STATE register
U2_TX	D9	O	UART 2 transmit data output
U3_RX/ PIO_INP[18]	C6	I	**U3_RX —** UART 3 receive data input
		I	**PIO_INP[18] —** general purpose input to PIO_INP_STATE register
U3_TX	A7	O	UART 3 transmit data output
U5_RX/PIO_INP[20]	A2	I	**U5_RX —** UART 5 receive data input
		I	**PIO_INP[20] —** general purpose input to PIO_INP_STATE register
U5_TX	C4	O	UART 5 transmit data output
U6_IRRX/ PIO_INP[21]	A1	I/O	**U6_IRRX —** UART 6 receive data input; can be IrDA data
		I	**PIO_INP[21] —** general purpose input to PIO_INP_STATE register
U6_IRTX	D5	O	UART 6 transmit data output; can be IrDA data
U7_HCTS/ PIO_INP[22]	B2	I	**U7_HCTS —** UART 7 hardware flow control (CTS) input
		I	**PIO_INP[22] —** general purpose input to PIO_INP_STATE register
U7_RX/ PIO_INP[23]	C3	I	**U7_RX —** UART 7 receive data input
		I	**PIO_INP[23] —** general purpose input to PIO_INP_STATE register
U7_TX	B3	O	UART 7 transmit data output
USB_ATX_INT_N	AA7	I	USB interrupt from external transceiver
USB_DAT_VP/ U5_RX	AA8	I/O	**USB_DAT_VP —** USB transmit data
		I	**U5_RX —** UART 5 receive data input
USB_I2C_SCL	AC8	I/O	serial clock for USB I^2C
USB_I2C_SDA	AD7	I/O	serial data for USB I^2C
USB_OE_TP_N	AD6	I/O	USB transmit enable for DAT/SE0

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Table 3: Pin description *...continued*

Symbol	Pin	Type	Description
USB_SE0_VM/ U5_TX	AB7	I/O	**USB_SE0_VM —** USB single ended zero transmit
		O	**U5_TX —** UART 5 transmit data output
VDD12	B14, A21, B19	I	1.2 V power supply for various internal functional blocks that are not included with VDDcore or VDDcorefixed
VDDad28	D24, E21	I	3 V power supply and positive reference voltage for the ADC
VDDcore12_01 to VDDcore12_03, VDDcore12_05 to VDDcore12_08	AA2, D6, K21, L3, AA12, AB6, AB18	I	1.2 V core main power supply for the CPU and other core logic; this voltage may be reduced to 0.9 V when the core is running at or below 13 MHz; the HIGHCORE pin may be used to signal this condition to an external voltage switch
VDDcorefixed12_01, VDDcorefixed12_02	C10, D18	I	1.2 V core secondary power supply voltage for the CPU and other core logic; this supply cannot be reduced in the same manner as the VDDcore12 supply
VDD1828, VDDio1828_01, VDDio1828_02	AD4, AA4, B7, B4	I	1.8 V or 3 V power supply for I/O pins that may operate from either a 1.8 V range or a 3 V range
VDDio18_01 to VDDio18_04	AA19, AA15, AB11, AC7	I	1.8 V power supply for I/O pins that operate only from a 1.8 V range
VDD28, VDDio28_01, VDDio28_02	U4, G4, D14, A16, A17, C17, A19	I	3 V power supply for I/O pins that operate only from a 3 V range
VDDosc12	D20	I	1.2 V power supply for the main oscillator
VDDpll397-12	C22	I	1.2 V power supply for the 397x PLL
VDDpllHCLK-12	A22	I	1.2 V power supply for the HCLK PLL
VDDpllUSB-12	B22	I	1.2 V power supply for the USB PLL
VDDrtc12	C12	I	1.2 V power supply for the RTC block
VDDrtccore12	C11	I	1.2 V power supply for the RTC block
VDDrtcosc12	C14	I	1.2 V power supply for the 32 kHz RTC oscillator
VDDsdram18_01 to VDDsdram18_09	G21, F22, J22, K22, P22, U22, Y21, AC24, AA20	I	1.8 V power supply for the SDRAM controller block
VSS	B16, D15, AC11, AB2, AD1, AC2, AD5, AC5, AA6, AC6, AD3, AC4, AC3, AB4, AD11, C9, A9, A8, C8, D11, B11, B15, A15, AB5, W4, C16, D17, A20, C19	I	ground for various internal logic blocks that are not included with VDDcore or VDDcorefixed.
VSSad	D22	I	ground for the ADC; this should nominally be the same voltage as VSS, but should be isolated to minimize noise and conversion error
VSScore_01 to VSScore_09	C20, D8, D16, J4, R3, R21, AA5, AA10, AB17	I	ground for the core logic functions
VSSio1828_01 to VSSio1828_02	D4, A10	I	ground for I/O pins that may operate from either a 1.8 V range or a 3 V range
VSSio18_01 to VSSio18_04	AC16, AD15, AC12, AB8	I	ground for I/O pins that operate only from a 1.8 V range

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Table 3: Pin description *...continued*

Symbol	Pin	Type	Description
VSSio28_01 to VSSio28_03	E3, F1, N3	I	ground for I/O pins that operate only from a 3 V range
VSSosc	B21	I	ground for the main oscillator
VSSpll397	C23	I	ground for the 397x PLL
VSSpllHCLK	D19	I	ground for the HCLK PLL
VSSpllUSB	B20	I	ground for the USB PLL
VSSrtccore	B13	I	ground for the RTC block
VSSrtcosc	C13	I	ground for the 32 kHz RTC oscillator
VSSsdram_01 to VSSsdram_10	F23, G22, J23, M21, N22, R22, W22, AA22, AB21, AA18	I	ground for the SDRAM controller block
i.c.	A18, B17, B18, C18, U1, AD2, AA13, AD16, AB16, AA14, AC14, AB15, AD14, AC13, AB14, AD13, AB13, AD12, H2, G1, G2, H4, D21, B24, A24, C15		internally connected; leave open

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6. Functional description

6.1 Architectural overview

The microcontroller is a general purpose 32-bit microprocessor, which offers high performance and very low power consumption. The ARM architecture is based on RISC principles, and the instruction set and related decode mechanism are much simpler than those of microprogrammed CISCs. This simplicity results in a high instruction throughput and impressive real-time interrupt response from a small and cost-effective processor core.

A 5-stage pipeline is employed so that all parts of the processing and memory systems can operate continuously. At any one point in time, several operations are typically in progress: subsequent instruction fetch, next instruction decode, instruction execution, memory access, and writeback. The combination of architectural enhancements gives the ARM9 about 30 % better performance than an ARM7 running at the same clock rate:

- Approximately 1.3 clocks per instruction (1.9 for ARM7)
- Approximately 1.1 Dhrystone MIPS/MHz (0.9 for ARM7)

The ARM926EJ-S processor also employs a unique architectural strategy known as Thumb, which makes it ideally suited to high-volume applications with memory restrictions, or applications where code density is an issue.

The key idea behind Thumb is that of a super-reduced instruction set. Essentially, the ARM926EJ-S processor has two instruction sets:

1. The standard 32-bit ARM set.
2. A 16-bit Thumb set.

The Thumb set's 16-bit instruction length allows it to approach twice the density of standard ARM code while retaining most of the ARM's performance advantage over a traditional 16-bit processor using 16-bit registers. This is possible because Thumb code operates on the same 32-bit register set as ARM code.

Thumb code is able to provide up to 65 % of the code size of ARM, and 160 % of the performance of an equivalent ARM processor connected to a 16-bit memory system.

In addition, the ARM9 includes enhanced DSP instructions and multiplier, as well as an enhanced 32-bit MAC block.

6.2 Vector Floating Point (VFP) coprocessor

This CPU coprocessor provides full support for single-precision and double-precision add, subtract, multiply, divide, and multiply-accumulate operations at CPU clock speeds. It is compliant with the IEEE 754 standard, and enables advanced Motor control and DSP applications. The VFP has three separate pipelines for floating-point MAC operations, divide or square root operations, and load/store operations. These pipelines can operate in parallel and can complete execution out of order. All single-precision instructions, except divide and square root, take one cycle and double-precision multiply and multiply-accumulate instructions take two cycles. The VFP also provides format conversions between floating-point and integer word formats.

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6.3 AHB matrix

The microcontroller has a multi-layer AHB matrix for inter-block communication. AHB is the ARM high-speed bus, which is part of the ARM bus architecture. AHB is a high-bandwidth low-latency bus that supports multi-master arbitration and a bus grant/request mechanism. For systems where there is only one bus master (the CPU), or where there are two masters (CPU and DMA) and the CPU does not generally need to contend with the DMA for program memory access (because the CPU has access to memory on its local bus or has caches or another AHB bus etc.), this arrangement works well. However, if there are multiple bus masters and the CPU needs access to external memory, a single AHB bus can cause a bottleneck. ARM's solution to this was to invent a multi-layer AHB which replaces the request/grant and arbitration mechanism with a multiplexer fabric that pushes arbitration to the level of the devices. Thus, if a CPU and a DMA controller want access to the same memory, the multi-layer fabric will arbitrate between the two on granting access to that memory. This allows simultaneous access by bus masters to different resources at the cost of increased arbitration complexity. As with all trade-offs, the pros and cons must be analyzed, for a microcontroller operating at 200 MHz, removing guaranteed central arbitration in case more than one bus master is active in favor of occasional local arbitration gives better performance.

The blocks outside the CPU can be roughly split into memory controllers, serial communication, I/O, timers/counters and RTC, system control, and debug and trace blocks. These are described as follows.

6.4 On-chip SRAM

On-chip SRAM may be used for code and/or data storage. The SRAM may be accessed as 8-bits, 16-bits, and 32-bits. The LPC3180 provides 64 kB of SRAM.

6.5 Memory map

The LPC3180 memory map incorporates several distinct regions, as shown in Figure 3. When an application is running, the CPU interrupt vectors are re-mapped to allow them to reside in on-chip SRAM.

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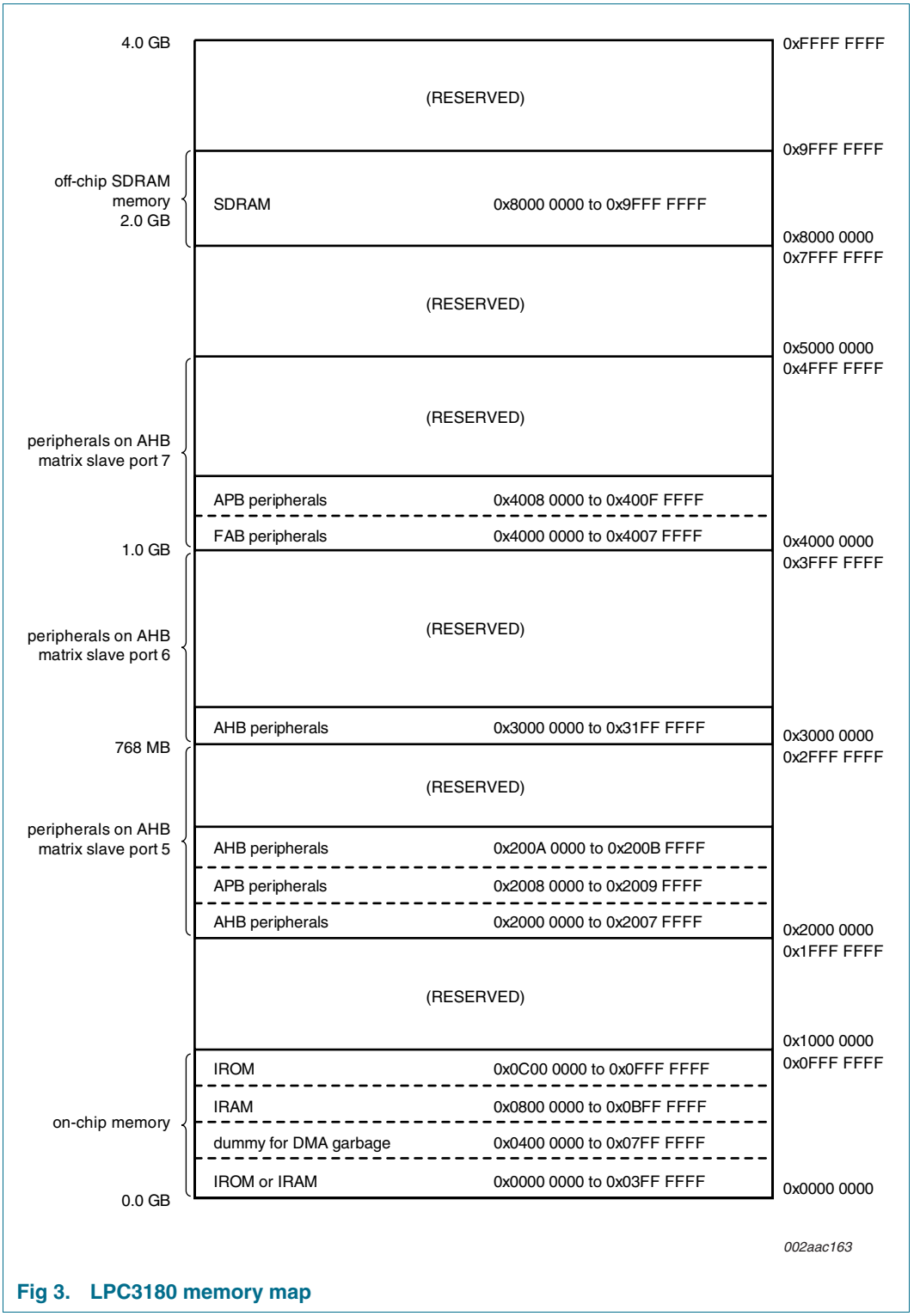

Fig 3. LPC3180 memory map

6.6 SDRAM memory controller

The SDRAM memory controller provides an interface between the system bus and external (off-chip) memory devices. A single chip select is supplied, supporting one group of SDRAM in the same address range. The SDRAM controller supports SDR SDRAM

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devices of 64, 128, 256, 512, or 1024 megabits in size, as well as DDR SDRAM devices of 64, 128, 256, 512, or 1024 megabits in size. The SDRAM controller uses four data ports to allow simultaneous requests from multiple on-chip AHB bus masters.

6.7 NAND flash controllers

The LPC3180 includes two NAND flash controllers, one for multi-level NAND flash devices and one for single-level NAND flash devices. The two NAND flash controllers use the same pins to interface to external NAND flash devices, so only one interface is active at a time.

6.7.1 Multi-level cell (MLC) NAND flash controller

The MLC NAND flash controller interfaces to either multi-level or single-level NAND flash devices. An external NAND flash device is used to allow the bootloader to automatically load a portion of the application code into internal SRAM for execution following reset.

The MLC NAND flash controller supports up to 2 Gbit devices with small (528 byte) or large (2114 byte) pages. Programmable NAND timing parameters allow support for a variety of NAND flash devices. A built-in Reed-Solomon encoder/decoder provides error detection and correction capability. A 528 byte data buffer reduces the need for CPU supervision during loading. The MLC NAND flash controller also provides DMA support.

6.7.2 Single-level NAND flash controller (SLC)

The SLC NAND flash controller interfaces to single-level NAND flash devices up to 2 Gbits in size. DMA page transfers are supported, including a 20 byte DMA read and write FIFO. Hardware support for ECC (Error Checking and Correction) is included for the main data area. Software can correct a single bit error.

6.8 DMA controller

The DMA controller allows peripheral-to memory, memory-to-peripheral, peripheral-to-peripheral, and memory-to-memory transactions. Each DMA stream provides unidirectional serial DMA transfers for a single source and destination. For example, a bidirectional port requires one stream for transmit and one for receives. The source and destination areas can each be either a memory region or a peripheral, and can be accessed through the same AHB master or one area by each master.

The DMA controls eight DMA channels with hardware prioritization. The DMA controller interfaces to the system via two AHB bus masters, each with a full 32-bit data bus width. DMA operations may be set up for 8, 16, and 32-bit data widths, and can be either big-endian or little-endian. Incrementing or non-incrementing addressing for source and destination are supported, as well as programmable DMA burst size. Scatter or gather DMA is supported through the use of linked lists. This means that the source and destination areas do not have to occupy contiguous areas of memory.

6.9 Interrupt controller

The interrupt controller is comprised of three basic interrupt controller blocks, supporting a total of 60 interrupt sources. Each interrupt source can be individually enabled/disabled and configured for high or low level triggering, or rising or falling edge triggering. Each interrupt may also be steered to either the FIQ or IRQ input of the ARM9. Raw interrupt

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status and masked interrupt status registers allow versatile condition evaluation. In addition to peripheral functions, each of the six general purpose input/output pins and 12 general purpose input pins are connected directly to the interrupt controller.

6.10 General purpose parallel I/O

Some device pins that are not dedicated to a specific peripheral function have been designed to be general purpose inputs, outputs, or I/Os. Also, some pins may be configured either as a specific peripheral function or a general purpose input, output, or I/O. A total of 55 pins can potentially be used as general purpose input/outputs, general purpose outputs, and general purpose inputs.

GPIO pins may be dynamically configured as inputs or outputs. Separate registers allow setting or clearing any number of GPIO and GPO outputs controlled by that register simultaneously. The value of the output register for standard GPIOs and GPO pins may be read back, as well as the current actual state of the port pins.

There are 12 GPI, 24 GPO, and six GPIO pins. When the SDRAM bus is configured for 16 data bits, 13 of the remaining SDRAM data pins may be used as GPIOs.

6.10.1 Features

- Bit-level set and clear registers allow a single instruction set or clear of any number of bits in one port.
- A single register selects direction for pins that support both input and output modes.
- Direction control of individual bits.
- For input/output pins, both the programmed output state and the actual pin state can be read.
- There are a total of 12 general purpose inputs, 24 general purpose outputs, and six general purpose input/outputs.
- Additionally, 13 SDRAM data lines may be used as GPIOs if a 16-bit SDRAM interface is used (rather than a 32-bit interface).

6.11 10-bit ADC

The ADC is a three channel, 10-bit successive approximation ADC. The ADC may be configured to produce results with a resolution anywhere from 10-bits to 3-bits. When high resolution is not needed, lowering the resolution can substantially reduce conversion time.

The analog portion of the ADC has its own power supply to enhance the low noise characteristics of the converter. This voltage is only supplied internally when the core has voltage. However, the ADC block is not affected by any difference in ramp-up time for VDDad and VDDcore voltage supplies.

6.11.1 Features

- Measurement range of 0 V to VDDts (nominally 3 V).
- Low noise ADC.
- Maximum 10-bit resolution, resolution can be reduced to any amount down to 3 bits for faster conversion.
- Three input channels.

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- Uses 32 KHz RTC clock

6.12 USB interface

The LPC3180 supports USB in either Device, Host, or OTG configuration.

6.12.1 USB device controller

The USB device controller enables 12 Mb/s data exchange with a USB host controller. It consists of register interface, serial interface engine, endpoint buffer memory and DMA controller. The serial interface engine decodes the USB data stream and writes data to the appropriate end point buffer memory. The status of a completed USB transfer or error condition is indicated via status registers. An interrupt is also generated if enabled. The DMA controller when enabled transfers data between the endpoint buffer and the USB RAM.

6.12.1.1 Features

- Fully compliant with USB 2.0 Full-speed specification.
- Supports 32 physical (16 logical) endpoints.
- Supports Control, Bulk, Interrupt and Isochronous endpoints.
- Scalable realization of endpoints at run time.
- Endpoint Maximum packet size selection (up to USB maximum specification) by software at run time.
- RAM message buffer size based on endpoint realization and maximum packet size.
- Supports bus-powered capability with low suspend current.
- Supports DMA transfer on all non-control endpoints.
- One Duplex DMA channel serves all endpoints.
- Allows dynamic switching between CPU controlled and DMA modes.
- Double buffer implementation for Bulk & Isochronous endpoints.

6.12.2 USB host controller

The host controller enables data exchange with various USB devices attached to the bus. It consists of register interface, serial interface engine and DMA controller. The register interface complies to the OHCI specification.

6.12.2.1 Features

- OHCI compliant.
- OpenHCI specifies the operation and interface of the USB Host Controller and SW Driver.
- The Host Controller has four USB states visible to the SW Driver:
  - USBOperational: Process Lists and generate SOF Tokens.
  - USBReset: Forces reset signaling on the bus, SOF disabled.
  - USBSuspend: Monitor USB for wakeup activity.
  - USBResume: Forces resume signaling on the bus.
- HCCA register points to Interrupt and Isochronous Descriptors List.

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- ControlHeadED and BulkHeadED registers point to Control and Bulk Descriptors List.

6.12.3 USB OTG controller

USB OTG (On-The-Go) is a supplement to the USB 2.0 specification that augments the capability of existing mobile devices and USB peripherals by adding host functionality for connection to USB peripherals.

6.12.3.1 Features

- Fully compliant with On-The-Go supplement to the USB Specification 2.0 Revision 1.0.
- Supports Host Negotiation Protocol (HNP) and Session Request Protocol (SRP) for dual-role devices under software control. HNP is partially implemented in hardware.
- Provides programmable timers required for HNP and SRP.
- Supports slave mode operation through AHB slave interface.
- Supports the OTG ATX from Philips (ISP 1301) or any external CEA-2011OTG specification compliant ATX.

6.13 UARTs

The LPC3180 contains seven UARTs. Four are standard UARTs, and three are special purpose high-speed UARTs.

6.13.1 Standard UARTs

The four standard UARTs are downwards compatible with the INS16Cx50. These UARTs support rates up to 460800 bps from a 13 MHz peripheral clock.

6.13.1.1 Features

- Each standard UART has 64 byte Receive and Transmit FIFOs.
- Receiver FIFO trigger points at 16, 32, 48, and 60 bytes.
- Transmitter FIFO trigger points at 0, 4, 8, and 16 bytes.
- Register locations conform to ‘550 industry standard.
- Each standard UART has a fractional rate pre-divider and an internal baud rate generator.
- The standard UARTs support three clocking modes: on, off, and auto-clock. The auto-clock mode shuts off the clock to the UART when it is idle.
- UART 6 includes an IrDA mode to support infrared communication.
- The standard UARTs are designed to support data rates of 2400, 4800, 9600, 19200, 38400, 57600, 115200, 230400, and 460800 bps.
- Each UART includes an internal loopback mode.

6.13.2 High-speed UARTs

The three high-speed UARTs are designed to support rates up to 921600 bps from a 13 MHz peripheral clock, for on-board communication in low noise conditions. This is accomplished by changing the oversampling from 16× to 14×, and altering the rate generation logic.

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6.13.2.1 Features

- Each high-speed UART has 64 byte Receive and Transmit FIFOs.
- Receiver FIFO trigger points at 1, 4, 8, 16, 32, and 48 bytes.
- Transmitter FIFO trigger points at 0, 4, and 8 bytes.
- Each high-speed UART has an internal baud rate generator.
- The high-speed UARTs are designed to support data rates of 2400, 4800, 9600, 19200, 38400, 57600, 115200, 230400, 460800, and 921600 bps.
- Each UART includes an internal loopback mode.

6.14 I^2C-bus serial I/O controller

There are two I^2C interfaces in the LPC3180. These I^2C blocks are a master only implementation supporting the 400 kHz I^2C mode and lower rates, with 7-bit slave addressing. Each has a four word FIFO for both transmit and receive. An interrupt signal is available from each block.

6.14.1 Features

- The two I^2C blocks are standard I^2C compliant bus interfaces that may be used in Single Master mode only.
- Programmable clock to allow adjustment of I^2C transfer rates.
- Bidirectional data transfer.
- Serial clock synchronization allows devices with different bit rates to communicate via one serial bus.
- Serial clock synchronization can be used as a handshake mechanism to suspend and resume serial transfer.

6.15 SPI serial I/O controller

The LPC3180 has two Serial Peripheral Interfaces (SPI). The SPI is a 3-wire serial interface that is able to interface with a large range of serial peripheral or memory devices (SPI mode 0 to 3 compatible slave devices).

Only a single master and a single slave can communicate on the interface during a given data transfer. During a data transfer the master always sends a byte of data to the slave, and the slave always sends a byte of data to the master. The SPI implementation on the LPC3180 does not support operation as a slave.

6.15.1 Features

- Supports slaves compatible with SPI modes 0 to 3.
- Half duplex synchronous transfers.
- DMA support for data transmit and receive.
- 1 to 16-bit word length.
- Choice of LSB or MSB first data transmission.
- 64 × 16-bit input or output FIFO.
- Bit rates up to 52 Mbits per second.

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- Busy input function.
- DMA time out interrupt to allow detection of end of reception when using DMA.
- Timed interrupt to facilitate emptying the FIFO at the end of a transmission.
- SPI clock and data pins may be used as general purpose pins if the SPI is not used.

6.16 SD card controller

The SD interface allows access to external SD memory cards. The SD card interface conforms to the SD Memory Card Specification Version 1.01.

6.16.1 Features

- Conformance to the SD Memory Card Specification Version 1.01.
- DMA is supported through the system DMA Controller.
- Provides all functions specific to the SD memory card. These include the clock generation unit, power management control, command and data transfer.

6.17 Keyboard scan

The keyboard scan function can automatically scan a keyboard of up to 64 keys in an 8×8 matrix. In operation, the keyboard scanner's internal state machine will normally be in an idle state, with all KEY_ROW[n] pins set high, waiting for a change in the column inputs to indicate that one or more keys have been pressed.

When a keypress is detected, the matrix is scanned by setting one output pin high at a time and reading the column inputs. After de-bouncing, the keypad state is stored and an interrupt is generated. The keypad is then continuously scanned waiting for 'extra key pressed' or 'key released'. Any new keypad state is scanned and stored into the matrix registers followed by a new interrupt request to the interrupt controller. It is possible to detect and separate up to 64 multiple keys pressed.

6.17.1 Features

- Supports up to 64 keys in 8×8 matrix.
- Programmable debounce period.
- A key press can wake up the CPU from stop mode.

6.18 High-speed timer

The high-speed timer block is clocked by the main peripheral clock. The clock is first divided down in a 16-bit programmable prescale counter which clocks a 32-bit Timer/Counter.

The high-speed timer includes three match registers that are compared to the Timer/Counter value. A match can generate an interrupt and cause the Timer/Counter to either continue to run, stop, or be reset. The high-speed timer also includes two capture registers that can take a snapshot of the Timer/Counter value when an input signal transitions. A capture event may also generate an interrupt.

6.18.1 Features

- 32-bit Timer/Counter with programmable 16-bit prescaler.

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- Counter or Timer operation.
- Two 32-bit capture registers.
- Three 32-bit match registers that allow:
  - Continuous operation with optional interrupt generation on match.
  - Stop timer on match with optional interrupt generation.
  - Reset timer on match with optional interrupt generation.
- Pause control to stop counting when core is in debug state.

6.19 Millisecond timer

The Millisecond timer is clocked by 32 kHz RTC clock, so a prescaler is not needed to obtain a lower count rate.

The millisecond timer includes three match registers that are compared to the Timer/Counter value. A match can generate an interrupt and the cause the Timer/Counter either continue to run, stop, or be reset.

6.19.1 Features

- 32-bit Timer/Counter, running from the 32 kHz RTC clock.
- Counter or Timer operation.
- Three 32-bit match registers that allow:
  - Continuous operation with optional interrupt generation on match.
  - Stop timer on match with optional interrupt generation.
  - Reset timer on match with optional interrupt generation.
- Pause control to stop counting when core is in debug state.

6.20 Watchdog timer

The watchdog timer block is clocked by the main peripheral clock, which clocks a 32-bit counter. A match register is compared to the Timer. When configured for watchdog functionality, a match drives the match output low. The match output is gated with an enable signal that gives the opportunity to generate two type of reset signal: one that only resets chip internally, and another that goes through a programmable pulse generator before it goes to the external pin RESOUT_N and to the internal chip reset.

6.20.1 Features

- Programmable 32-bit timer.
- Internally resets the device if not periodically reloaded.
- Flag to indicate that a Watchdog reset has occurred.
- Programmable watchdog pulse output on RESOUT_N pin.
- Can be used as a standard timer if watchdog is not used.
- Pause control to stop counting when core is in debug state.

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6.21 RTC

The RTC runs at 32768 Hz using a very low power oscillator. The RTC counts seconds and can generate alarm interrupts that can wake up the device from STOP mode. The RTCCLK can also clock the 397x PLL, the Millisecond Timer, the ADC, the Keyboard Scanner and the PWMs. The RTC up-counter value represents a number of seconds elapsed since second 0, which is an application determined time. The RTC counter will reach maximum value after about 136 years. The RTC down-counter is initiated with all 1's.

Two 32-bit Match registers are readable and writable by the processor. A match will result in an interrupt provided that the interrupt is enabled. The ONSW output pin can also be triggered by a match event, and cause an external power supply to turn on all of the operating voltages, as a way to startup after power has been removed.

The RTC block is implemented in a separate voltage domain. The block is supplied via a separate supply pin from a battery or other power source.

The RTC block also contains 32 words (128 bytes) of very low voltage SRAM. This SRAM is able to hold its contents down to the minimum RTC operating voltage.

6.21.1 Features

- Measures the passage of time in seconds.
- 32 bit up and down seconds counters.
- Ultra Low Power design to support battery powered systems.
- Dedicated 32 KHz oscillator.
- An output pin is included to assist in waking up when the chip has had power removed to all functions except the RTC.
- Two 32 bit match registers with interrupt option.
- 32 words (128 bytes) of very low voltage SRAM.
- The RTC and Battery RAM power have an independent power domain and dedicated supply pins, which can be powered from a battery or power supply.

6.22 Pulse width modulators

The LPC3180 provides two PWMs. They are clocked separately by either the main peripheral clock or the 32 kHz RTC clock. Both PWMs have a duty cycle programmable in 255 steps.

6.22.1 Features

- Clocked by the main peripheral clock or the 32 kHz RTC clock.
- Programmable 4-bit prescaler.
- Duty cycle programmable in 255 steps.
- Output frequency up to 50 kHz when using a 13 MHz peripheral clock.

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6.23 Reset

Reset is accomplished by an active low signal on the RESET_N input pin. A reset pulse with a minimum width of 10 main oscillator clocks after the oscillator is stable is required to guarantee a valid chip reset. At power-up, 10 milliseconds should be allowed for the oscillator to start up and stabilize after Vdd reaches operational voltage. An internal reset with a minimum duration of 10 clock pulses will also be applied if the watchdog timer generates an internal device reset.

6.24 Clocking and power control

Clocking in the LPC3180 is designed to be versatile, so that system and peripheral requirements may be met, while allowing optimization of power consumption. Clocks to most functions may be turned off if not needed, some peripherals do this automatically.

The LPC3180 includes three operational modes that give control over processing speed and power consumption. In addition, clock rates to different functional blocks may be controlled by changing clock sources, re-configuring PLL values, or altering clock divider configurations. This allows a trade-off of power versus processing speed based on application requirements.

6.24.1 Crystal oscillator

The Main Oscillator is the basis for the clocks most chip functions use by default. Optionally, many functions can be clocked instead by the output of a PLL (with a fixed 397x rate multiplication) which runs from the RTC oscillator. In this mode, the Main Oscillator may be turned off unless the USB interface is enabled. If a SYSCLK frequency other than 13 MHz is required in the application, or if the USB block is not used, the main oscillator may be used with a frequency of between 1 MHz and 20 MHz.

6.24.2 PLLs

The LPC3180 includes three PLLs: one allows boosting the RTC frequency to 13.008896 MHz for use as the primary system clock; one provides the 48 MHz clock required by the USB block; and one provides the basis for the CPU clock, the AHB bus clock, and the main peripheral clock.

The first PLL multiplies the 32768 Hz RTC clock by 397 to obtain a 13.008896 MHz clock. The 397x PLL is designed for low power operation and low jitter. This PLL requires an external R/C loop filter for proper operation.

The other two PLLs accept an input clock from either the main oscillator or the output of the 397x PLL. The input frequency is multiplied up to a higher frequency, then divided down to provide the output clock.

The PLL input may initially be divided down by a pre-divider value ‘N’, which may have the values 1, 2, 3, or 4. This pre-divider can allow a greater number of possibilities for the output frequency.

Following the PLL input divider is the PLL multiplier. This can multiply the pre-divider output by a value ‘M’, in the range of 1 through 256. The resulting frequency must be in the range of 156 MHz to 320 MHz. The multiplier works by dividing the output of a Current Controlled Oscillator (CCO) by the value of M, then using a phase detector to compare the divided CCO output to the pre-divider output. The error value is used to adjust the CCO frequency.

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At the PLL output, there is a post-divider that can be used to bring the CCO frequency down to the desired PLL output frequency. The post-divider value ‘P’, can divide the CCO output by 1, 2, 4, 8, or 16. The post-divider can also be bypassed, allowing the PLL CCO output to be used directly. The maximum PLL output frequency that is supported by the CPU is 208 MHz.

6.24.3 Power control and modes

The LPC3180 supports three operational modes, two of which are specifically designed to reduce power consumption. The modes are: RUN mode, Direct RUN mode, and STOP mode.

RUN mode is the normal operating mode for applications that require the CPU, AHB bus, or any peripheral function other than the USB block to run faster than the main oscillator frequency. In RUN mode, The CPU can run at up to 208 MHz and the AHB bus can run at up to 104 MHz.

Direct RUN mode allows reducing the CPU and AHB bus rates in order to save power. Direct RUN mode can also be the normal operating mode for applications that do not require the CPU, AHB bus, or any peripheral function other than the USB block to run faster than the main oscillator frequency. Direct RUN mode is the default mode following chip reset.

STOP mode causes all CPU and AHB operation to cease, and stops clocks to peripherals other than the USB block.

6.24.4 APB bus

Many peripheral functions are accessed by on-chip APB busses that are attached to the higher speed AHB bus. The APB bus performs reads and writes to peripheral registers in three peripheral clocks.

6.24.5 FAB bus

Some peripherals are placed on a special bus called FAB that allows faster CPU access to those peripheral functions. Write accesses to FAB peripherals take a single AHB clock. Read access to FAB peripherals take two AHB clocks.

6.25 Emulation and debugging

The LPC3180 supports emulation and debugging via a dedicated JTAG serial port. An Embedded Trace Buffer allows tracing program execution. The dedicated JTAG port allows debugging of all chip features without impact to any pins that may be used in the application.

6.25.1 EmbeddedICE

Standard ARM EmbeddedICE logic provides on-chip debug support. The debugging of the target system requires a host computer running the debugger software and an EmbeddedICE protocol converter. The EmbeddedICE protocol converter converts the Remote Debug Protocol commands to the JTAG data needed to access the ARM core.

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The ARM core has a Debug Communication Channel function built-in. The debug communication channel allows a program running on the target to communicate with the host debugger or another separate host without stopping the program flow or entering the debug state.

6.25.2 Embedded trace buffer

The Embedded Trace Module (ETM) is connected directly to the ARM core. It compresses the trace information and exports it through a narrow trace port. An internal Embedded Trace Buffer of 2 k by 24-bits captures the trace information under software debugger control. Data from the Embedded Trace Buffer is recovered by the debug software through the JTAG port.

The trace contains information about when the ARM core switches between states. Instruction trace (or PC trace) shows the flow of execution of the processor and provides a list of all the instructions that were executed. Instruction trace is significantly compressed by only broadcasting branch addresses as well as a set of status signals that indicate the pipeline status on a cycle by cycle basis. For data accesses either data or address or both can be traced.

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7. Limiting values

Table 4: Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). [1]

Symbol	Parameter	Conditions	Min	Max	Unit
$V_{DD\ (1.2V)}$ [2]	core, PLL, oscillator, and RTC supplies		−0.5	+1.3	V
$V_{DD\ (1.8V)}$ [3]	I/O pad supply		−0.5	+1.95	V
$V_{DD\ (3V)}$ [4]	I/O pad supply		−0.5	+3.6	V
$V_{DD\ (analog\ 3V)}$ [5]	ADC supply		−0.5	3.3	V
$V_{DD\ (1.8V\ or\ 3V)}$ [6]	I/O pad supply		−0.5	+3.6	V
V_{IA}	analog input voltage		−0.5	**<tbd>**	V
V_I	input voltage [7] [8]		−0.5	**<tbd>**	V
	input voltage [7] [9]		−0.5	**<tbd>**	V
I_{DD}	supply current [10]		**<tbd>**	**<tbd>**	mA
I_{SS}	DC ground current per ground pin		**<tbd>**	**<tbd>**	mA
T_{stg}	storage temperature		−40	125	°C
$P_{tot(pack)}$	total power dissipation (per package)	based on package heat transfer, not device power consumption		**<tbd>**	W

[1] The following applies to Table 4:

a) This product includes circuitry specifically designed for the protection of its internal devices from the damaging effects of excessive static charge. Nonetheless, it is suggested that conventional precautions be taken to avoid applying greater than the rated maximum.

b) Parameters are valid over operating temperature range unless otherwise specified. All voltages are with respect to V_{SS} unless otherwise noted.

[2] Applies to pins VDDcore12_01 to VDDcore12_08, Vddcorefixed_01 to Vddcorefixed_02, VDDosc12, VDDpll397-12, VDDpllHCLK-12, VDDpllUSB-12, VDDrtc12, VDDrtccore12, VDDrtsosc12, and VDD12.

[3] Applies to pins VDDio18_01 to VDDio18_04 and VDDsdram18_01 to VDDsdram18_09.

[4] Applies to pins VDDio28_01 to VDDio28_02 and VDD28.

[5] Applies to VDDad28 pins.

[6] Applies to pins VDDio1828_01 to VDDio1828_012 and VDD1828.

[7] Including voltage on outputs in 3-state mode.

[8] 1.8 V pins.

[9] 3 V pins.

[10] Per supply pin.

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8. Static characteristics

Table 5: Static characteristics

T_a = −40 °C to +85 °C, unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ [1]	Max	Unit
$V_{DD\ (1.2V)}$ [2]	core supply voltage for full performance	full frequency range		1.1	1.2	1.3	V
$V_{DD\ (1.2V)}$ [2]	core supply voltage for reduced power	up to 14 MHz CPU		0.9		1.3	V
$V_{DD\ (1.2V)}$ [3]	RTC supply voltage			0.9		1.3	V
$V_{DD\ (1.2V)}$ [4]	PLL and oscillator supplies			1.1	1.2	1.3	V
$V_{DD\ (1.8V)}$ [5]	external 1.8 V supply voltage			1.7	1.8	1.95	V
$V_{DD\ (3V)}$ [6]	external 3 V supply voltage			2.7	3	3.3	V
$V_{DD\ (analog\ 3V)}$ [7]	ADC supply voltage			2.7	3	3.3	V
$V_{DD\ (1.8V\ or\ 3V)}$ [8]	external 1.8 V/3 V supply voltage			1.7/2.7	1.8/3	3.3	V
I_{IL}	LOW-state input current	V_I = 0 V; no pull-up		-	-	3	µA
I_{IH}	HIGH-state input current	$V_I = V_{DD}$; no pull-down	[9]	-	-	3	µA
I_{OZ}	3-state output leakage current	V_O = 0 V; $V_O = V_{DD}$; no pull-up/down	[9]	-	-	3	µA
I_{latch}	I/O latch-up current	$-(1.5V_{DD}) < V < (1.5V_{DD})$	[9]	-	-	100	mA
V_I	input voltage		[9] [10] [11] [12]	0	-	V_{DD}	V
V_{IH}	HIGH-state input voltage, 1.8 V inputs			1.6	-	-	V
	HIGH-state input voltage, 3 V inputs			2.0	-	-	V
V_{IL}	LOW-state input voltage, 1.8 V inputs			-	-	0.6	V
	LOW-state input voltage, 3 V inputs			-	-	0.8	V
V_{OH}	HIGH-state output voltage, 1.8 V outputs [13]	I_{OH} = −1 mA		V_{DD} − 0.4	-	-	V
	HIGH-state output voltage, 3 V outputs [13]	I_{OH} = −4 mA		V_{DD} − 0.4	-	-	V
V_{OL}	LOW-state output voltage, 1.8 V outputs [13]	I_{OL} = 4 mA		-	-	0.4	V
	LOW-state output voltage, 3 V outputs [13]	I_{OL} = 4 mA		-	-	0.4	V
I_{OH}	HIGH-state output current [13]	$V_{OH} = V_{DD}$ − 0.4 V	[9]	-	−4	-	mA
I_{OL}	LOW-state output current [13]	V_{OL} = 0.4 V	[9]	-	4	-	mA
I_{OHS}	HIGH-state short circuit current [14]	V_{OH} = 0 V		-	−45	-	mA
I_{OLS}	LOW-state short circuit current [14]	$V_{OL} = V_{DD}$	[9]	-	45	-	mA

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Table 5: Static characteristics *…continued*

T_a = −40 °C to +85 °C, unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ [1]	Max	Unit
I_{DD}	RUN mode power supply current	VDDcore12 = 1.2 V; T_a = 25 °C; I-cache enabled; CPU clock = 208 MHz; all peripherals enabled	-	80	-	mA
	Direct RUN mode power supply current	VDDcore12 = 0.9 V; T_a = 25 °C; CPU clock = 13 MHz	-	7	-	mA
	STOP mode power supply current	VDDcore12 = 0.9 V; T_a = 25 °C; CPU clock = stopped internally	-	-	500	µA

[1] Typical ratings are not guaranteed. The values listed are at room temperature (+25 °C), nominal supply voltages.

[2] Applies to VDDcore12_01 to VDDcore12_08 pins.

[3] Applies to pins VDDrtc12, VDDrtccore12, and VDDrtsosc12.

[4] Applies to pins Vddcorefixed_01 to Vddcorefixed_02, VDDosc12, VDDpll397-12, VDDpllHCLK-12, VDDpllUSB-12, and VDD12.

[5] Applies to pins VDDio18_01 to VDDio18_04 and VDDsdram18_01 to VDDsdram18_09.

[6] Applies to pins VDDio28_01 to VDDio28_02 and VDD28.

[7] Applies to VDDad28 pins.

[8] Applies to pins VDDio1828_01 to VDDio1828_012 and VDD1828.

[9] Referenced to the applicable VDD for the pin.

[10] Including voltage on outputs in 3-state mode.

[11] The applicable VDD voltage for the pin must be present.

[12] 3-state outputs go into 3-state mode when VDD(3V3) is grounded.

[13] Accounts for 100 mV voltage drop in all supply lines.

[14] Only allowed for a short time period.

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9. Dynamic characteristics

Table 6: Dynamic characteristics

T_a= −40 °C to +85 °C, unless otherwise specified. [1]

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
External clock						
f_{osc}	external clock frequency supplied by an external crystal		1	13	20	MHz
Port pins						
t_r	rise time		-	5	-	ns
t_f	fall time		-	5	-	ns

[1] Parameters are valid over operating temperature range unless otherwise specified.

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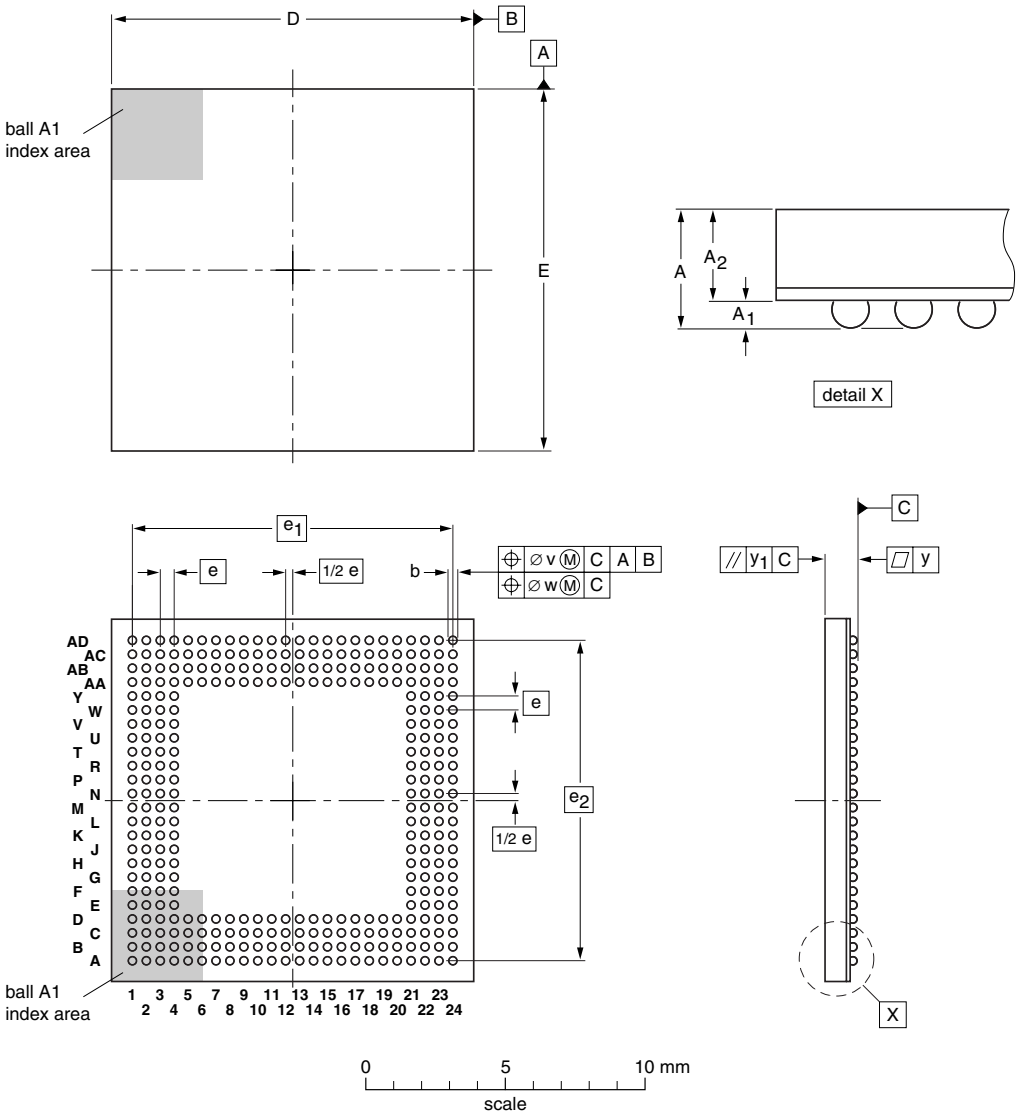
10. Package outline

LFBGA320: plastic low profile fine-pitch ball grid array package; 320 balls; body 13 x 13 x 0.9 mm SOT824-1



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	b	D	E	e	e_1	e_2	v	w	y	y_1
mm	1.3	0.3 0.2	1.0 0.8	0.35 0.25	13.1 12.9	13.1 12.9	0.5	11.5	11.5	0.15	0.05	0.08	0.1

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT824-1		- - -				03-07-09

Fig 4. Package outline SOT824-1

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11. Abbreviations

Table 7: Acronym list

Acronym	Description
ADC	Analog-to-Digital Converter
AHB	AMBA Advanced High-performance Bus
APB	AMBA Advanced Peripheral Bus
CPU	Central Processing Unit
DMA	Direct Memory Access
FAB	Fast Access Bus
FIFO	First In, First Out
GPI	General Purpose Input
GPIO	General Purpose Input/Output
GPO	General Purpose Output
OTG	USB On-The-Go
PWM	Pulse Width Modulator
RAM	Random Access Memory
SDRAM	Synchronous Dynamic Random Access Memory
SPI	Serial Peripheral Interface
UART	Universal Asynchronous Receiver/Transmitter
USB	Universal Serial Bus

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12. Revision history

Table 8: Revision history

Document ID	Release date	Data sheet status	Change notice	Doc. number	Supersedes
LPC3180_1	20060217	Preliminary data sheet	-	-	-

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13. Data sheet status

Level	Data sheet status [1]	Product status [2] [3]	Definition
I	Objective data	Development	This data sheet contains data from the objective specification for product development. Philips Semiconductors reserves the right to change the specification in any manner without notice.
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[3] For data sheets describing multiple type numbers, the highest-level product status determines the data sheet status.

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Limiting values definition — Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 60134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

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Date of release: 21 February 2006
Document number: LPC3180_1

Published in the Netherlands