LPC29xx- Base Module

Agenda

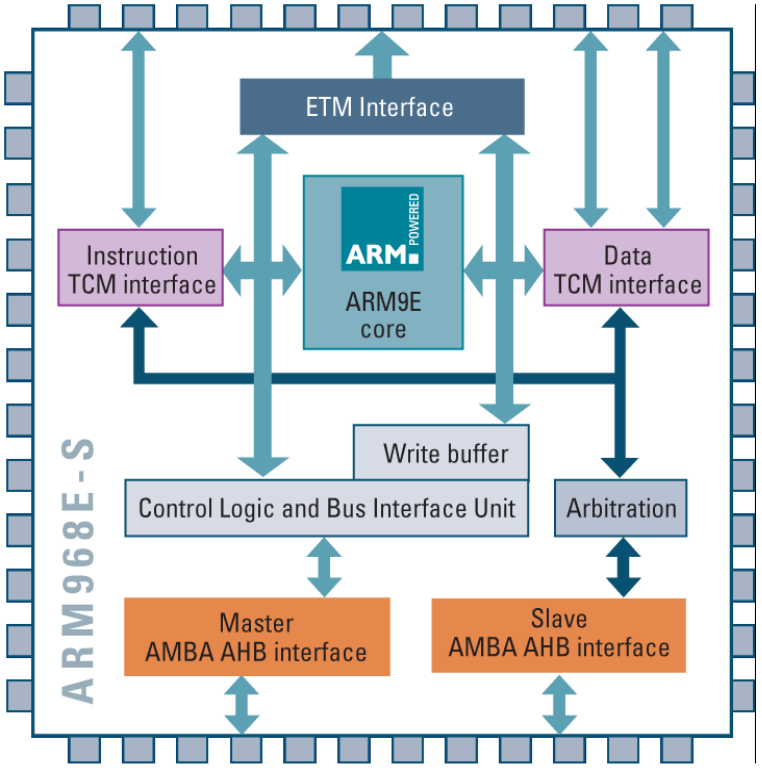
- Introduction
- Memory support
- Subsystems
  - PCR (Power Clock & Reset)
  - General (GeSS)
  - Networking (IVNSS)
  - Peripheral (PeSS)
  - Modulation and Sampling (MSCSS)
- Power modes
- DMA support
- Tools

Introduction

- ARM968E-S Overview
- LPC29xx Derivatives
- LPC29xx Block Diagram

The ARM9E Processor Family
ARM968E-S (& ARM926EJ-S)

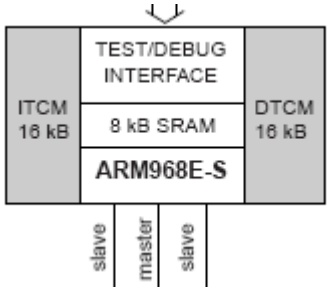
- ARMv5TE instruction set
  - DSP instructions
- Tightly Coupled Memories
  - Next slide
- ETM9 interface



Tightly coupled memory (TCM)

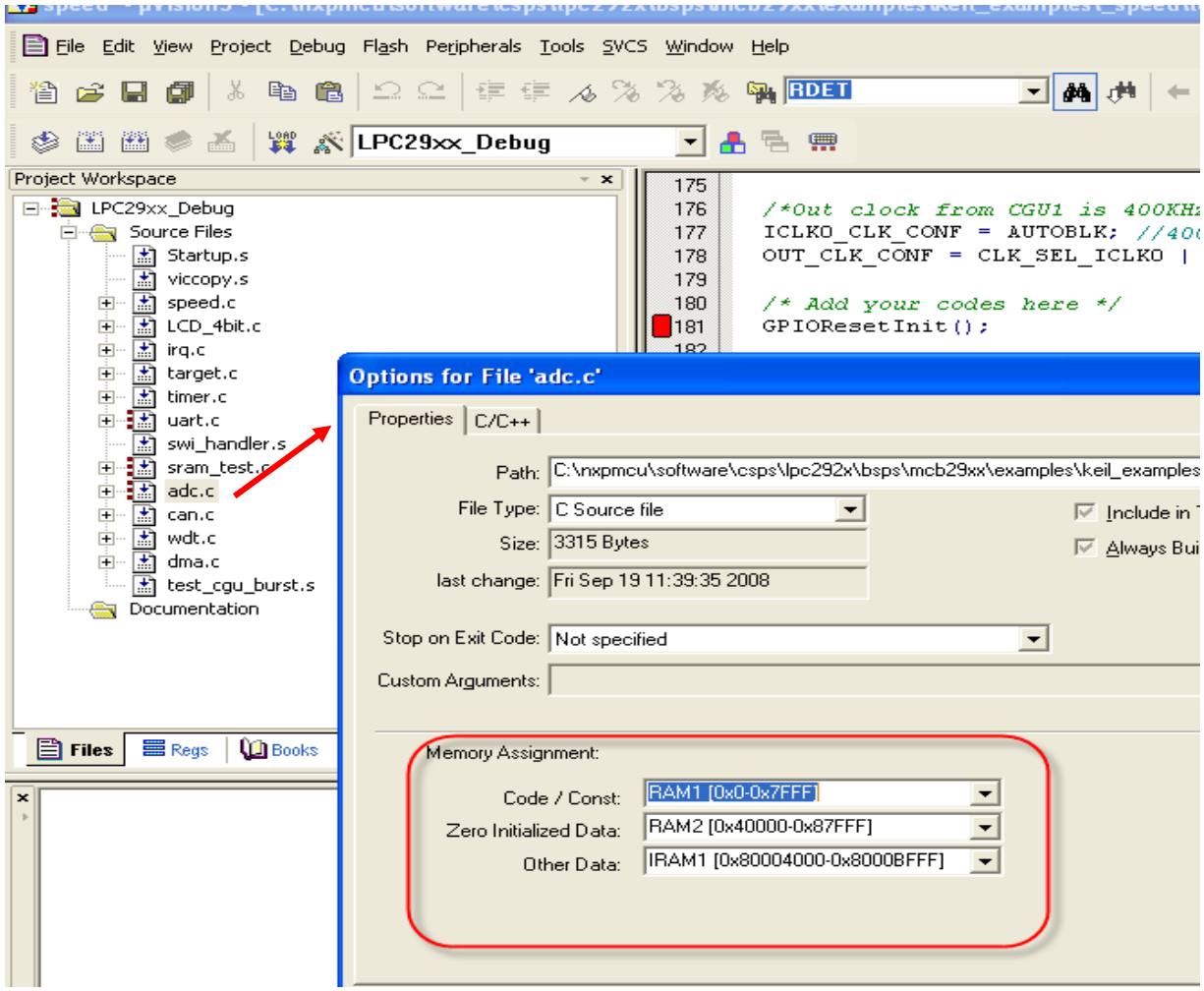
- TCM is a low-latency memory that provides predictable performance
  - TCM accesses are deterministic and do not access the AHB
  - Cache on the other hand is not predictable

- Due to its deterministic behavior, TCM can hold critical routines, such as interrupt handling routines or real-time tasks where the indeterminacy of a cache is highly undesirable



- Can easily be controlled by a small footprint embedded OS
  - Cache requires a MUCH larger OS to manage it efficiently

Configuring TCM's using Keil Tools



LPC29xx Family- An Introduction

- Industry's fastest running ARM968 running at 125MHz

- Memory support
  - On-chip SRAM and Flash, EEPROM, TCM, External Memory Interface

- Key peripherals
  - Motor control block
    - PWM, QEI, two 3.3V and one 5V ADC
  - 2 CAN controllers
  - 2 LIN controllers
  - USB FS OTG/Host/Device controllers

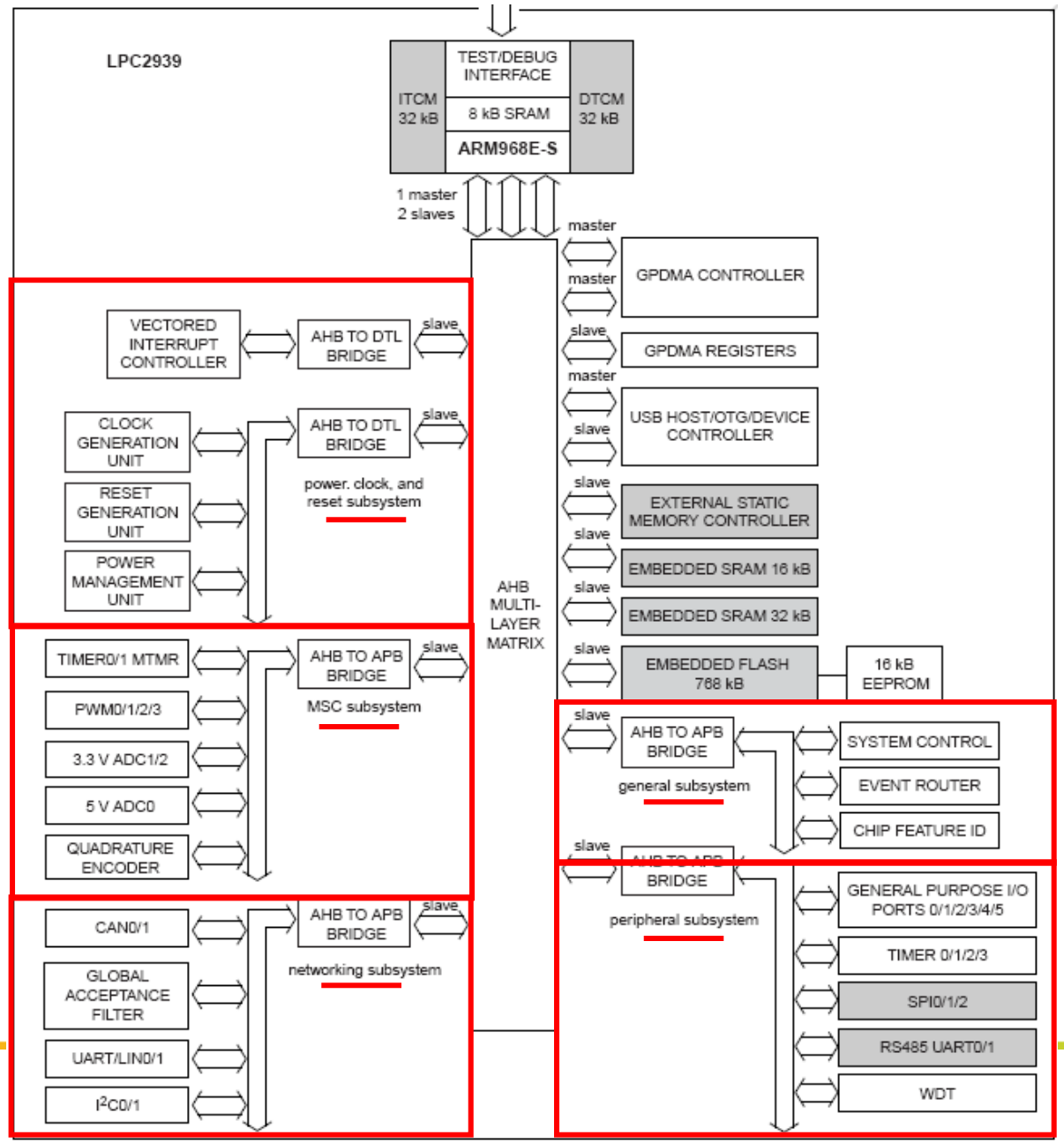
LPC29xx Derivatives

LPC29xx part overview

Part number	Flash	SRAM (incl ETB)	TCM (I/D)	CAN	LIN/ UART	Pins	UART RS485	SPI	3V3 ADC	5 V ADC	SMC	USB device	USB host	USB OTG	ETM	QEI	I2C-bus	Clkout pin
LPC2939	768 kB	56 kB	32/32 kB	2	2	208	2	3	2	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes
LPC2930	-	56 kB	32/32 kB	2	2	208	2	3	2	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes
LPC2929	768 kB	56 kB	32/32 kB	2	2	144	2	3	2	Yes	Yes	Yes	No	Yes	Yes	Yes	Yes	Yes
LPC2927	512 kB	56 kB	32/32 kB	2	2	144	2	3	2	Yes	Yes	Yes	No	Yes	Yes	Yes	Yes	Yes
LPC2925	512 kB	40 kB	16/16 kB	2	2	100	2	3	2	No	No	Yes	No	No	Yes	Yes	Yes	Yes
LPC2923	256 kB	24 kB	16/16 kB	2	2	100	2	3	2	No	No	Yes	No	No	Yes	Yes	Yes	Yes
LPC2921	128 kB	24 kB	16/16 kB	2	2	100	2	3	2	No	No	Yes	No	No	Yes	Yes	Yes	Yes
LPC2919/01	768 kB	56 kB	16/16 kB	2	2	144	2	3	2	No	Yes	No	No	No	Yes	Yes	Yes	Yes
LPC2917/01	512 kB	56 kB	16/16 kB	2	2	144	2	3	2	No	Yes	No	No	No	Yes	Yes	Yes	Yes

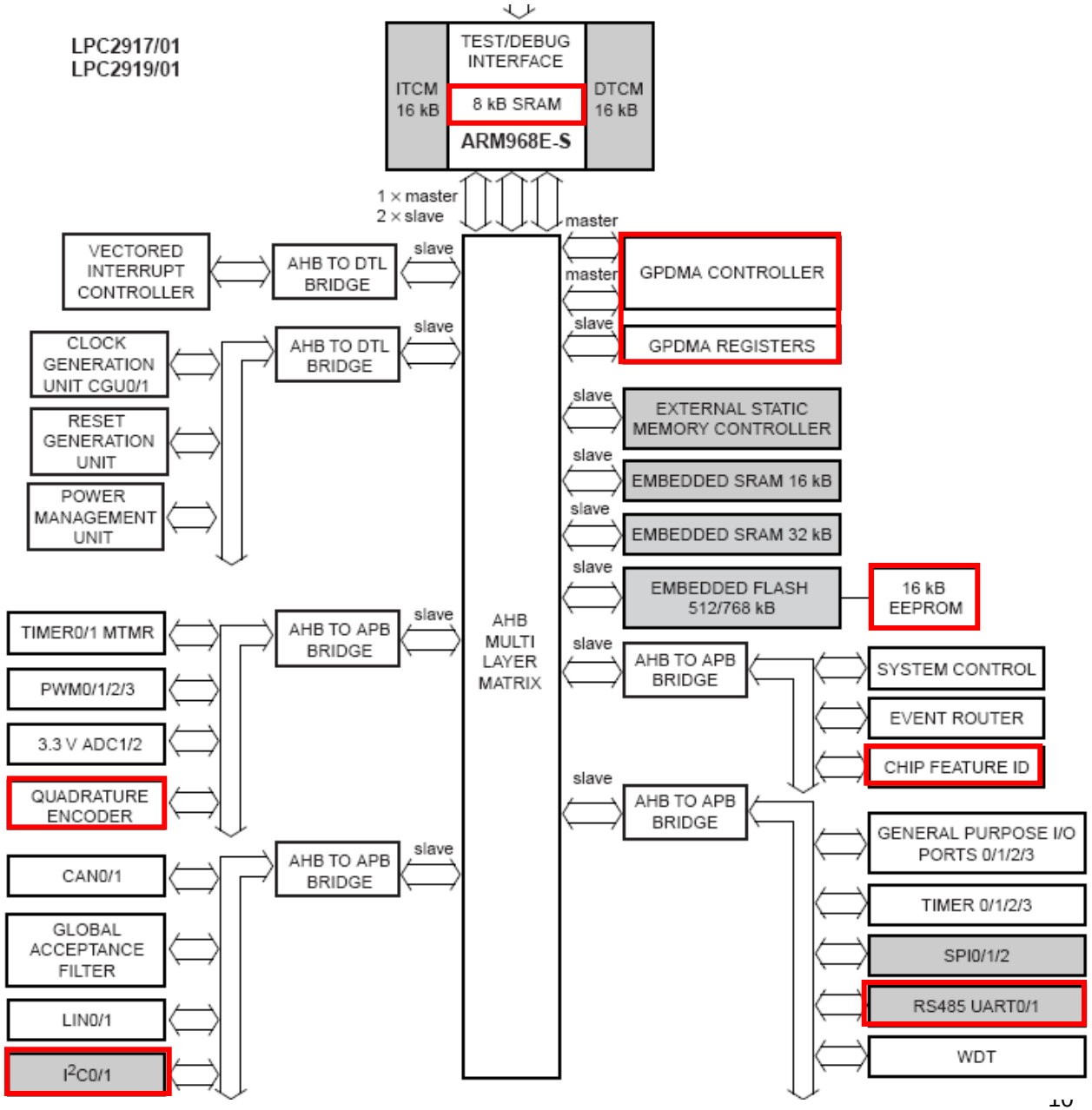
Remark: Note that parts LPC2927 and LPC2929 are not fully pin compatible with parts LPC2917/01 and LPC2919/01 or LPC2917 and LPC2919. On the LPC2927/29 the MSCSS and timer blocks have a reduced pinout.

LPC2939 Block Diagram



LPC2919/01
LPC2917/01

- 8KB ETB
- QEI
- I2C0/1
- GP DMA
- Chip Feature ID
- RS485 UARTs
- 125MHz

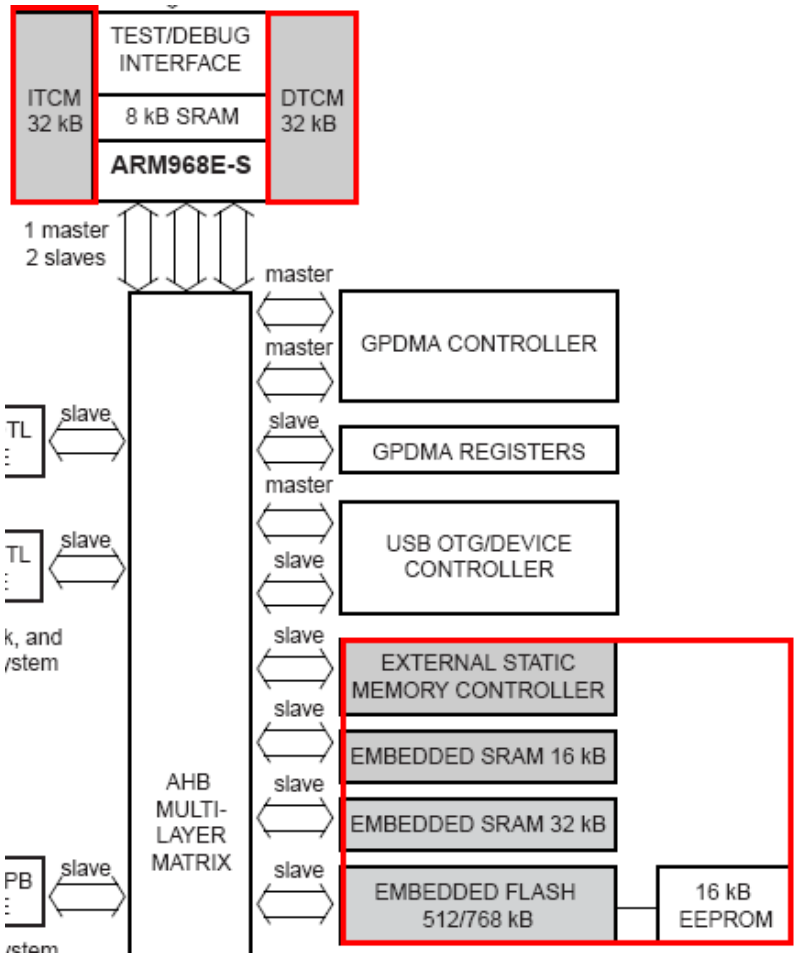


Memory Support

- SRAM
- EMC
- Flash
- EEPROM
- Booting

Overview

- 32KB or 16KB Instruction and Data TCMs
- On-chip SRAM- Up to 56KB
- On-chip Flash- Up to 768KB
- 16KB EEPROM
- 8KB ETB SRAM
- External static memory controller



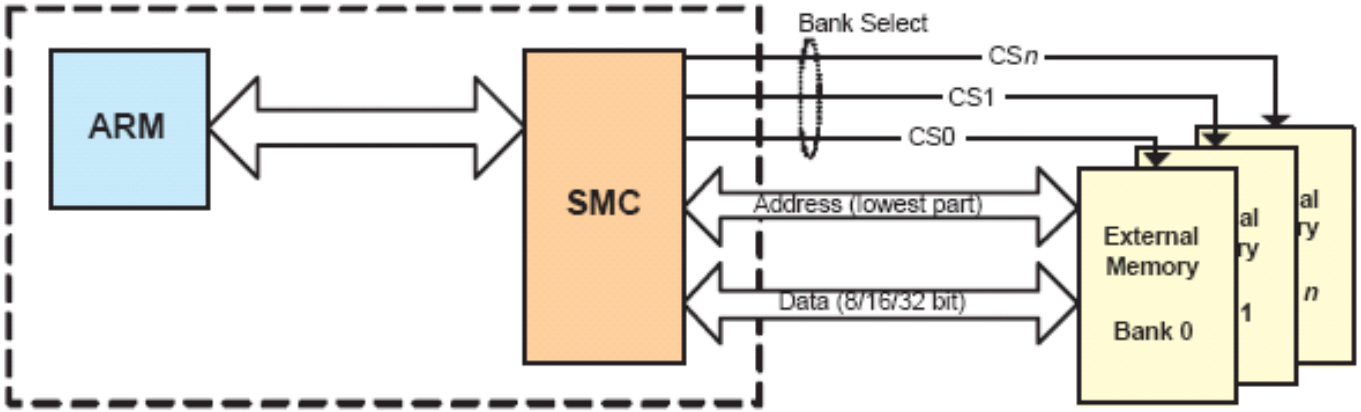
SRAM

- 56KB SRAM
  - 32 KB general purpose SRAM
  - Independent additional 16 KB SRAM
  - 8KB ETB RAM
- LPC2921, LPC2923, LPC2925
- Memory shadowing from Flash to SRAM supported enabling faster interrupt execution from SRAM

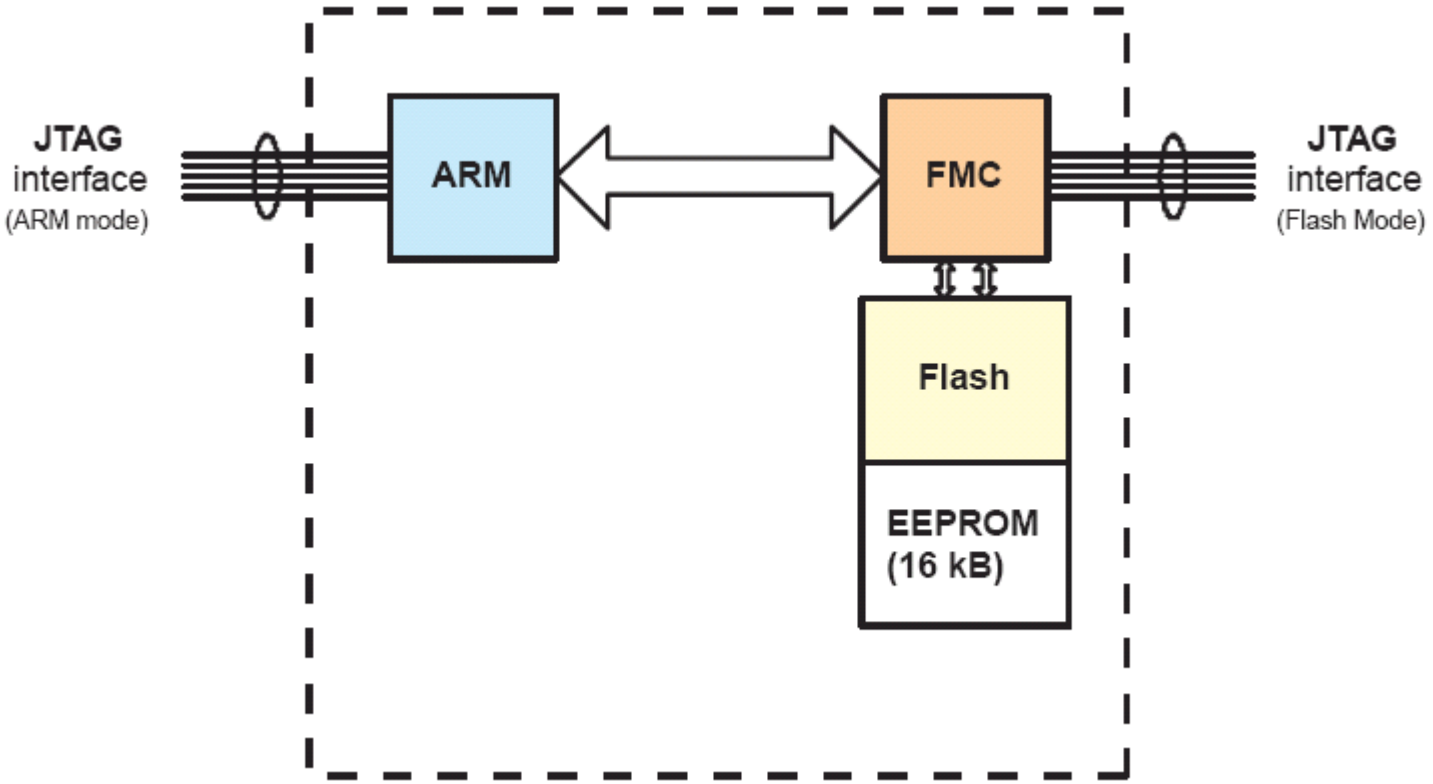
Part number	Flash	SRAM	
		SRAM (16 kB)	SRAM (32 kB)
LPC2917/01	512 kB	yes	yes
LPC2919/01	768 kB	yes	yes
LPC2921	128 kB	yes	no
LPC2923	256 kB	yes	no
LPC2925	512 kB	no	yes
LPC2927	512 kB	yes	yes
LPC2929	768 kB	yes	yes
LPC2930	-	yes	yes
LPC2939	768 kB	yes	yes

External Memory Interface

- 8 memory banks each capable of addressing 16MB
- 24-bit Address and 32-bit data bus
- Data bus configurable as 8-, 16- or 32-bit width
- Unused data bus pins become general purpose I/O

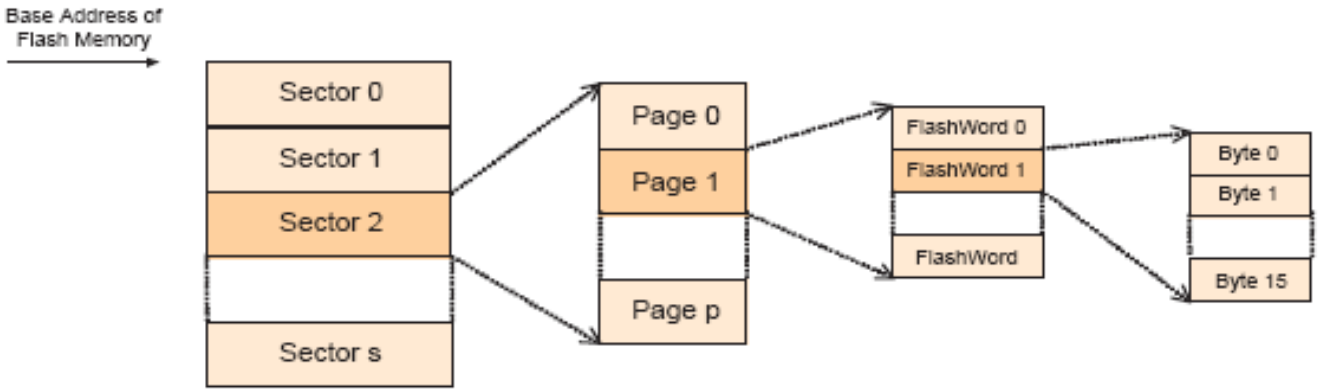


Flash Memory



Flash Operations

- Erasing: Done per sector
- Burning: Programming is done per page (smallest flash write block is 16 bytes)
- Protection
  - Sector wise write protection
  - JTAG interface can be disabled as well



Flash Features

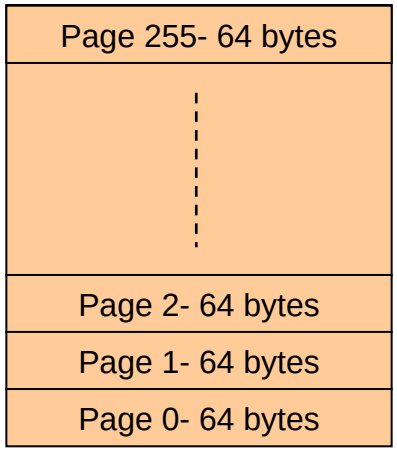
- Flash signature generation
  - 128-bit signature from a range of Flash memory
- Flash interrupts
  - END_OF_BURN, END_OF_ERASE, END_OF_MISR
- Index sector
  - JTAG access protection
  - Storage of customer information
  - Sector security
- Flash endurance- 100K cycles (-25˚C to 85˚C)
- Flash retention- 10 years (<100K cycles @ -40˚C to 85˚C)

EEPROM

- 256 pages= 16KB

- Prerequisites for EEPROM operations
  - Minimum operating voltage= 1.5V
  - Need a 375kHz clock for erase/program operations

- EEPROM and Flash are independent modules



16KB EEPROM

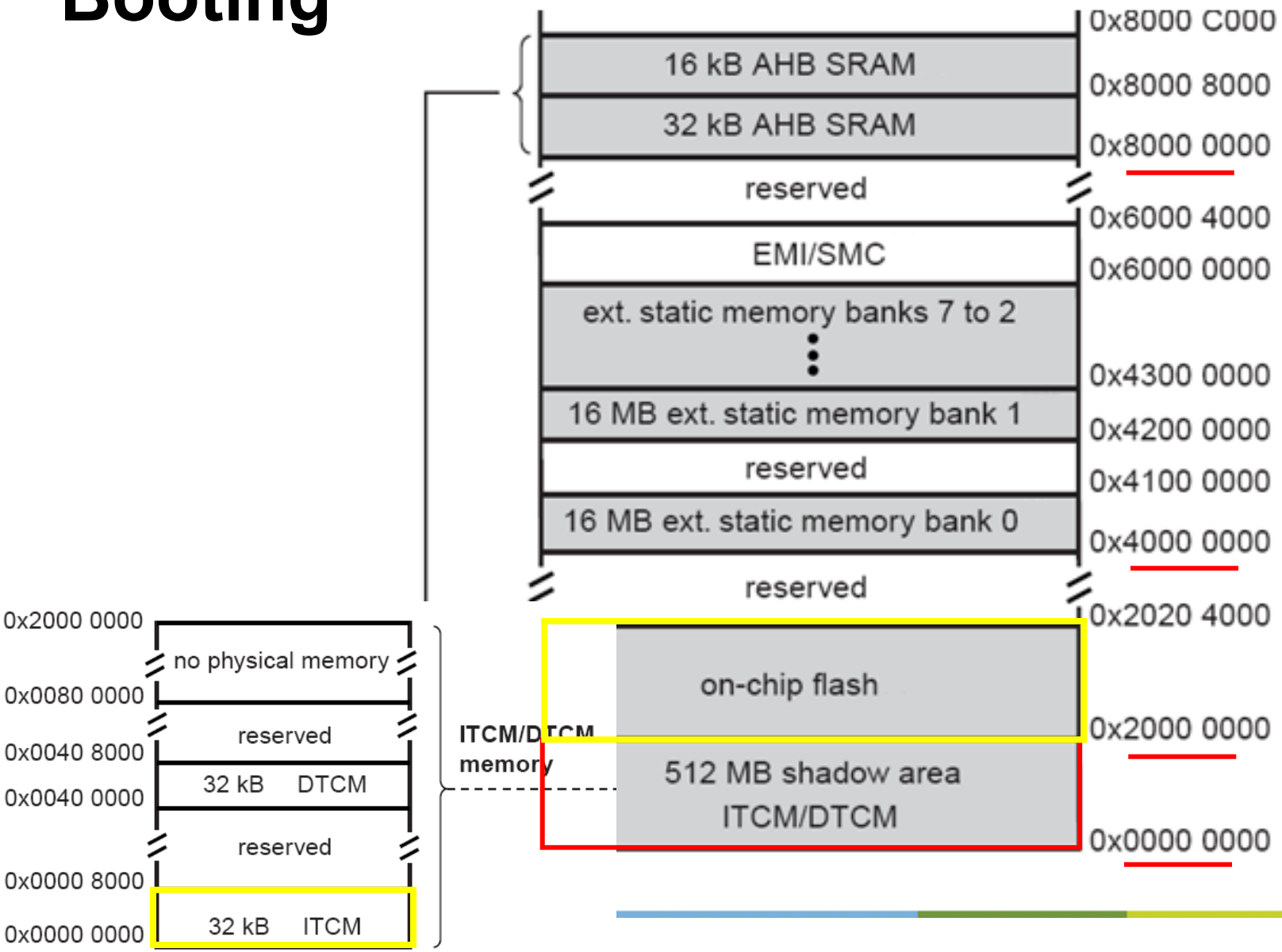
EEPROM Operations

- 8-bit, 16-bit and 32-bit read operations
- 8-bit, 16-bit and 32-bit write operations
- Erase/program page
- BIST operation supported that would lead to 2 16-bit signatures
- The EEPROM can be powered down

Memory Regions

Memory region #	Address	Description
0	0x0000 0000	TCM area and shadow area
1	0x2000 0000	embedded flash area
2	0x4000 0000	external static memory area
3	0x6000 0000	external static memory controller area
4	0x8000 0000	internal SRAM area
5	0xA000 0000	not used
6	0xC000 0000	not used
7	0xE000 0000	bus-peripherals area

Booting


0x8000 C000
16 kB AHB SRAM
0x8000 8000
32 kB AHB SRAM
0x8000 0000
reserved
0x6000 4000
EMI/SMC
0x6000 0000
ext. static memory banks 7 to 2
0x4300 0000
16 MB ext. static memory bank 1
0x4200 0000
reserved
0x4100 0000
16 MB ext. static memory bank 0
0x4000 0000
reserved
0x2020 4000
on-chip flash
0x2000 0000
512 MB shadow area
ITCM/DTCM
0x0000 0000
0x2000 0000
no physical memory
0x0080 0000
reserved
0x0040 8000
32 kB DTCM
0x0040 0000
reserved
0x0000 8000
32 kB ITCM
0x0000 0000
ITCM/DTCM
memory

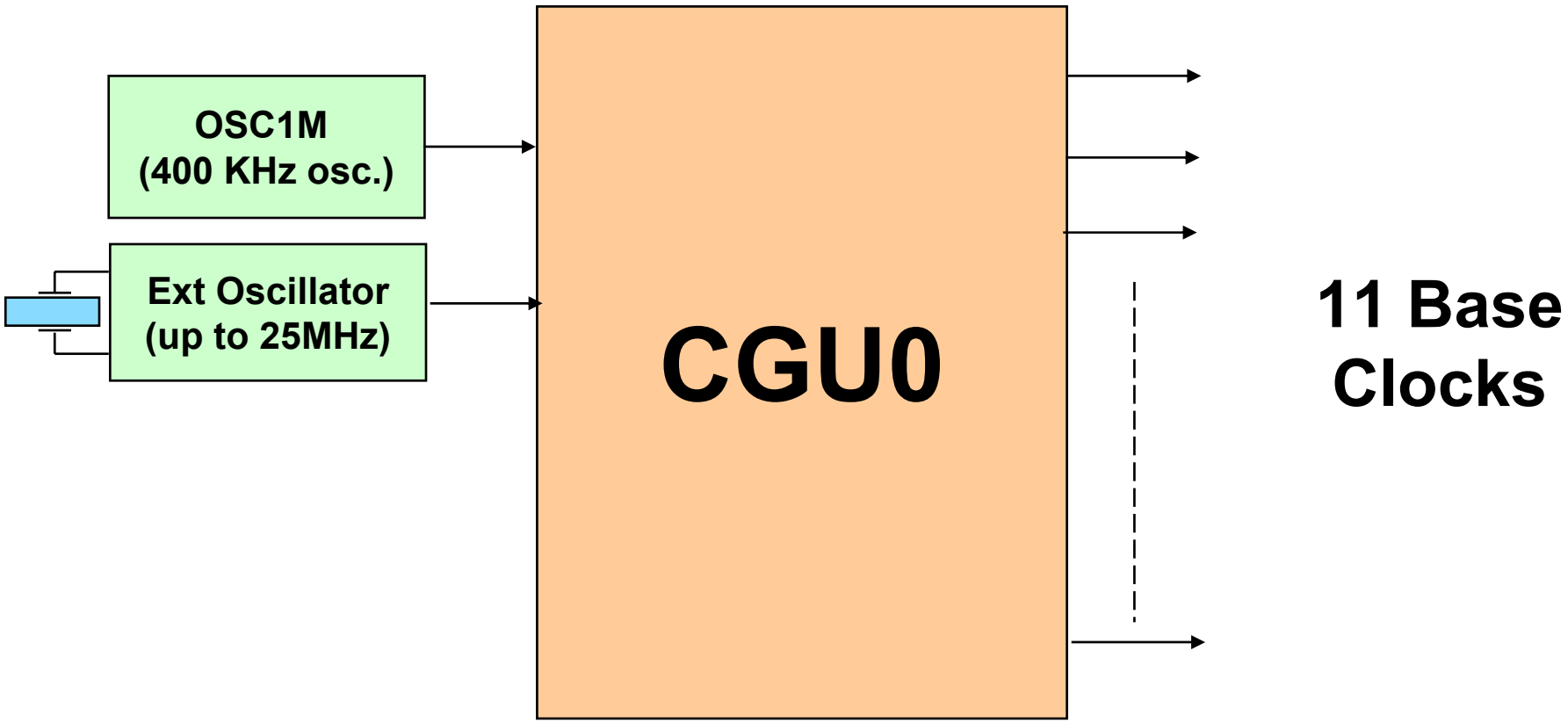
Power, Clock & Reset Subsystem (PCRSS)

- Clock Generation Unit (CGU)
- Reset Generation Unit (RGU)
- Power Management Unit (PMU)

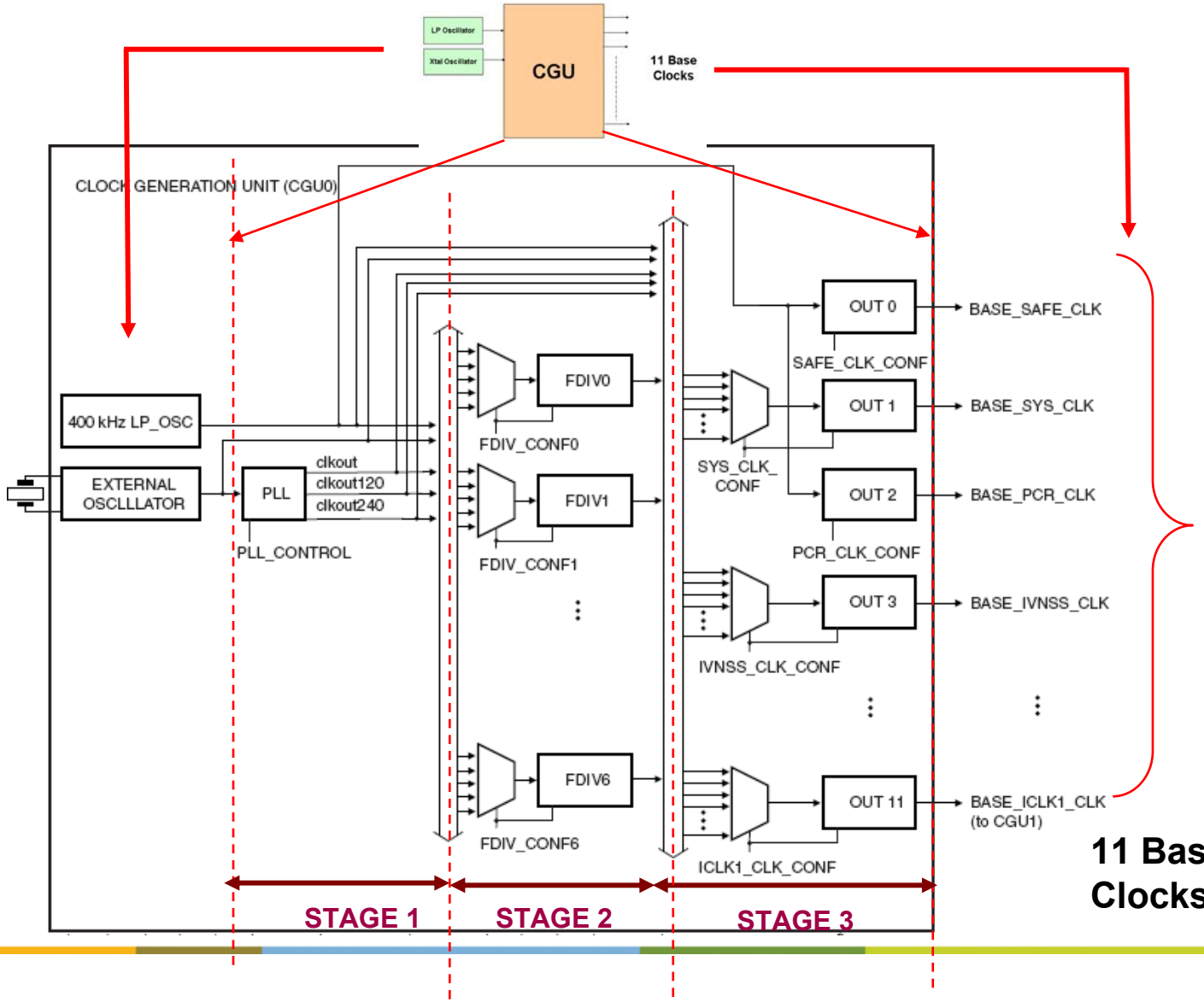
Clock Structure: CGU0 and CGU1

- CGU0 provides clocks to all the subsystems
- CGU1 provides clock to the USB block and provides a clock output
- Both CGUs are functionally identical

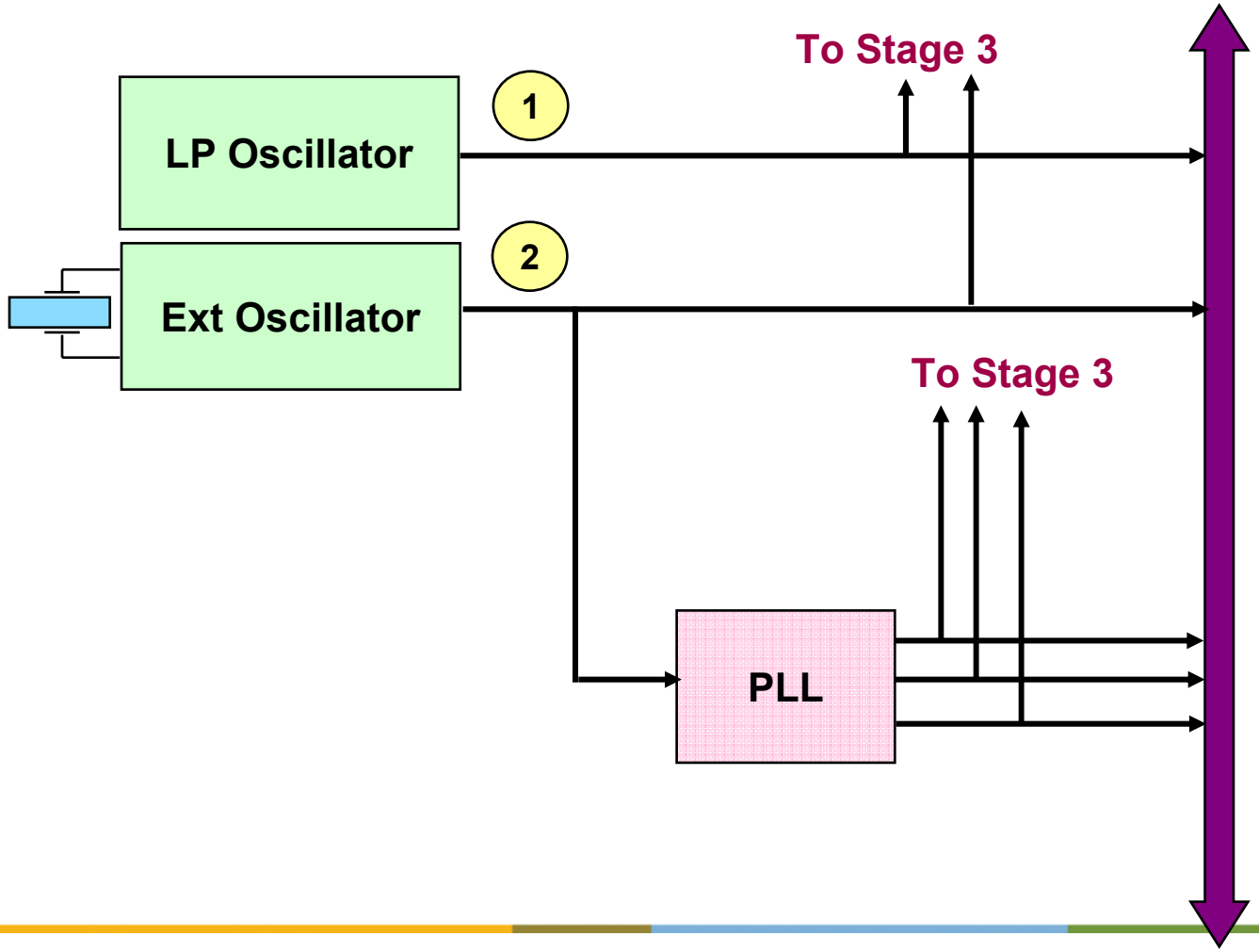
CGU0 Operation



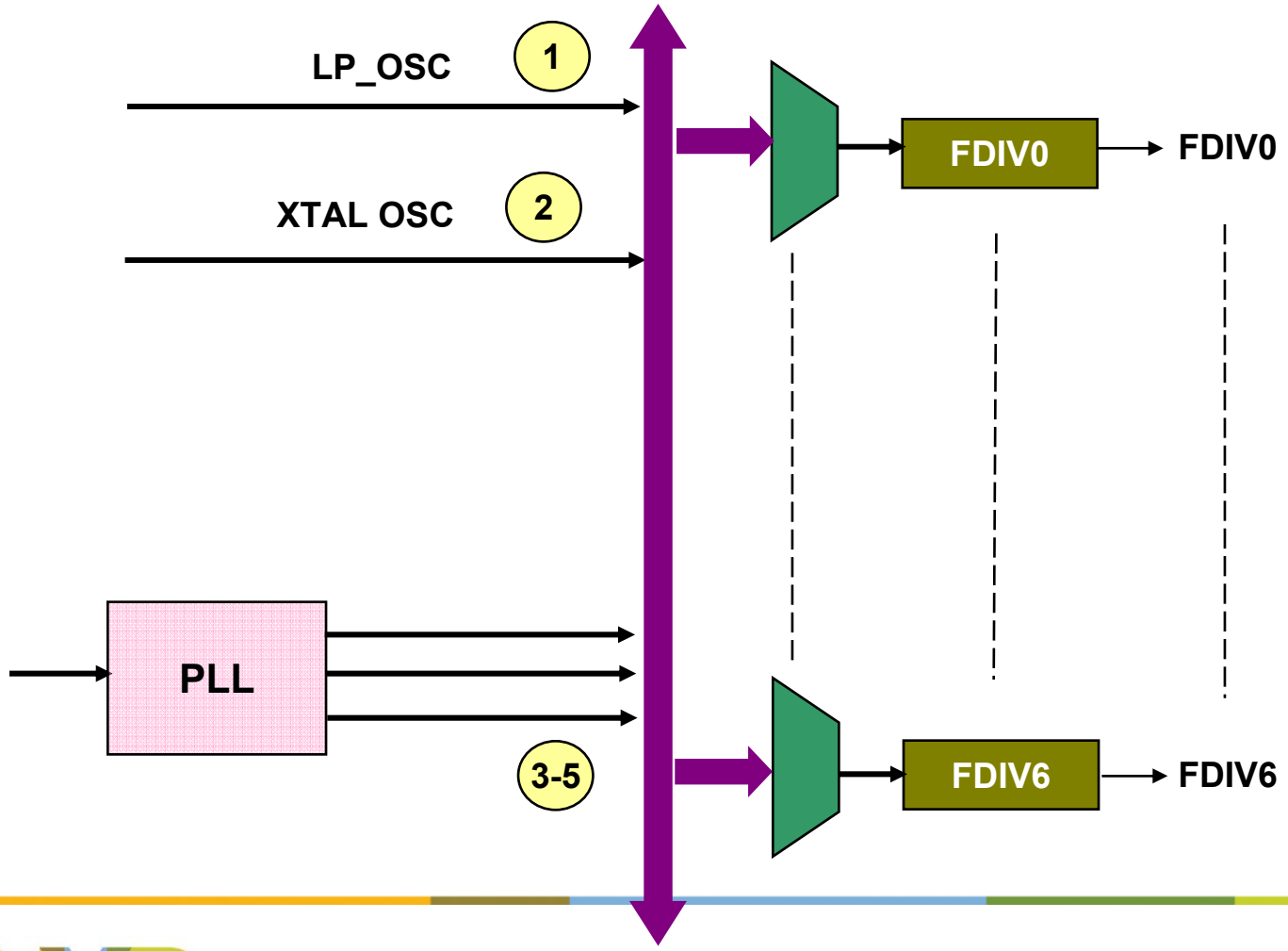
CGU0 Breakdown



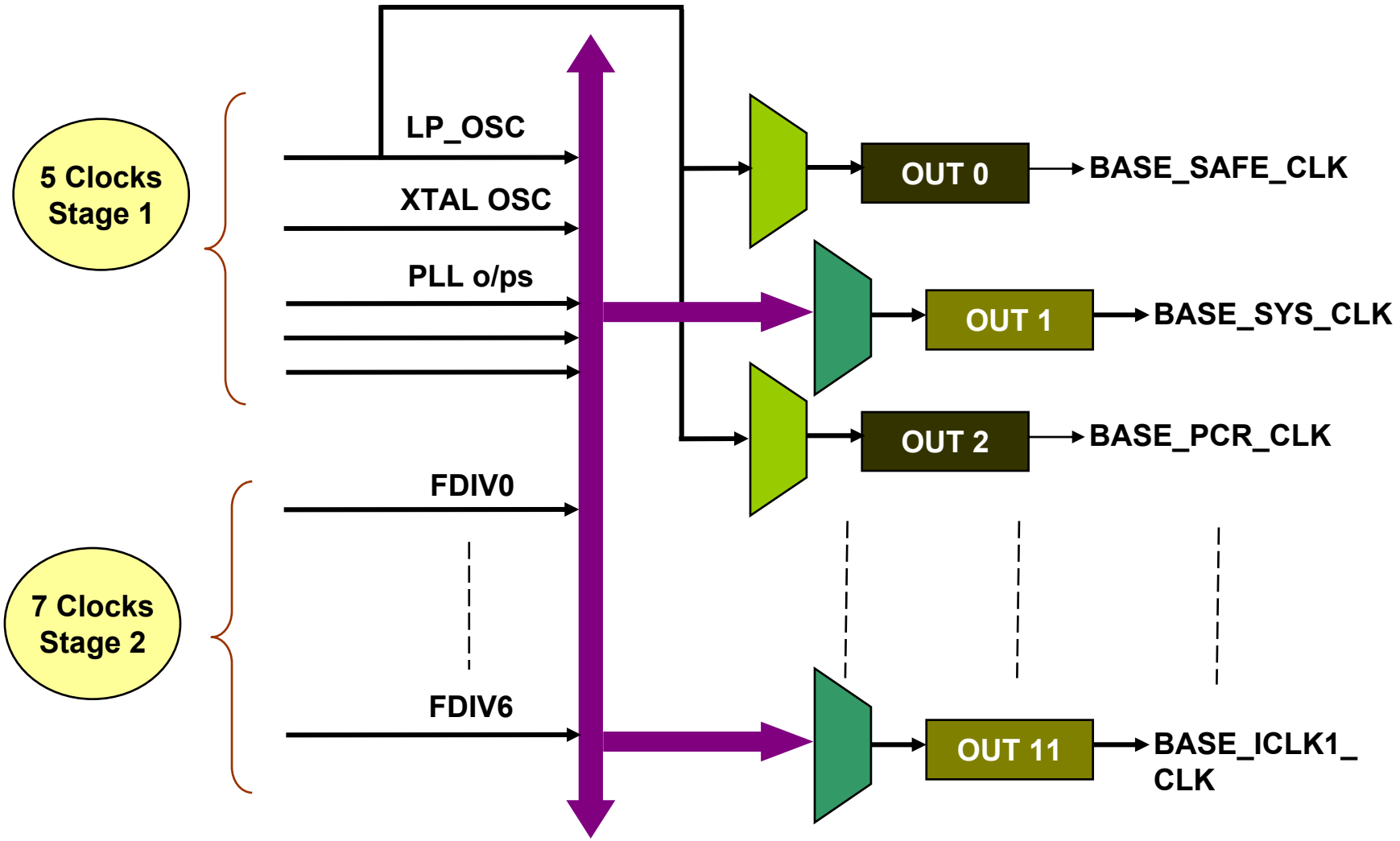
Stage 1: PLL



Stage 2: Fractional Dividers



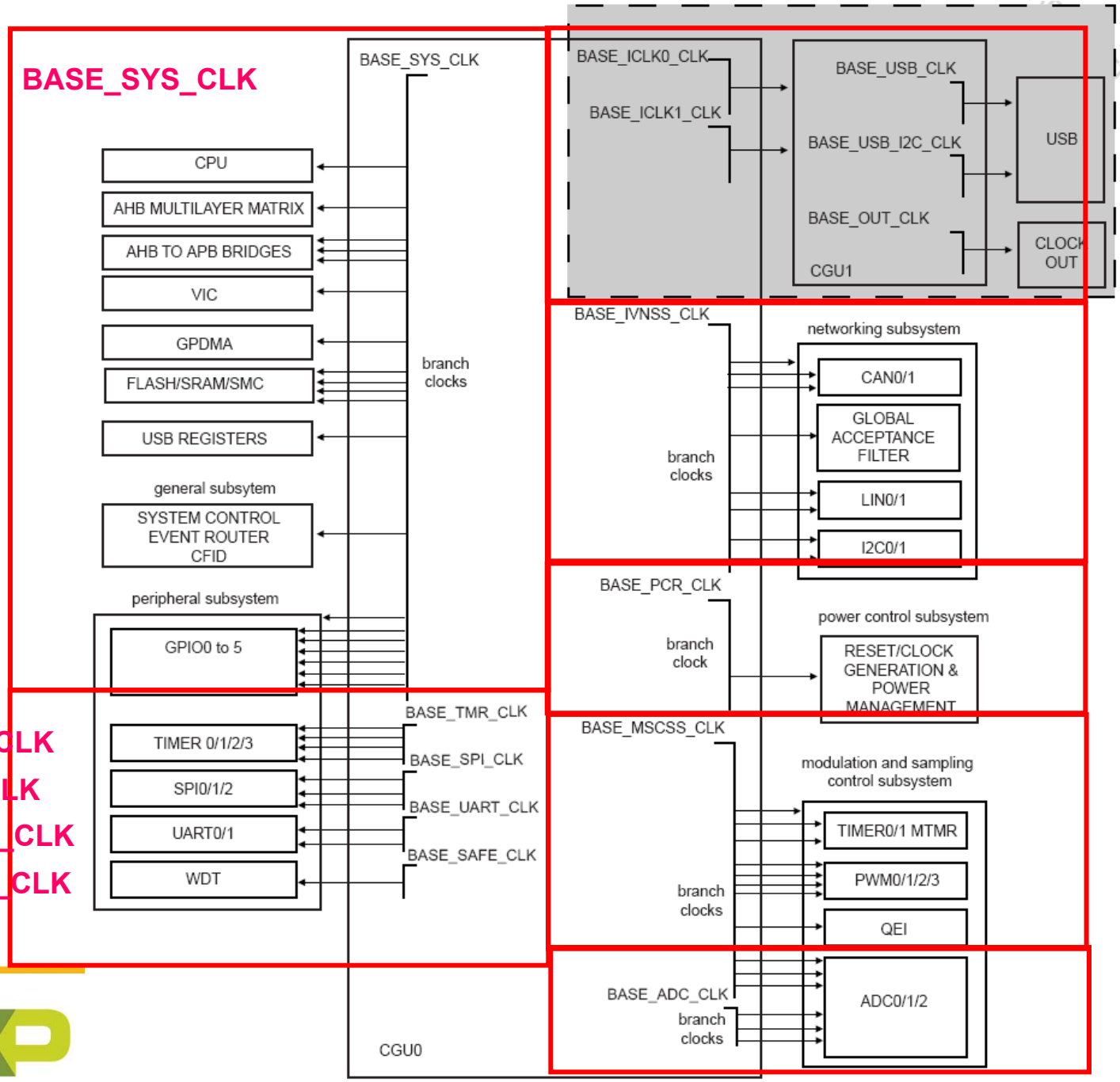
Stage 3: Output Registers



The 11 Base Clocks

BASE CLOCK	DESTINATION
BASE_SAFE_CLK	Watchdog timer
BASE_SYS_CLK	ARM and AHB clock
BASE_PCR_CLK	PCR subsystem
BASE_IVNSS_CLK	Networking subsystem
BASE_MSCSS_CLK	MSC subsystem
BASE_ICLK0_CLK	Used by CGU1
BASE_UART_CLK	Clock to UARTs
BASE_SPI_CLK	Clock to SPIs
BASE_TMR_CLK	Clock to Timers
BASE_ADC_CLK	Clock to ADCs
BASE_ICLK1_CLK	Used by CGU1

Visual Guidance on Next Slide



BASE_ICLK0/1_CLK

BASE_IVNSS_CLK

BASE_PCR_CLK

BASE_MSCSS_CLK

BASE_TMR_CLK

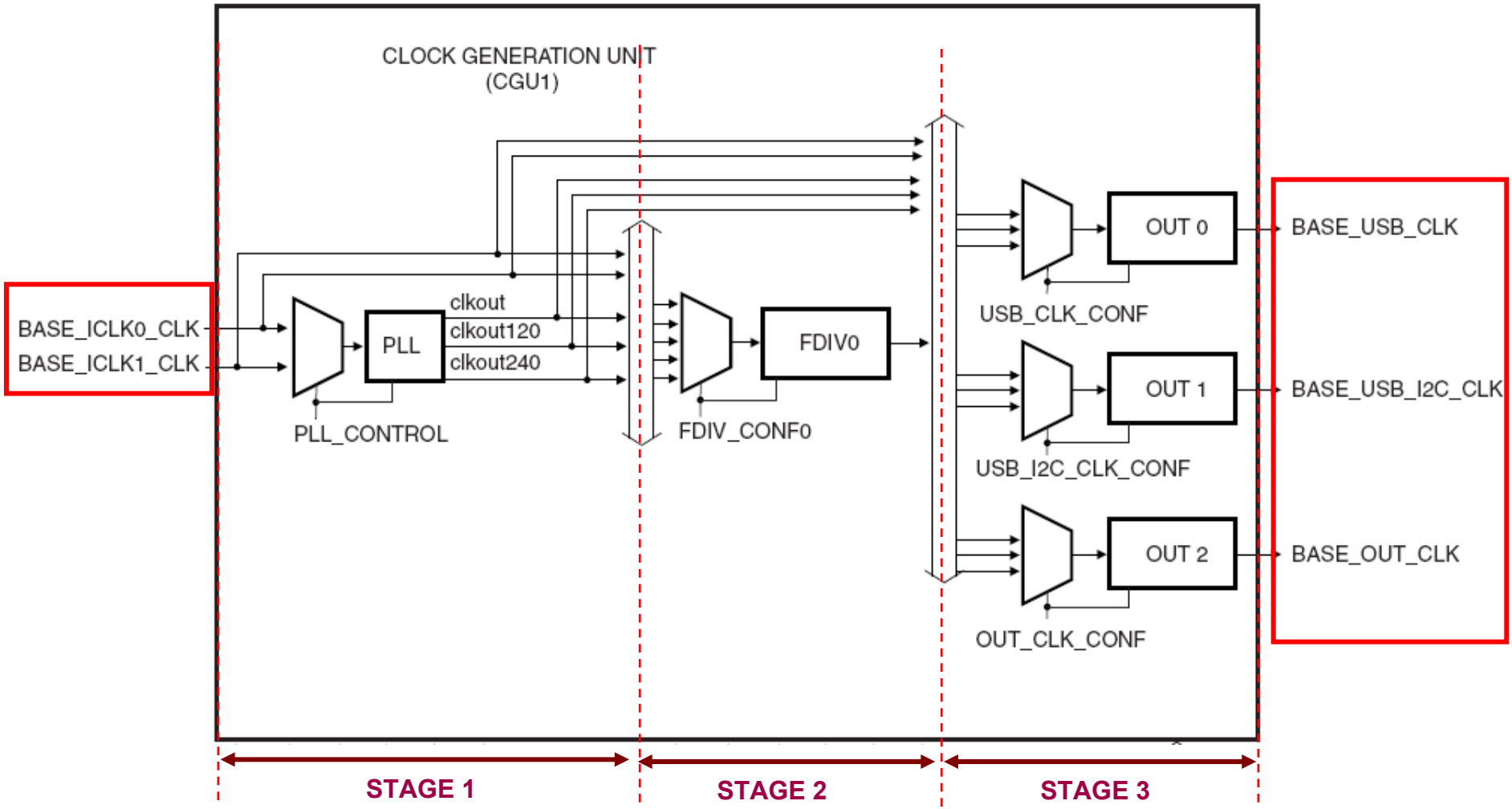
BASE_SPI_CLK

BASE_UART_CLK

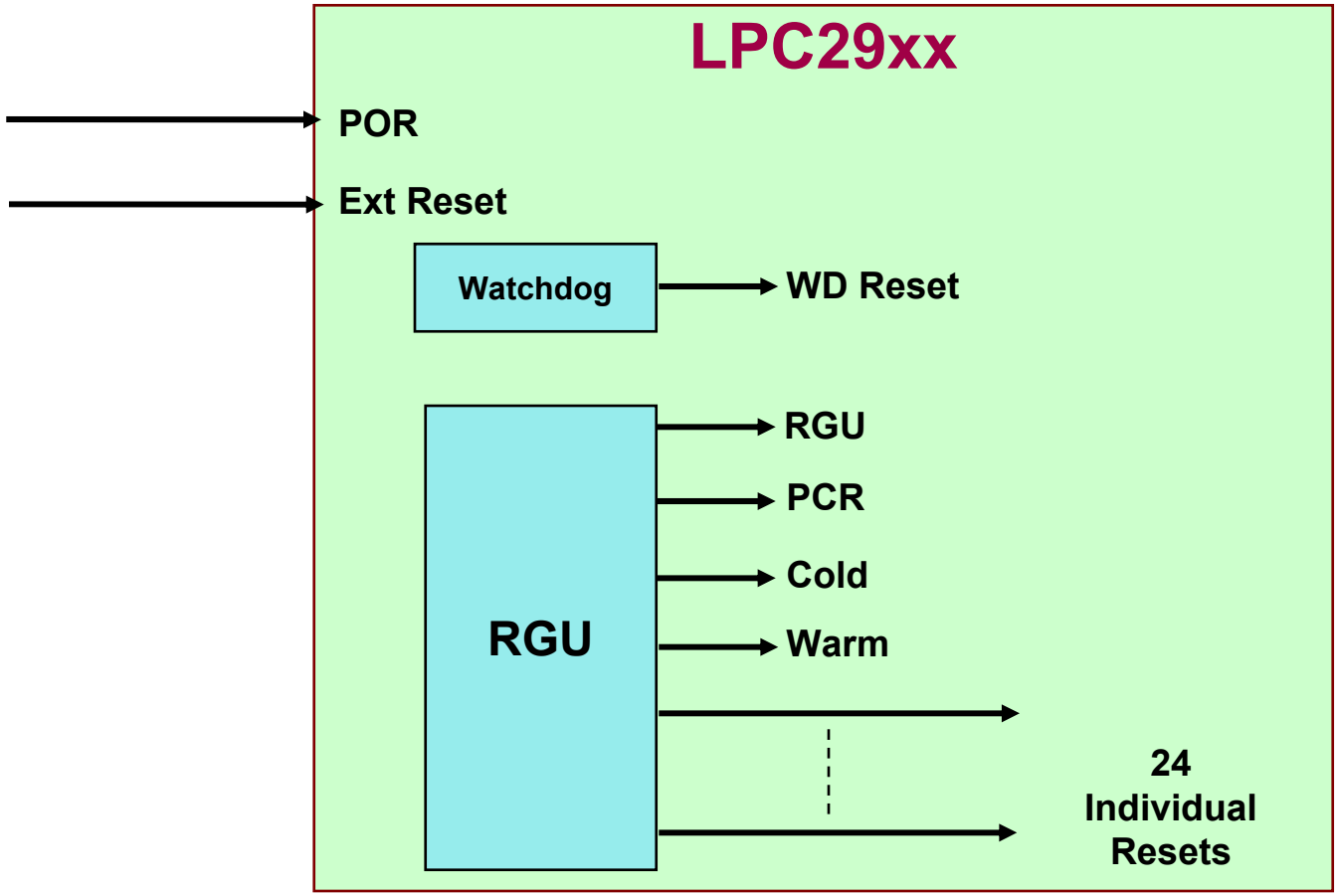
BASE_SAFE_CLK

BASE_ADC_CLK

CGU1


CLOCK GENERATION UNIT
(CGU1)
BASE_ICLK0_CLK
BASE_ICLK1_CLK
PLL
clkout
clkout120
clkout240
PLL_CONTROL
FDIV0
FDIV_CONF0
OUT 0
USB_CLK_CONF
OUT 1
USB_I2C_CLK_CONF
OUT 2
OUT_CLK_CONF
BASE_USB_CLK
BASE_USB_I2C_CLK
BASE_OUT_CLK
STAGE 1
STAGE 2
STAGE 3

RGU


LPC29xx
POR
Ext Reset
Watchdog
WD Reset
RGU
RGU
PCR
Cold
Warm
24
Individual
Resets

Block Resets Explained

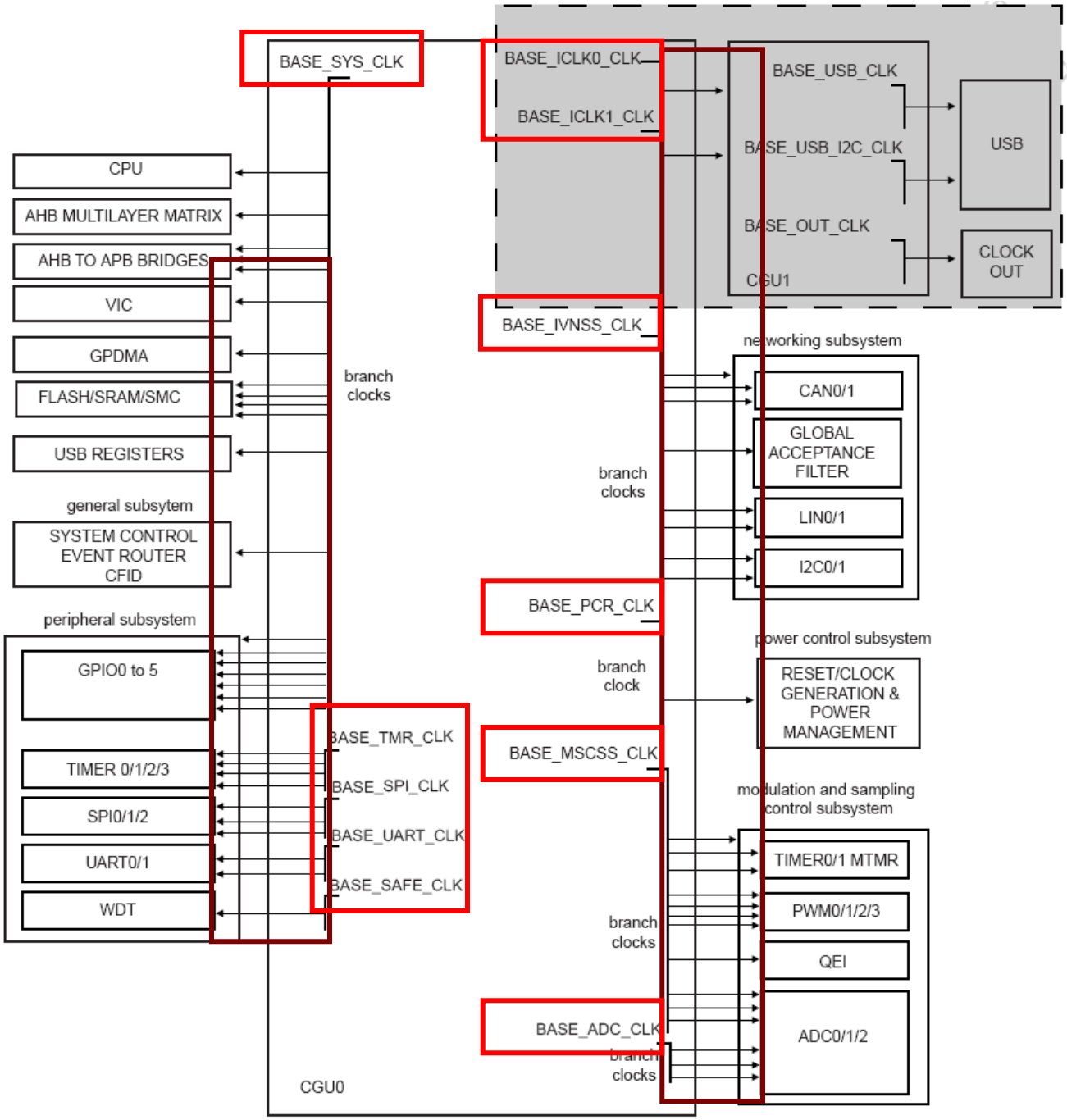
Priority	Reset	OSC1M	RGU	WDT	SCU	Flash controller	CFID	Memory controllers (SRAM,SMC)	all other peripherals
1	POR	yes	yes	yes	yes	yes	yes	yes	yes
2	EXT RESET	no	yes	yes	yes	yes	yes	yes	yes
3	RGU	no	yes	yes	yes	yes	yes	yes	yes
4	WDT	no	no	yes	yes	yes	yes	yes	yes
5	PCR	no	no	yes	yes	yes	yes	yes	yes
6	Cold	no	no	no	no	yes	yes	yes	yes
7	Warm	no	no	no	no	no	no	no	yes

RGU Summary

- Activation of reset
  - Group reset- RGU, PCR, Cold and Warm
  - Provides 24 individual resets to different blocks like SPI, UART, USB etc.

- Other key functions
  - Monitoring
  - Finding the source of reset
  - Locking the CGU

PMU


BASE_SYS_CLK
BASE_ICLK0_CLK
BASE_ICLK1_CLK
BASE_USB_CLK
BASE_USB_I2C_CLK
BASE_OUT_CLK
CGU1
USB
CLOCK OUT
BASE_IVNSS_CLK
networking subsystem
CAN0/1
GLOBAL ACCEPTANCE FILTER
LIN0/1
I2C0/1
BASE_PCR_CLK
power control subsystem
RESET/CLOCK GENERATION & POWER MANAGEMENT
BASE_MSCSS_CLK
modulation and sampling control subsystem
TIMER0/1 MTMR
PWM0/1/2/3
QEI
ADC0/1/2
BASE_ADC_CLK
CPU
AHB MULTILAYER MATRIX
AHB TO APB BRIDGES
VIC
GPDMA
FLASH/SRAM/SMC
USB REGISTERS
general subsytem
SYSTEM CONTROL EVENT ROUTER CFID
peripheral subsystem
GPIO0 to 5
TIMER 0/1/2/3
SPI0/1/2
UART0/1
WDT
BASE_TMR_CLK
BASE_SPI_CLK
BASE_UART_CLK
BASE_SAFE_CLK
branch clocks
branch clocks
branch clock
branch clocks
branch clocks
CGU0

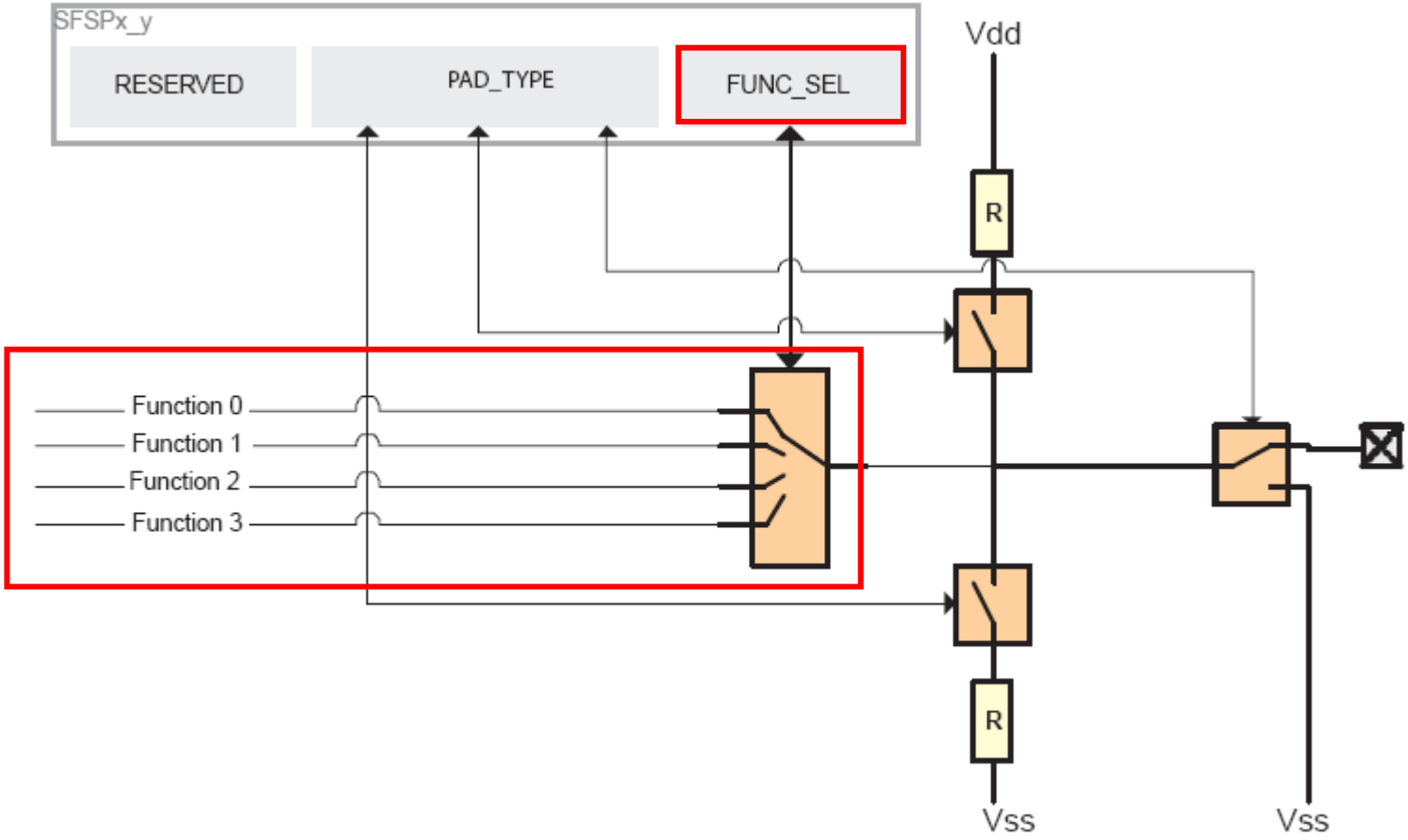
PMU Explained

- Configuration and status registers are provided for all branch clocks (except CLK_SYS_CPU, CLK_SYS & CLK_SYS_PCR)
  - Individual branch clocks can be also be switched off
  - Individual branch clocks can be made ready for sleep mode
- Using a single PD bit, all selected branch clocks can be put to sleep
- Wakeup from idle mode, can be achieved with the Event router which is covered later

General Subsystem (GeSS)

- System Control Unit (SCU)
- Event Router
- [Vectored Interrupt Controller]

SCU- Selecting Pin Function



Input Pads

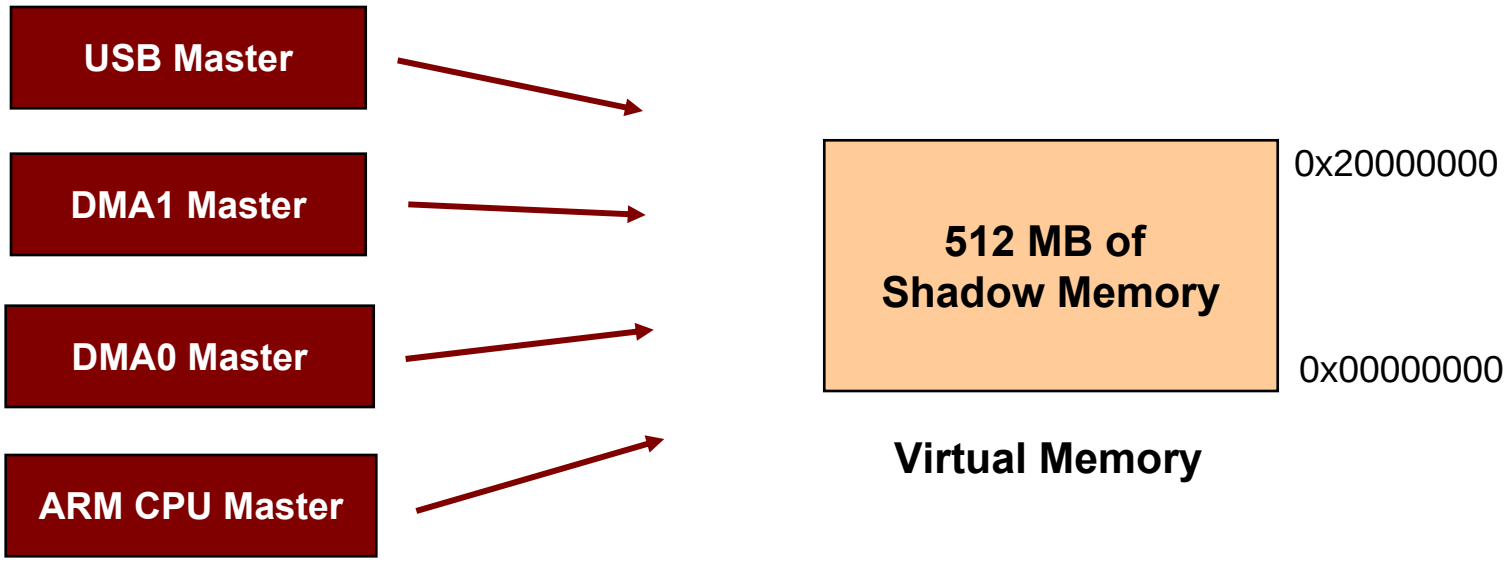
- Analog input

- Digital input
  - With internal pull up/down
  - With internal pull up
  - With internal pull down
  - With bus keeper

- When pull up is activated the input is NOT 5V TOLERANT

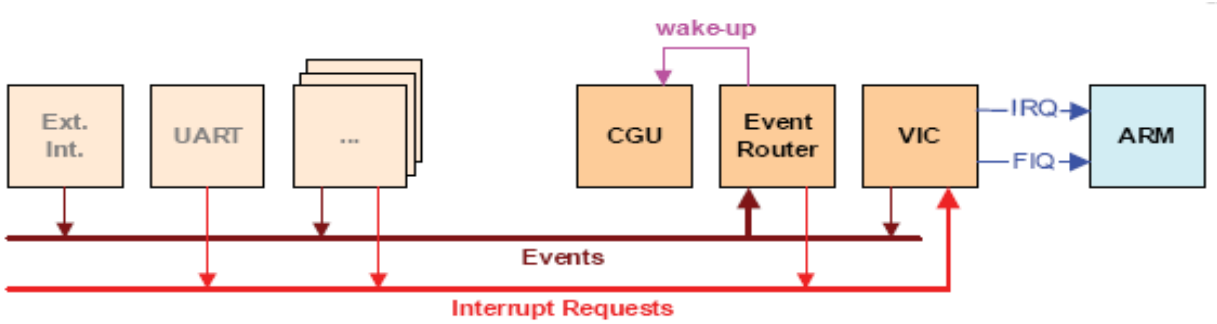
SCU- Memory Mapping

- Shadow memory mapping registers defines which part of the memory region is present in the shadow memory area



Event Router- What is it?

- Main purpose:
  - Uses “events” to wake up the CGU
  - Uses “events” to act like an interrupt source to the VIC
- Events:
  - External pins
  - Internal interrupts
- Interacts with the VIC in both ways
  - Acts like a source of interrupt to the VIC
  - Or use the VIC as a source to wake up the CGU



Event Router

EXTINTx

CANx Rx pins

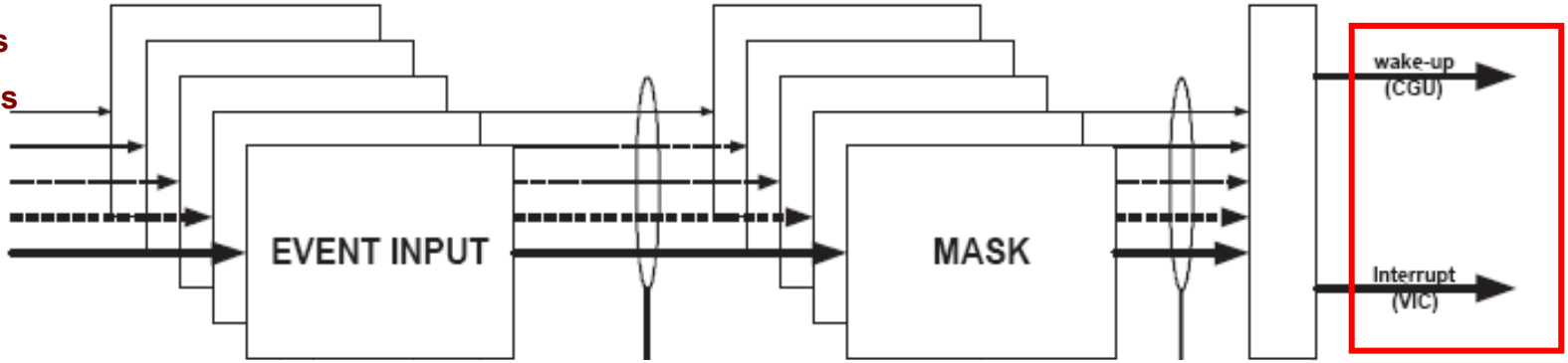
I2C Clock pins

LINx Rx pins

SPIx Rx pins

UARTx pins

USB pins

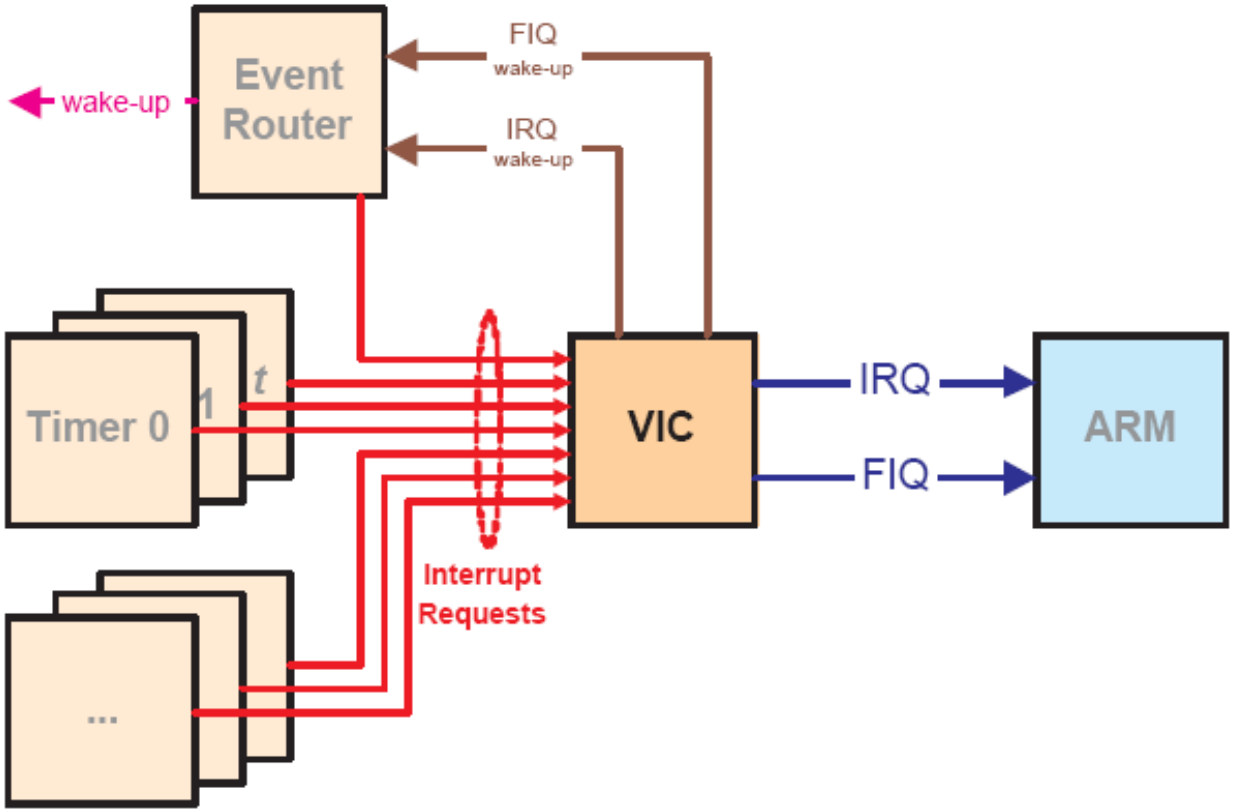


CAN interrupt

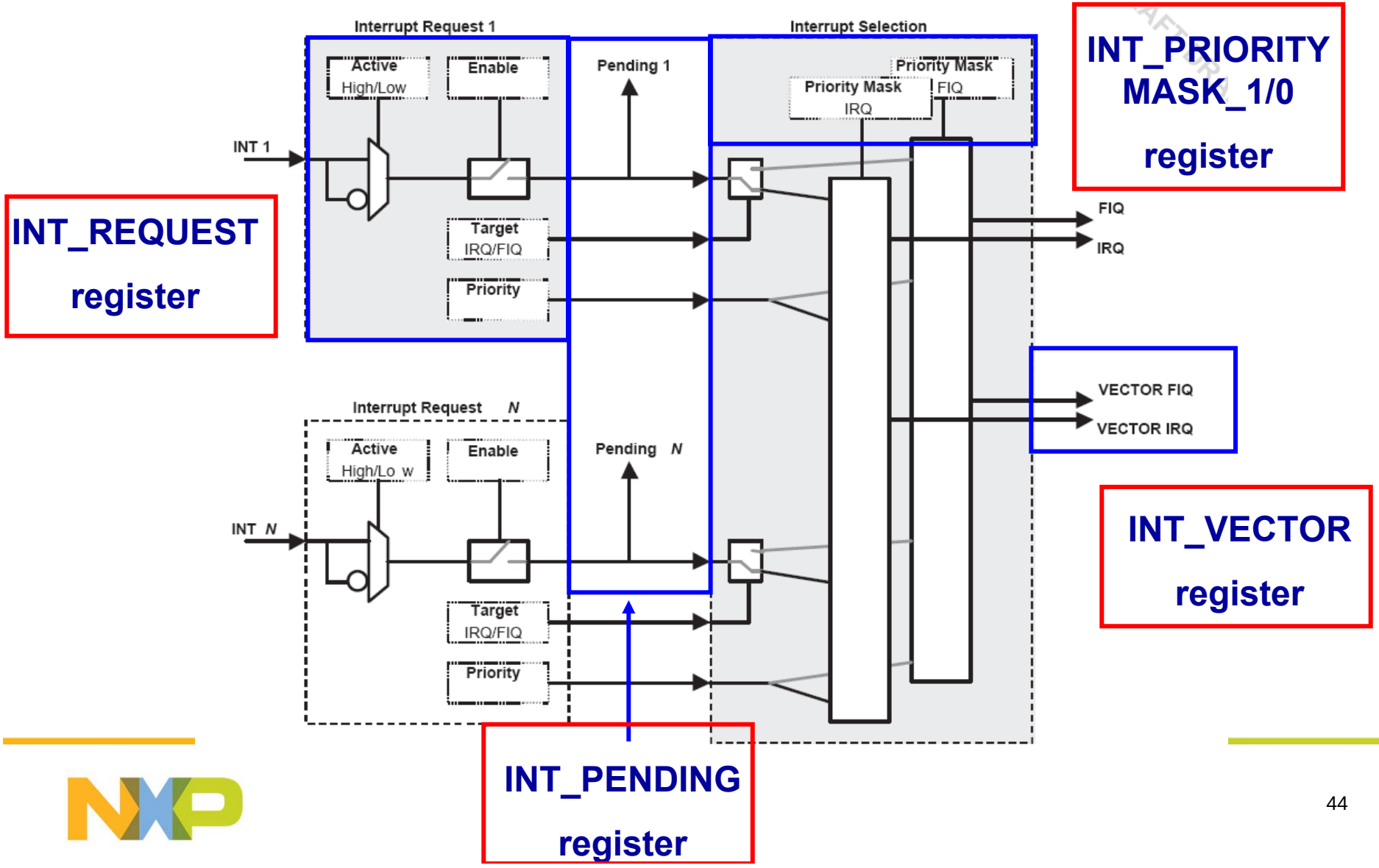
VIC IRQ

VIC FIQ

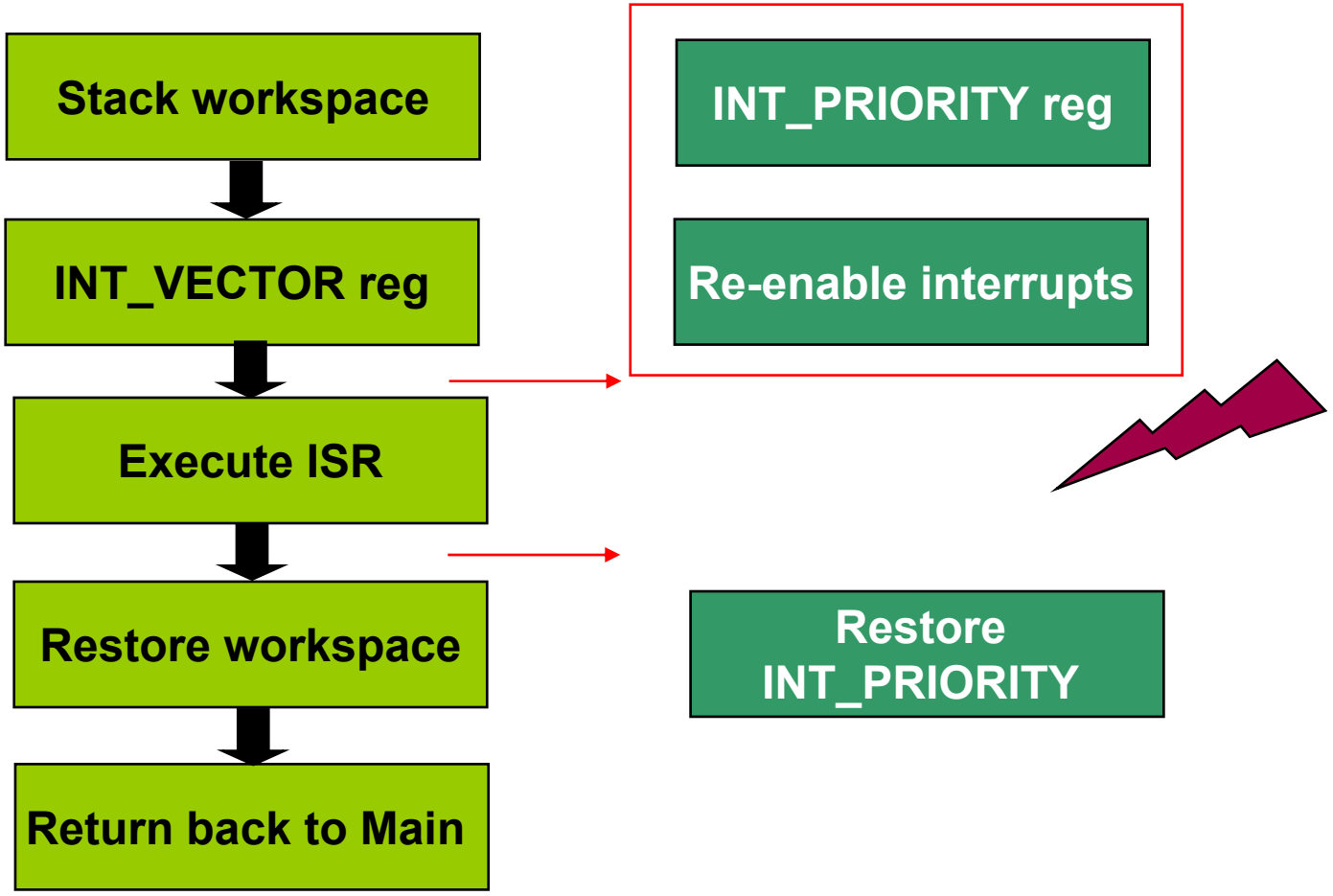
Vectored Interrupt Controller (VIC)



An Inside Look into the VIC



Interrupt Execution (Nested & Non-Nested)



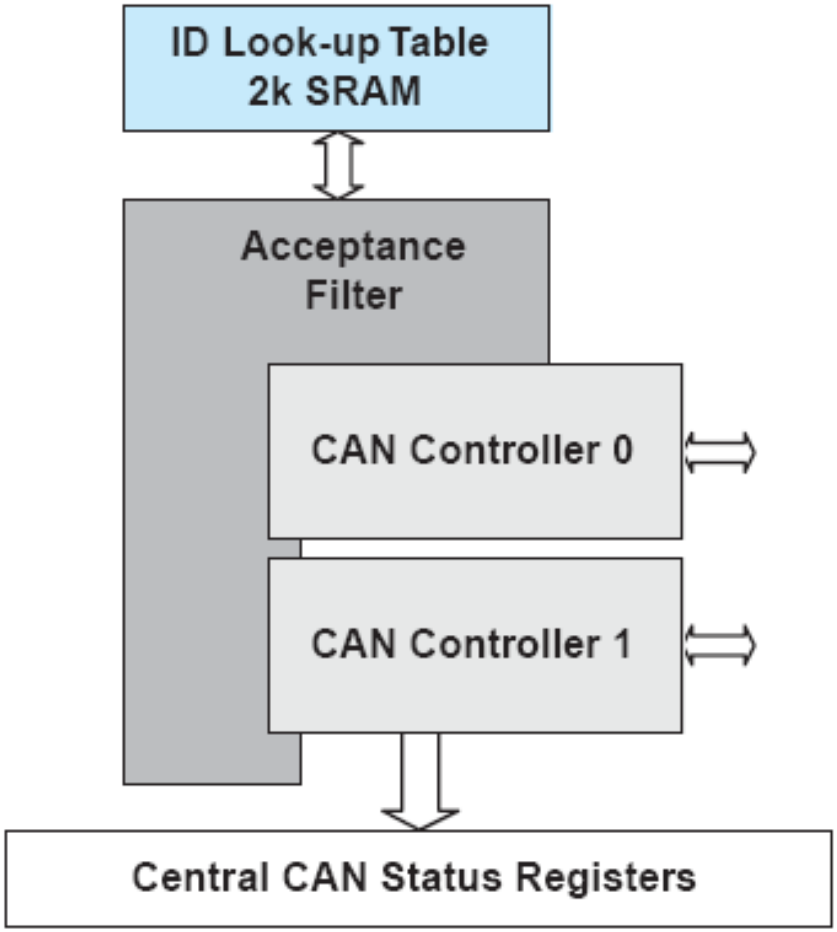
Networking Subsystem (IVNSS)

- CAN
- LIN
- I^2C

2 CAN Controllers- Key Features

- Data rates up to 1 Mb/s, CAN 2.0B & ISO 11898 compatible
- Supports Full-CAN mode and extensive message filtering
- Each controller supports triple transmit buffers and double receive buffers
- Error and System Diagnostics Support, Self Reception Mode & Listen Only Mode
- Advanced Hardware Acceptance Filter to reduce CPU load

CAN Functional Description

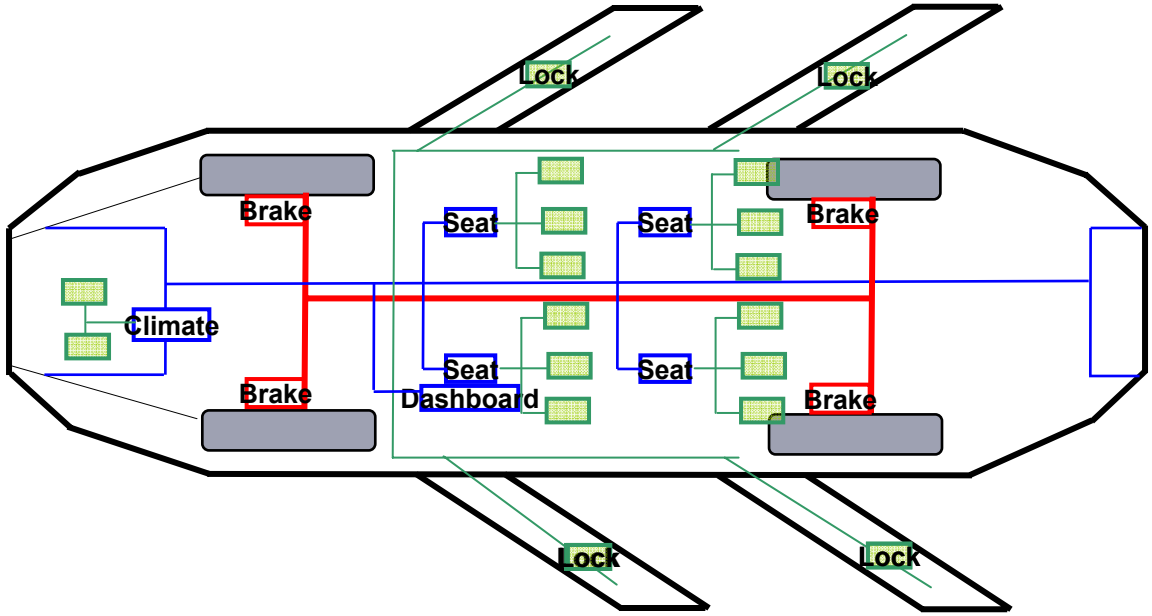


Global Acceptance Filter

- Uses a 2KB look-up table
- The table can contain up to 1024 SFI or 512 EFI or mixture of both types
- Broken up into 5 sections
- CAN configuration example: http://www.nxp.com/acrobat_download/applicationnotes/AN10674_1.pdf

LIN- An Introduction

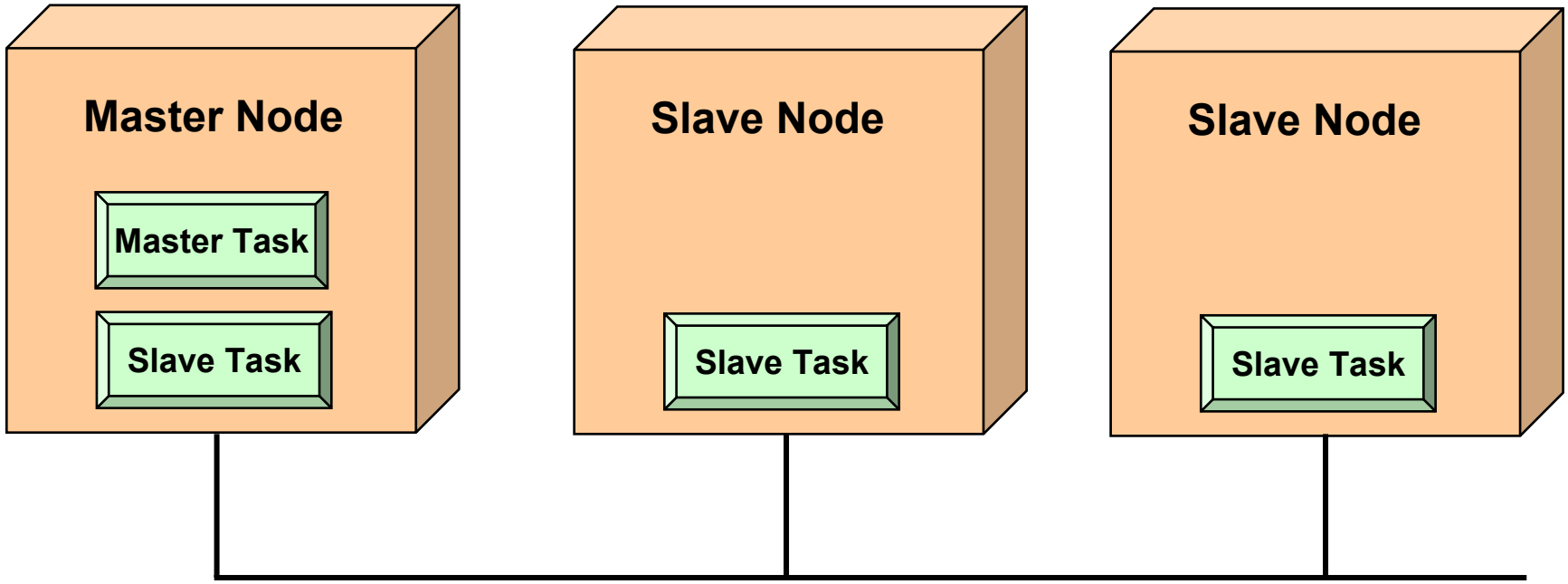
- Low cost sub network, complementing CAN and FlexRay
- Single master, multiple slaves concept
- Based on the UART interface
- Speed up to 20Kbits/sec



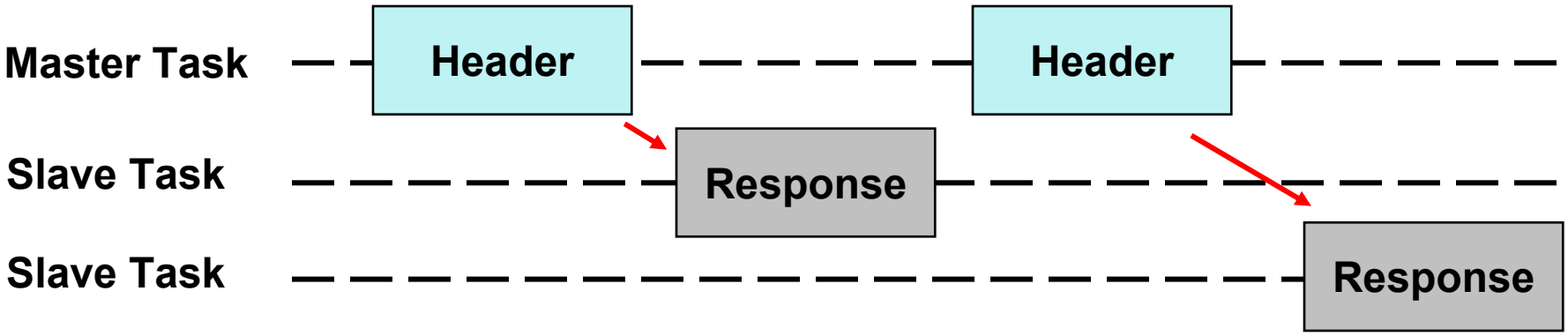
FlexRay
CAN
LIN

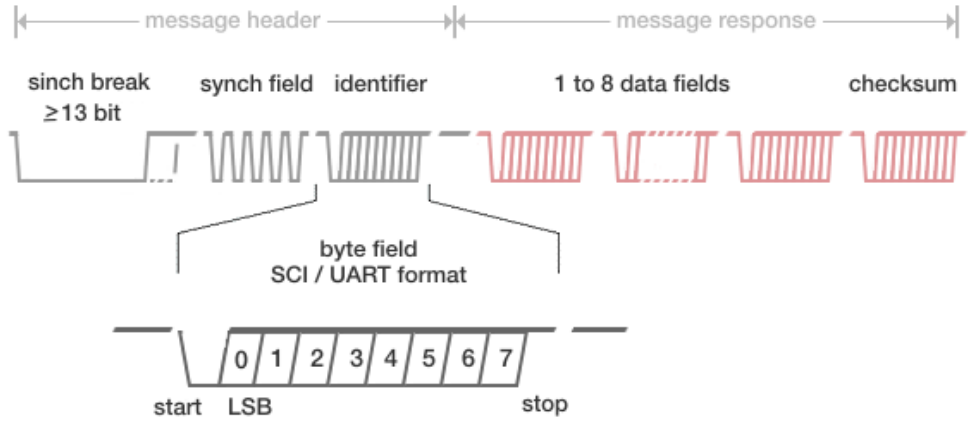
LOCAL INTERCONNECT NETWORK

LIN Network


Master Node
Master Task
Slave Task
Slave Node
Slave Task
Slave Node
Slave Task

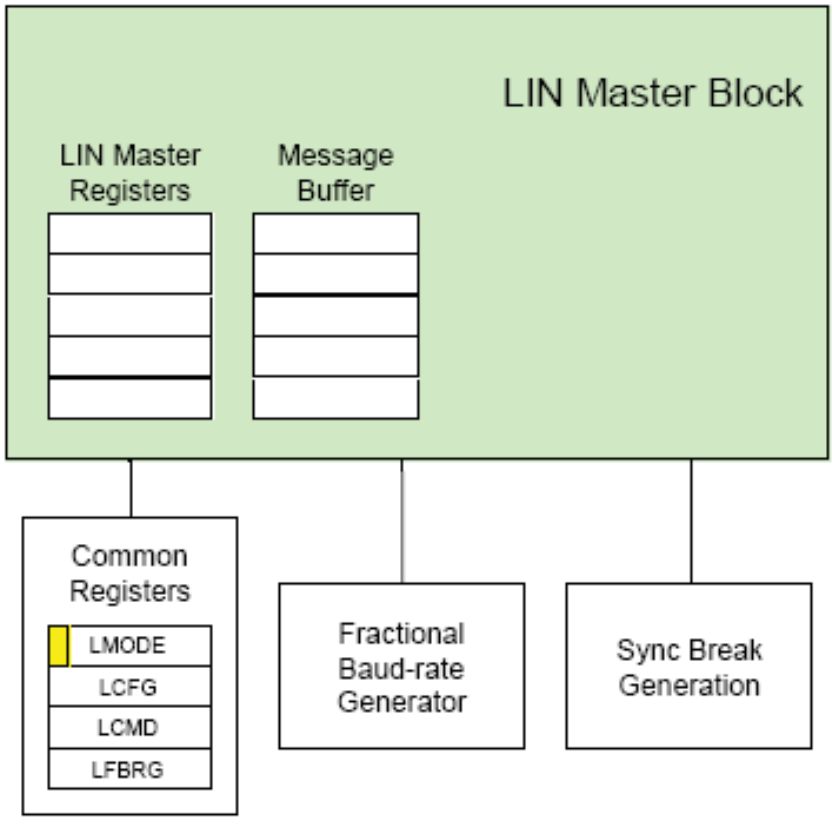
LIN Message Transmission





LIN Master Controller

- 4 32-bit Message buffers
- Programmable sync-break from 10-16 bits
- “Step-by-step example for using the LIN master”



2 I²C-Interfaces

- 400 KHz transfer rates (Fast I2C)
- Easy to configure as master, slave or master/slave
- Multi-master bus with arbitration control
- Supports multiple address recognition and a bus monitor mode

Peripheral Subsystem (PeSS)

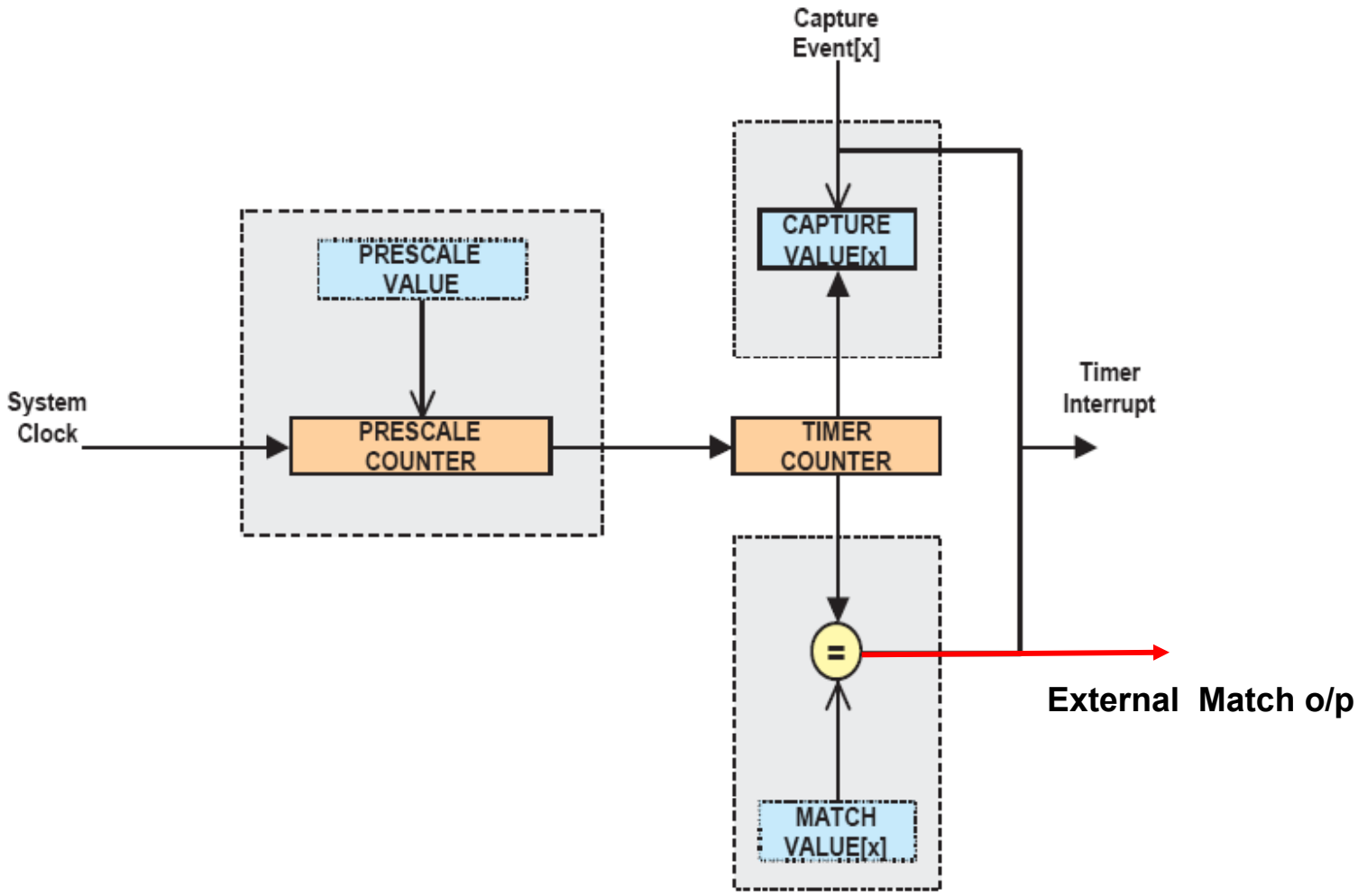
- IO ports
- SPIs
- Timers
- UARTs

General Purpose IO Ports

- Up to 108 IO pins with programmable pull up, pull down and bus keeper
- 6 GPIO ports each capable of accessing up to 32 pins
- The pins must be routed in the SCU

Part number	GPIO port 0	GPIO port 1	GPIO port 2	GPIO port 3	GPIO port 4	GPIO port 5	GPIO port 5/USB
LPC2917/19/01	P0[31:0]	P1[31:0]	P2[27:0]	P3[15:0]	-	-	-
LPC2921/23/25	P0[31:0]	P1[27:0]	-	-	-	-	P5[19:18]
LPC2927/29	P0[31:0]	P1[27:0]	P2[27:0]	P3[15:0]	-	-	P5[19:18]
LPC2930	P0[31:0]	P1[27:0]	P2[27:0]	P3[15:0]	P4[23:0]	P5[15:0]	P5[19:16]
LPC2939	P0[31:0]	P1[27:0]	P2[27:0]	P3[15:0]	P4[23:0]	P5[15:0]	P5[19:16]

Timers 0/1/2/3


Capture
Event[x]
CAPTURE
VALUE[x]
PRESCALE
VALUE
System
Clock
PRESCALE
COUNTER
TIMER
COUNTER
Timer
Interrupt
=
External Match o/p
MATCH
VALUE[x]

Watchdog- Features

- The timer registers are protected by key sequences
- Two operating modes- Normal and debug
- Internal chip reset when not triggered periodically- Through RGU

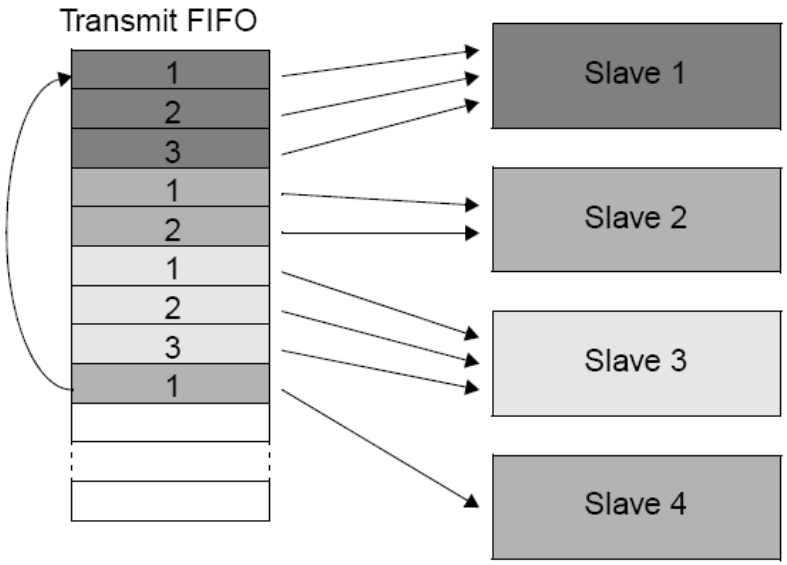
Priority	Reset	OSC1M	RGU	WDT	SCU	Flash controller	CFID	Memory controllers (SRAM,SMC)	all other peripherals
1	POR	yes	yes	yes	yes	yes	yes	yes	yes
2	EXT RESET	no	yes	yes	yes	yes	yes	yes	yes
3	RGU	no	yes	yes	yes	yes	yes	yes	yes
4	WDT	no	no	yes	yes	yes	yes	yes	yes
5	PCR	no	no	yes	yes	yes	yes	yes	yes
6	Cold	no	no	no	no	yes	yes	yes	yes
7	Warm	no	no	no	no	no	no	no	yes

SPI 0/1/2

- Master or slave operation
- Supports up to four slaves in sequential multi-slave operation (next slide)
- Programmable clock bit rate and pre-scaler, based on SPI source clock from the CGU
- Separate transmit and receive FIFO buffers, 16-bit wide, 32 locations deep
- Programmable data frame size from 4 to 16 bits
- Internal loop back test mode

SPI Mode of Operation

- Master mode
  - Normal transmission mode
    - Software intervention needed each time a new slave needs to be addressed
  - Sequential-slave mode
    - Will sequentially transmit data to 4 slaves as long as data is available in the FIFO
  - Max. clock rate in master mode <= fclk_spi/2



- Slave mode
  - Max. clock rate in slave mode= fclk_spi/4

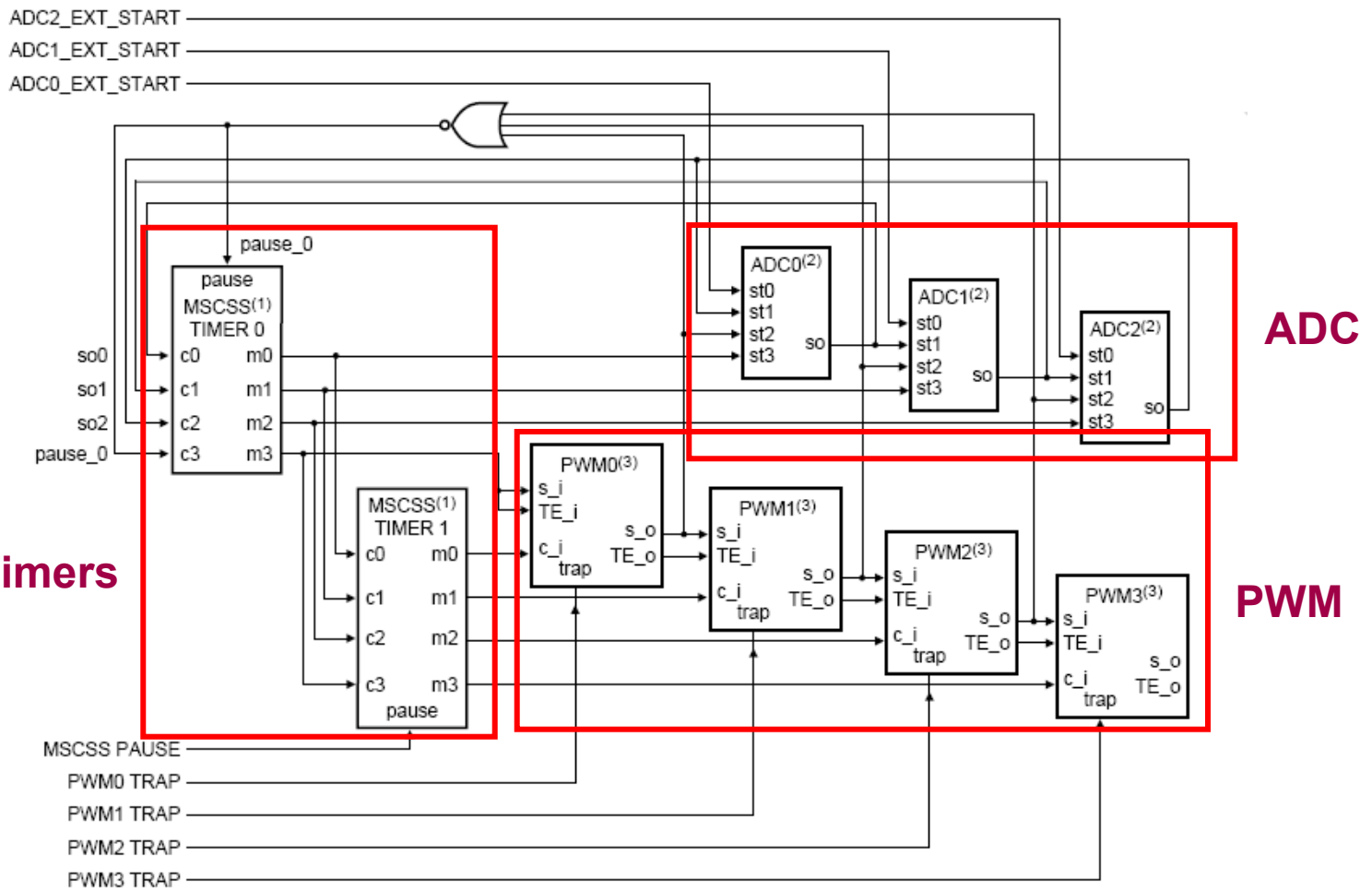
UART 0/1 Interfaces

- Industry standard 16C550 UARTs
- RS-485/9-bit mode support. Great for Multiprocessor Environment!
- 16 bytes FIFO message buffer for transmit and receive
- Fractional divider
- Standard modem interface signals included (CTS, DCD, DTS, DTR, RI, RTS)

MSC Subsystem (MSCSS)

- PWM
- ADC
- QEI

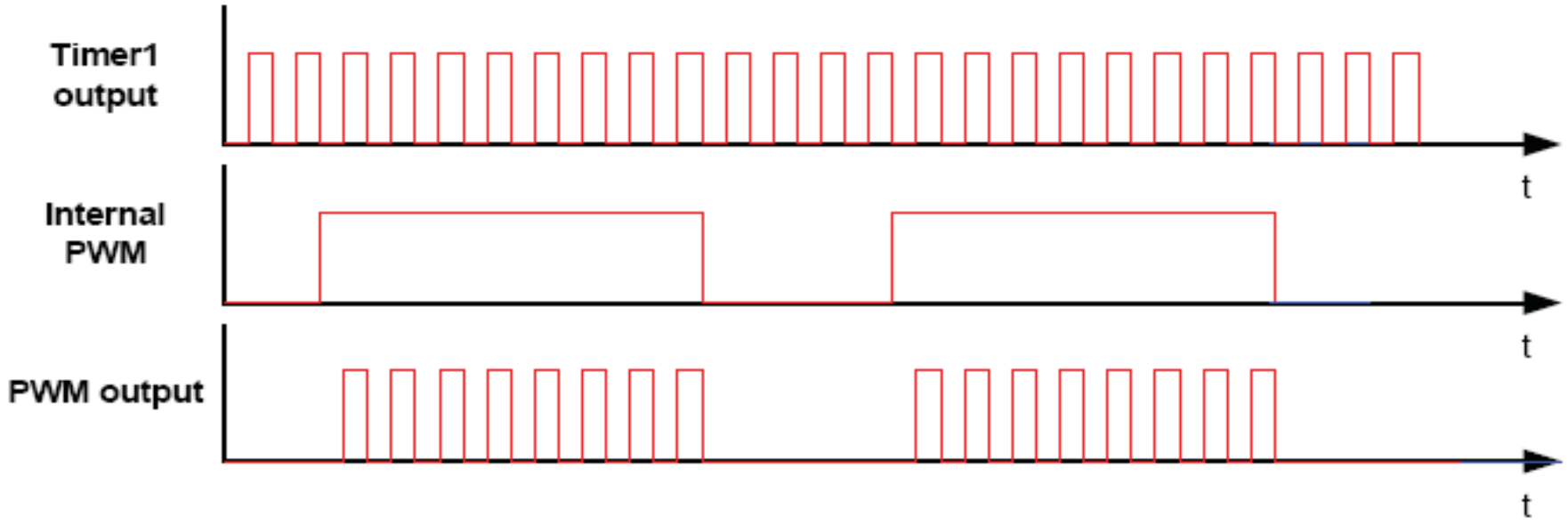
MSCSS- The Big Picture



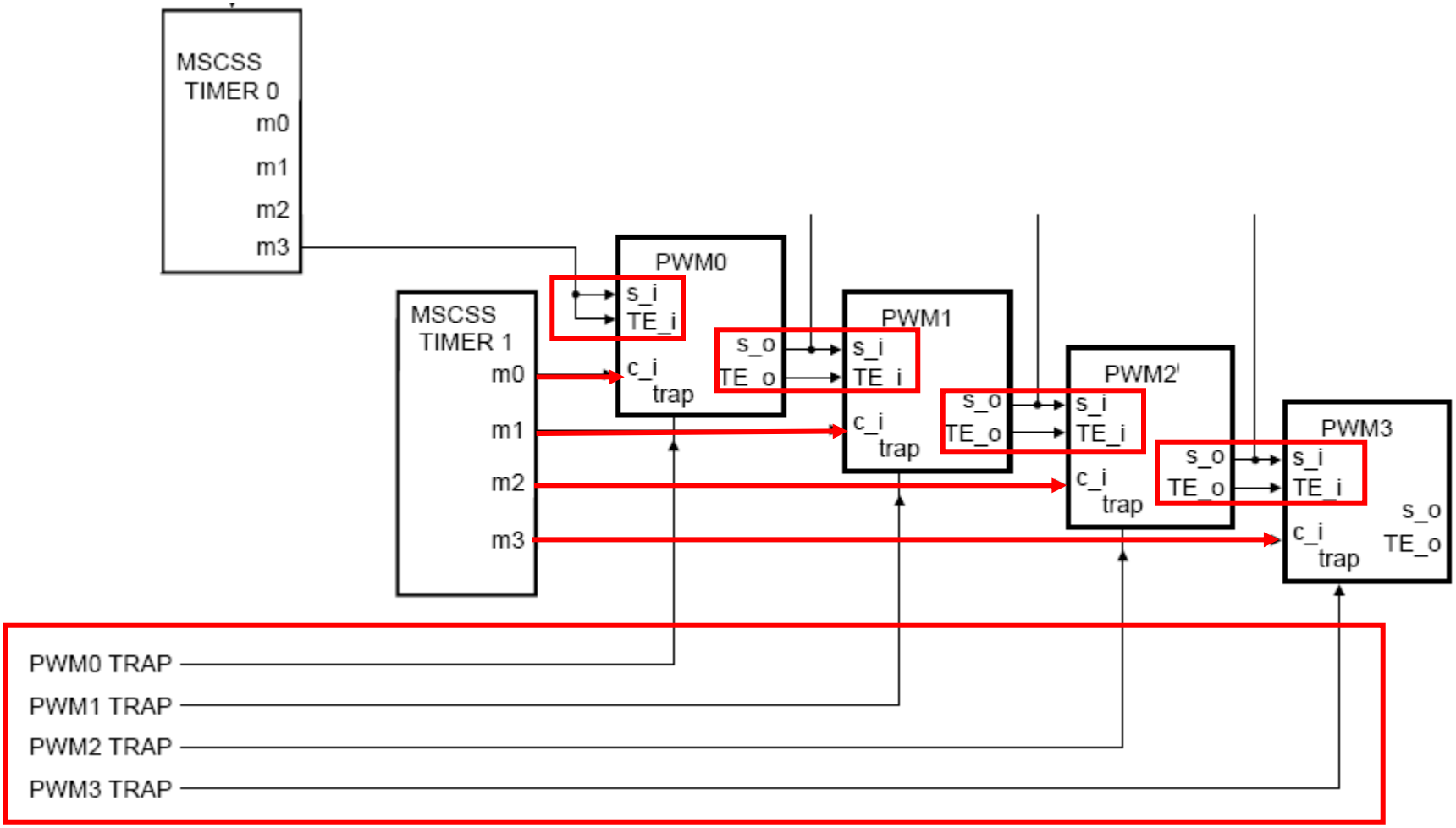
PWM Blocks- Key Features

- 4 PWM blocks that can operate synchronously
- Each PWM can produce 6 PWM outputs
- Operation modes
  - Continuous
  - Burst
  - Trap
  - Run-once
- Capture Functionality
- Shadow register set

PWM Explained (1)



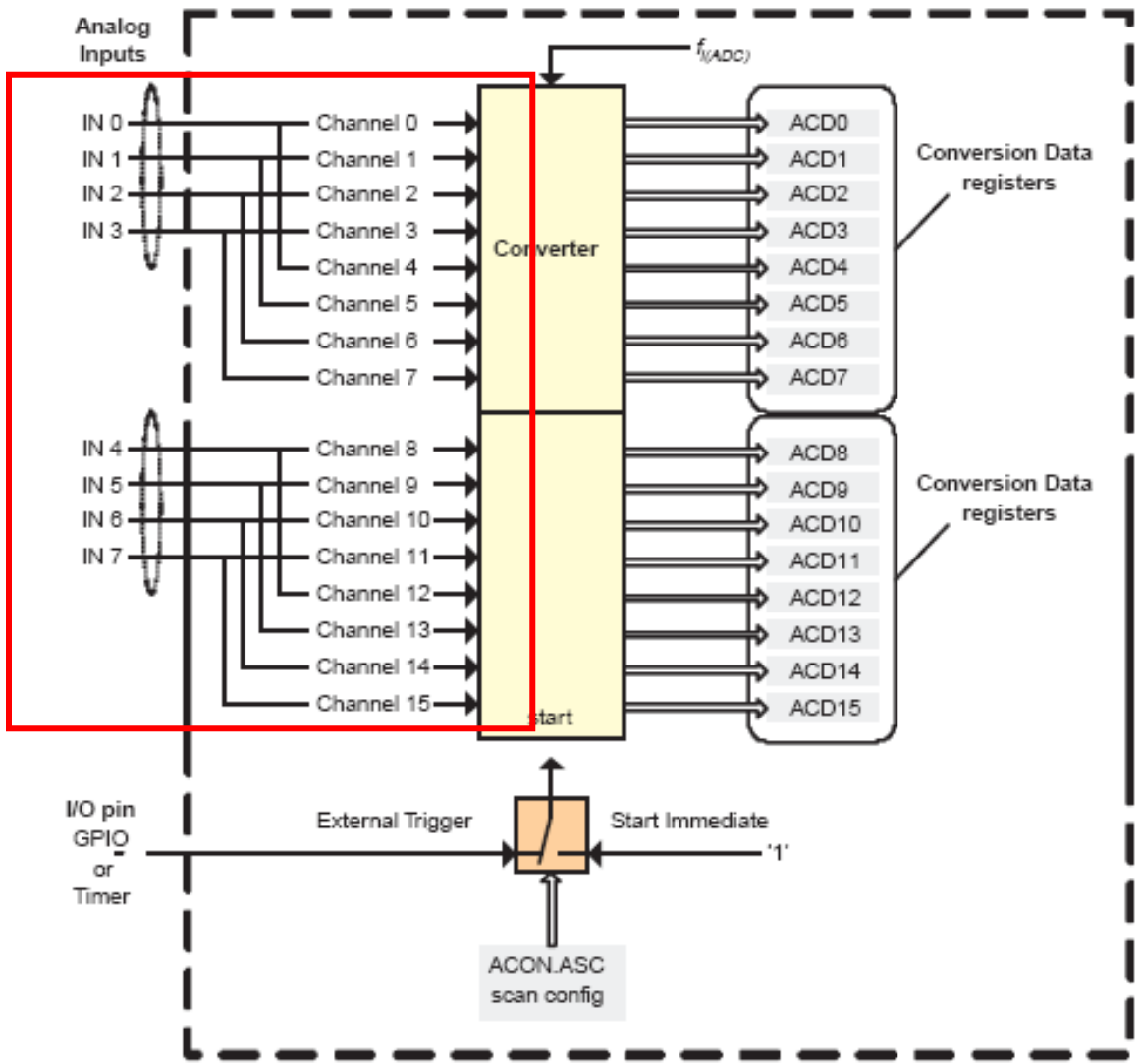
PWM Explained (2)



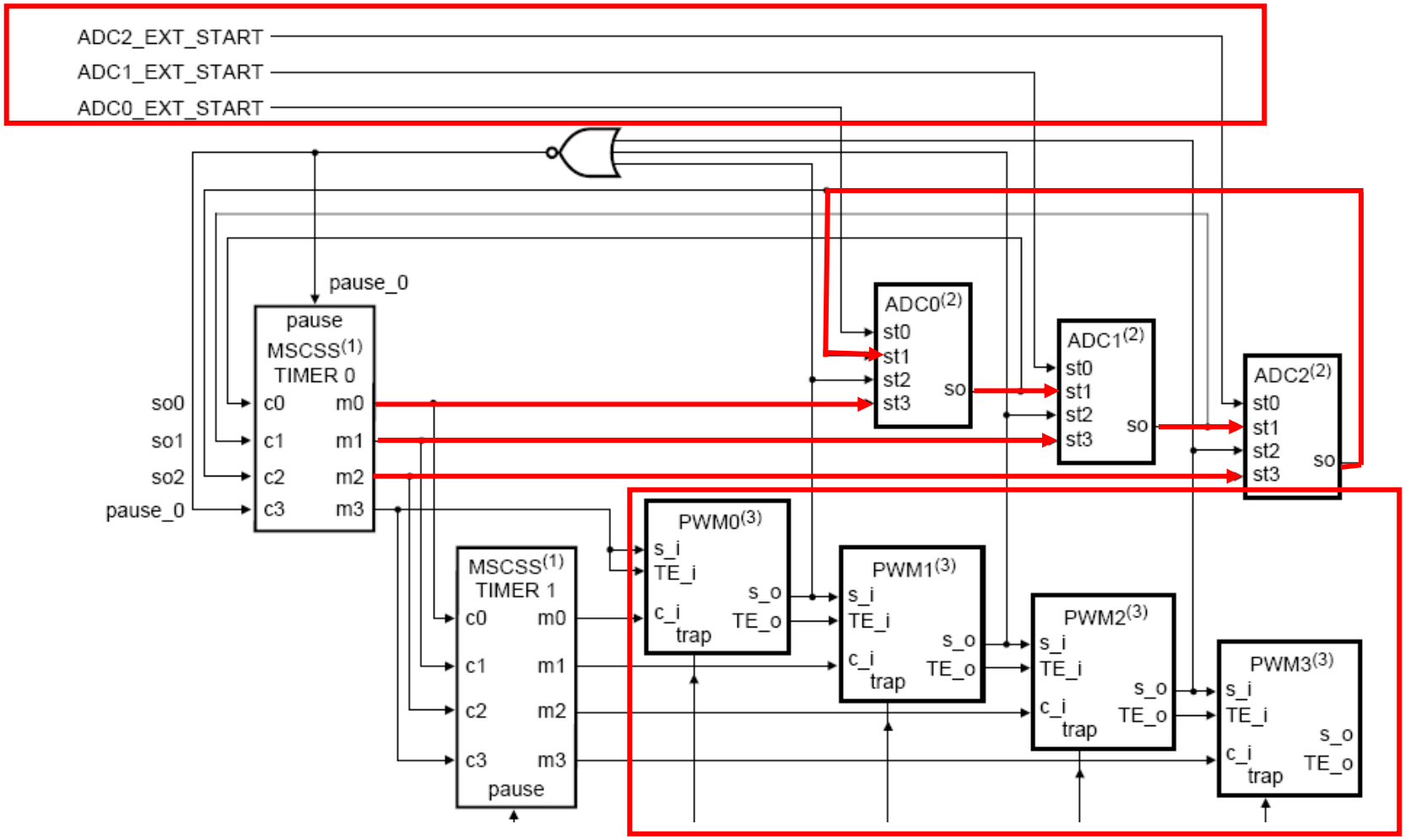
ADC- Key features

- Two 10-bit ADCs, 8-channels each, with **3.3 V** measurement range
- One 8-channel 10-bit ADC with **5.0 V** measurement range
- Total 24 analog inputs, with conversion times as low as **2.44 µs** per channel
- Each channel provides a compare function to minimize interrupts

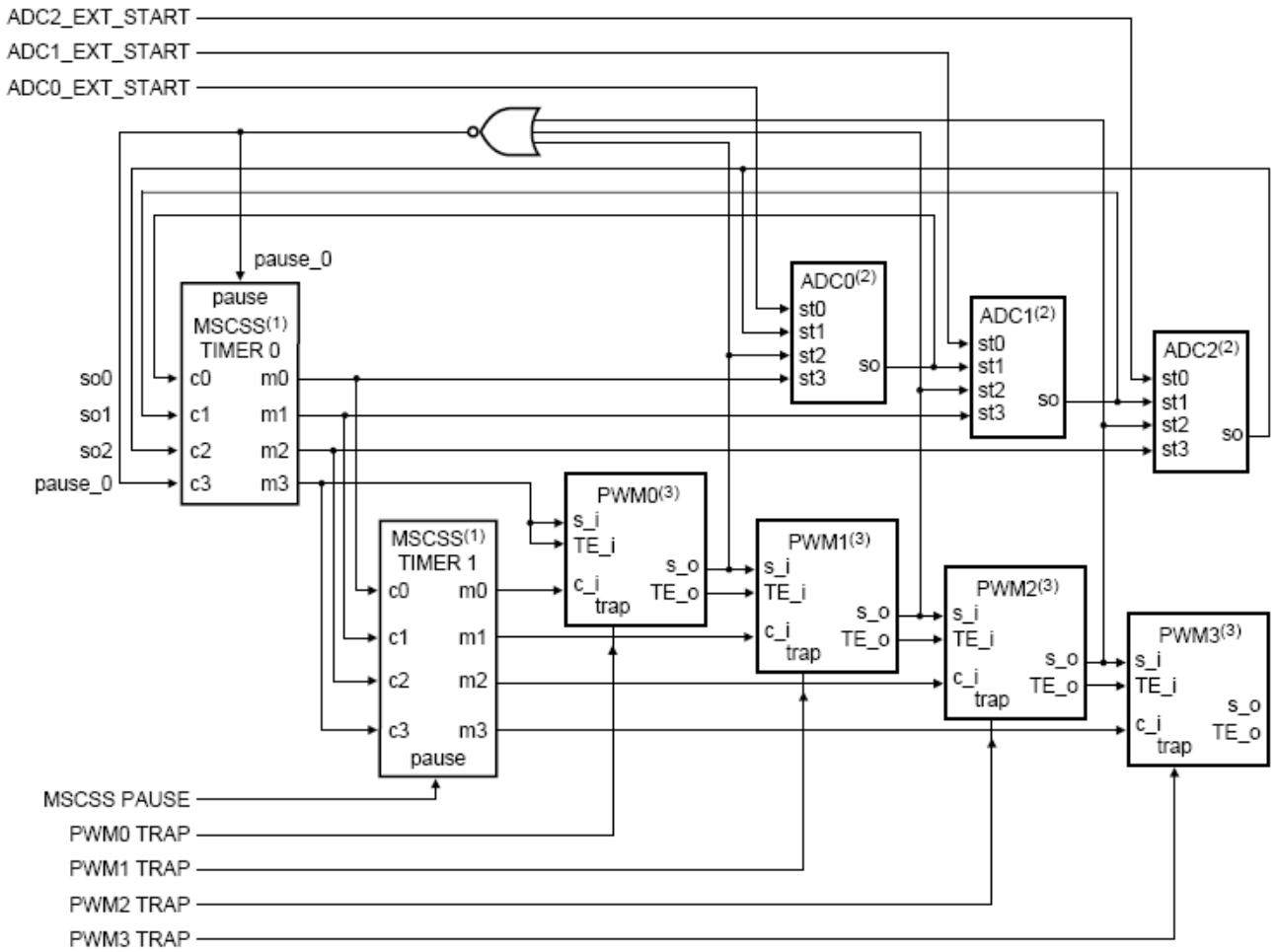
ADC Block Diagram



ADC Start Conditions

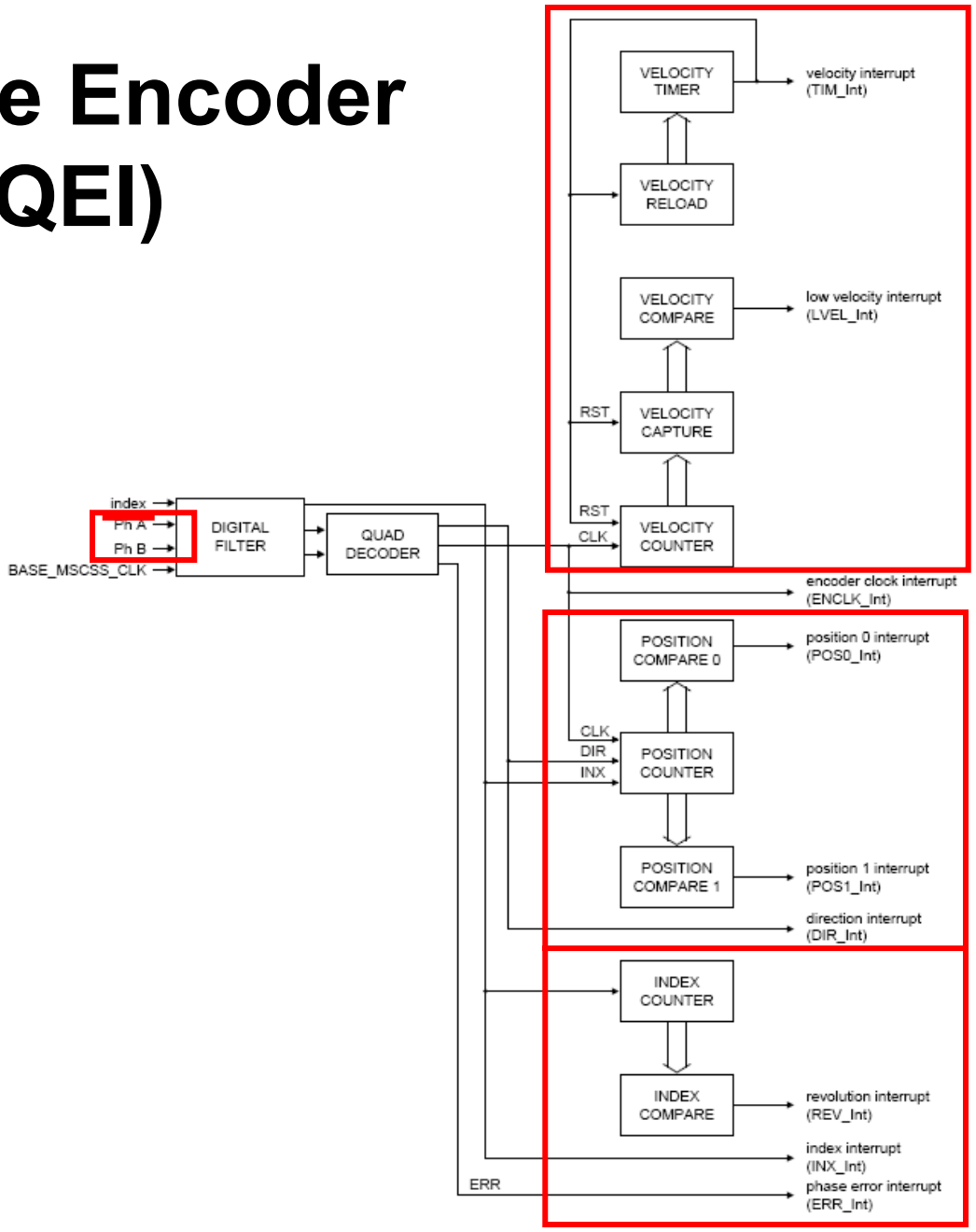


MSCSS- Possible Applications



- Voltage monitoring and level measurement
- Synchronized PWM events
- Synchronized PWM and ADC events
- Dimmer application using PWMs
- Sine wave generation
- Comparator

Quadrature Encoder Interface (QEI)

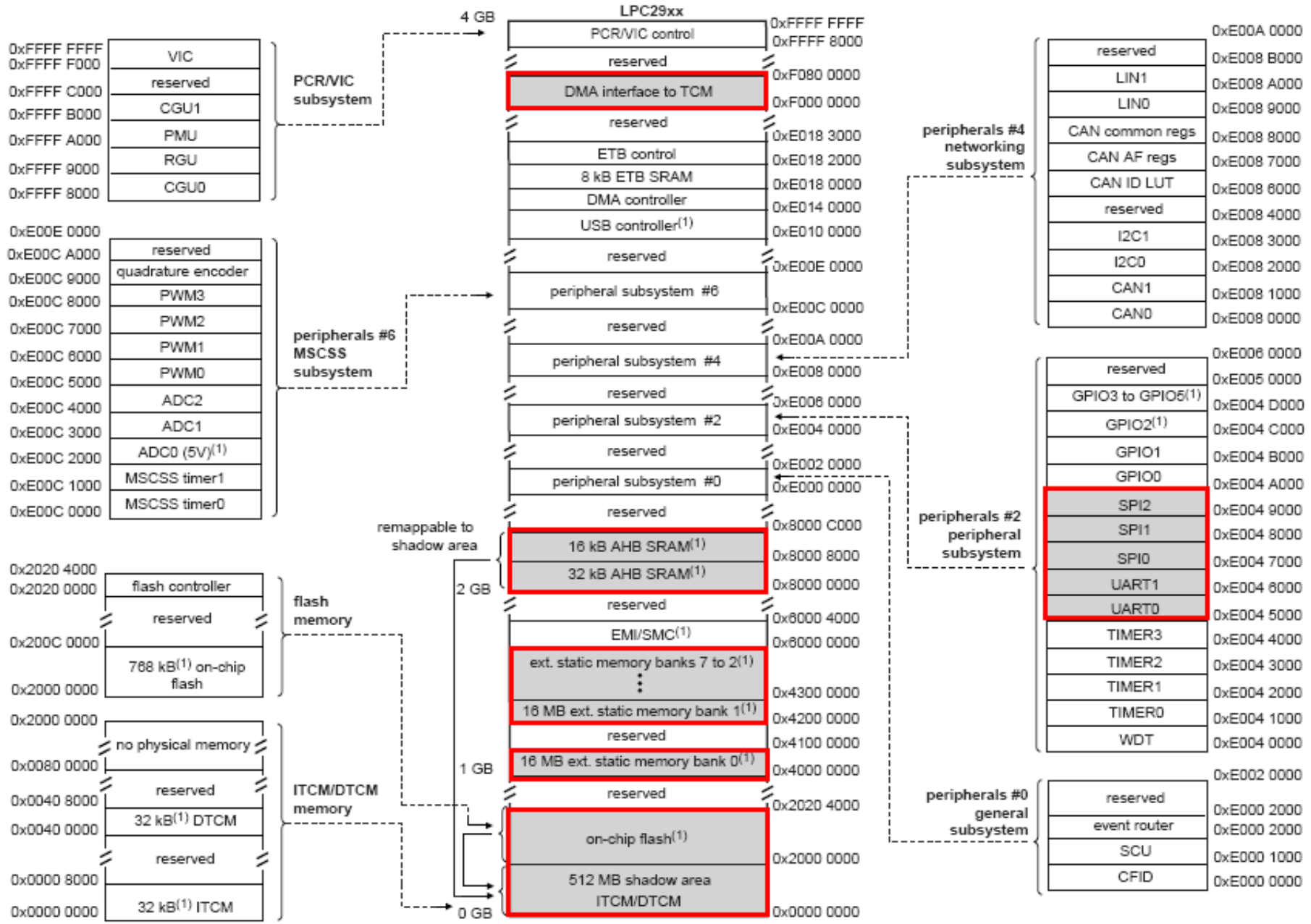


QEI- Key Features

- Tracks encoder position
- Digital filter with programmable delays for encoder input signals
- Programmable for 2X or 4X position counting.
- Velocity capture
- Index counter for revolution counting
- Can combine index and position interrupts to produce an interrupt for whole and partial revolution displacement

Other Peripherals

- GPDMA
- USB FS Host/Device/OTG Controllers


LPC29xx
4 GB
0xFFFF FFFF
PCR/VIC control
0xFFFF 8000
reserved
0xF080 0000
DMA interface to TCM
0xF000 0000
reserved
0xE018 3000
ETB control
0xE018 2000
8 kB ETB SRAM
0xE018 0000
DMA controller
0xE014 0000
USB controller(1)
0xE010 0000
reserved
0xE00E 0000
peripheral subsystem #6
0xE00C 0000
reserved
0xE00A 0000
peripheral subsystem #4
0xE008 0000
reserved
0xE006 0000
peripheral subsystem #2
0xE004 0000
reserved
0xE002 0000
peripheral subsystem #0
0xE000 0000
reserved
0x8000 C000
16 kB AHB SRAM(1)
0x8000 8000
32 kB AHB SRAM(1)
0x8000 0000
reserved
0x6000 4000
EMI/SMC(1)
0x6000 0000
ext. static memory banks 7 to 2(1)
0x4300 0000
16 MB ext. static memory bank 1(1)
0x4200 0000
reserved
0x4100 0000
16 MB ext. static memory bank 0(1)
0x4000 0000
reserved
0x2020 4000
on-chip flash(1)
0x2000 0000
512 MB shadow area ITCM/DTCM
0x0000 0000
2 GB
1 GB
0 GB
remappable to shadow area
0xFFFF FFFF
0xFFFF F000
VIC
reserved
0xFFFF C000
CGU1
0xFFFF B000
PMU
0xFFFF A000
RGU
0xFFFF 9000
CGU0
0xFFFF 8000
PCR/VIC subsystem
0xE00E 0000
0xE00C A000
reserved
quadrature encoder
0xE00C 9000
PWM3
0xE00C 8000
PWM2
0xE00C 7000
PWM1
0xE00C 6000
PWM0
0xE00C 5000
ADC2
0xE00C 4000
ADC1
0xE00C 3000
ADC0 (5V)(1)
0xE00C 2000
MSCSS timer1
0xE00C 1000
MSCSS timer0
0xE00C 0000
peripherals #6 MSCSS subsystem
0x2020 4000
0x2020 0000
flash controller
reserved
0x200C 0000
768 kB(1) on-chip flash
0x2000 0000
flash memory
0x2000 0000
no physical memory
0x0080 0000
reserved
0x0040 8000
32 kB(1) DTCM
0x0040 0000
reserved
0x0000 8000
32 kB(1) ITCM
0x0000 0000
ITCM/DTCM memory
peripherals #4 networking subsystem
0xE00A 0000
reserved
0xE008 B000
LIN1
0xE008 A000
LIN0
0xE008 9000
CAN common regs
0xE008 8000
CAN AF regs
0xE008 7000
CAN ID LUT
0xE008 6000
reserved
0xE008 4000
I2C1
0xE008 3000
I2C0
0xE008 2000
CAN1
0xE008 1000
CAN0
0xE008 0000
peripherals #2 peripheral subsystem
0xE006 0000
reserved
0xE005 0000
GPIO3 to GPIO5(1)
0xE004 D000
GPIO2(1)
0xE004 C000
GPIO1
0xE004 B000
GPIO0
0xE004 A000
SPI2
0xE004 9000
SPI1
0xE004 8000
SPI0
0xE004 7000
UART1
0xE004 6000
UART0
0xE004 5000
TIMER3
0xE004 4000
TIMER2
0xE004 3000
TIMER1
0xE004 2000
TIMER0
0xE004 1000
WDT
0xE004 0000
peripherals #0 general subsystem
0xE002 0000
reserved
0xE000 2000
event router
0xE000 2000
SCU
0xE000 1000
CFID
0xE000 0000

USB Portfolio

Core	Product	On-Chip Controller			No. of Ports	On-chip PHY
		Device	Host	OTG		
ARM968	LPC2921	FS	-	-	1	Yes
	LPC2923	FS	-	-	1	Yes
	LPC2925	FS	-	-	1	Yes
	LPC2927	FS	-	FS	1	Device
	LPC2929	FS	-	FS	1	Device
	LPC2930	FS	FS	FS	2	Device, Host
	LPC2939	FS	FS	FS	2	Device, Host

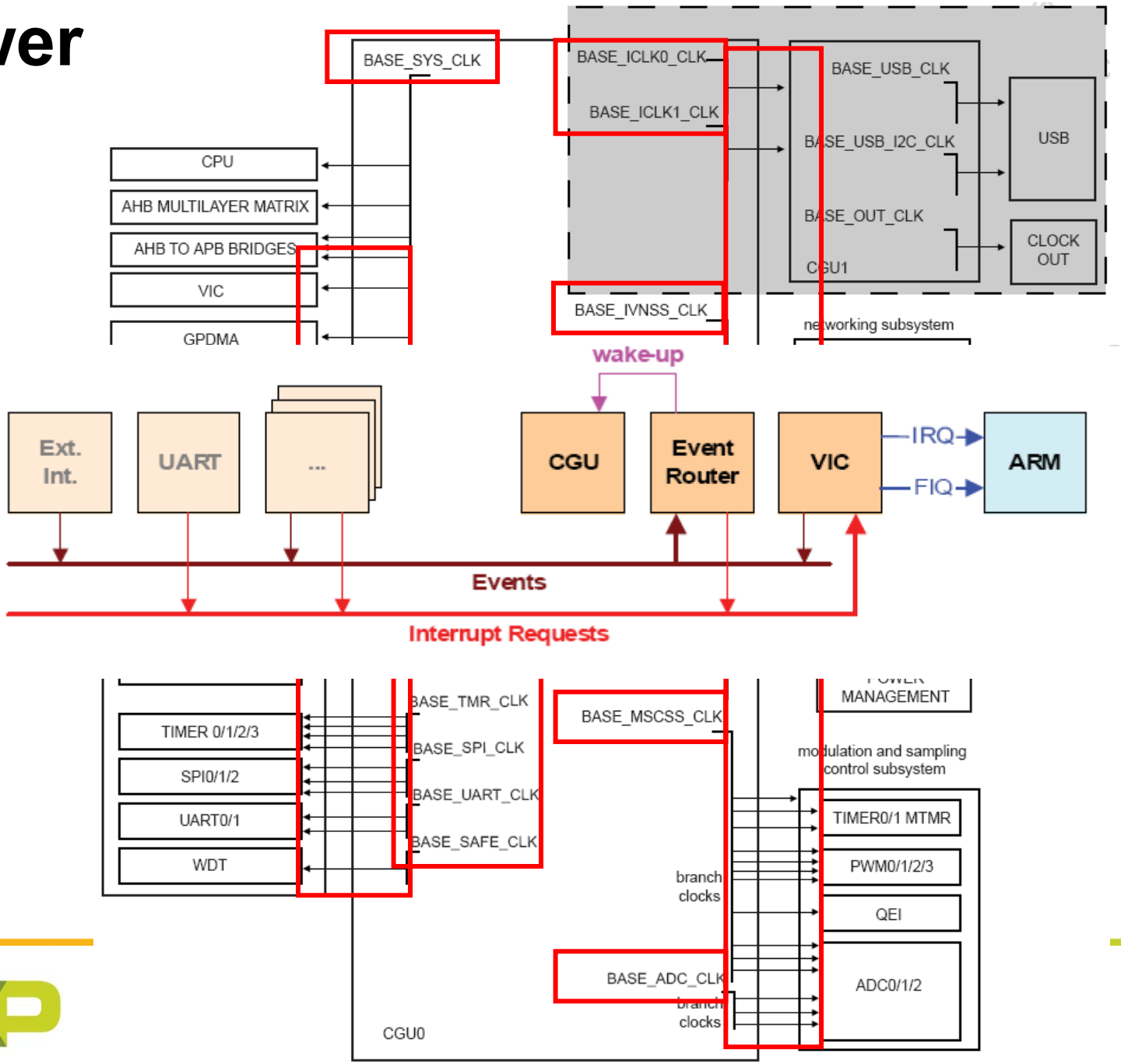
Notes: All devices (except LPC2927/29) with 2 ports can be used in the following combinations: Device (OTG) + Host, Host (OTG) + Host, Host + Device

USB Device/ Host/ OTG controllers

- Device
  - Supports 32 physical (16 logical) endpoints
  - Supports Control, Bulk, Interrupt and Isochronous endpoints
  - Scalable realization of endpoints at run time
  - Supports SoftConnect and GoodLink features
- Host controller
  - OHCI compliant
  - The Host Controller has four USB states visible to the SW Driver
- OTG
  - Fully compliant with On-The-Go supplement to the *USB 2.0 Specification, Revision 1.0a*
  - Hardware support for Host Negotiation Protocol (HNP)
  - Includes a programmable timer required for HNP and SRP
  - Supports any OTG transceiver compliant with the *OTG Transceiver Specification*

Power Modes

Power

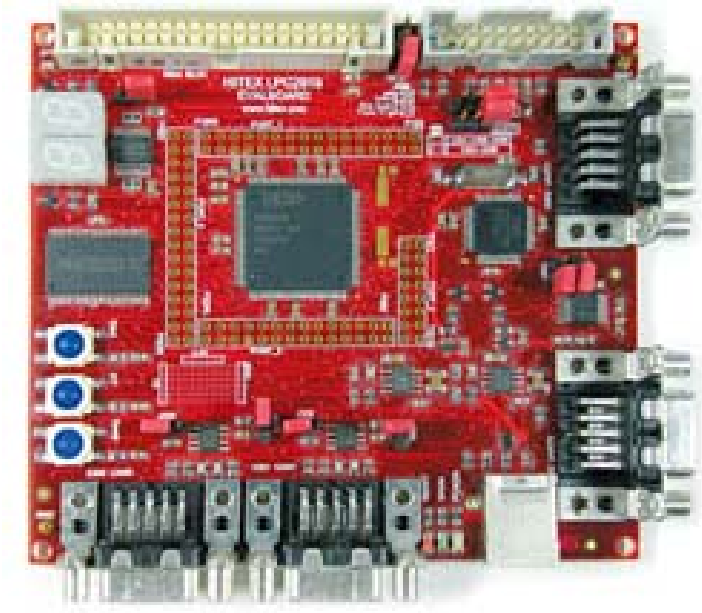

BASE_SYS_CLK
BASE_ICLK0_CLK
BASE_ICLK1_CLK
BASE_USB_CLK
BASE_USB_I2C_CLK
BASE_OUT_CLK
CGU1
USB
CLOCK OUT
BASE_IVNSS_CLK
networking subsystem
CPU
AHB MULTILAYER MATRIX
AHB TO APB BRIDGES
VIC
GPDMA
wake-up
Ext. Int.
UART
...
CGU
Event Router
VIC
IRQ
FIQ
ARM
Events
Interrupt Requests
BASE_TMR_CLK
BASE_SPI_CLK
BASE_UART_CLK
BASE_SAFE_CLK
TIMER 0/1/2/3
SPI0/1/2
UART0/1
WDT
BASE_MSCSS_CLK
MANAGEMENT
modulation and sampling control subsystem
TIMER0/1 MTMR
PWM0/1/2/3
QEI
ADC0/1/2
branch clocks
BASE_ADC_CLK
branch clocks
CGU0

Power Numbers- LPC2939

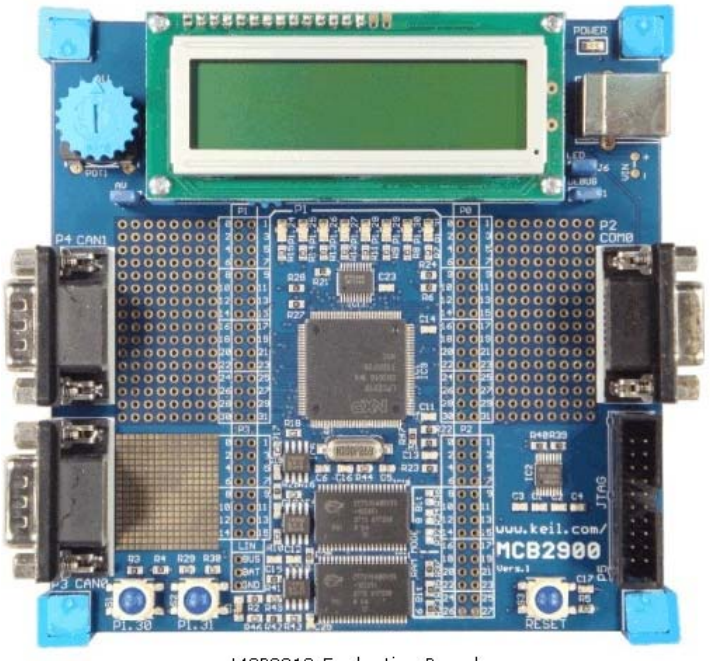
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Supplies						
Core supply						
$V_{DD(CORE)}$	core supply voltage		1.71	1.80	1.89	V
$I_{DD(CORE)}$	core supply current	ARM9 and all peripherals active at max clock speeds	-	1.1	2.5	mA/ MHz
		all clocks off	-	30	475	µA
I/O supply						

Tools

Evaluation Boards

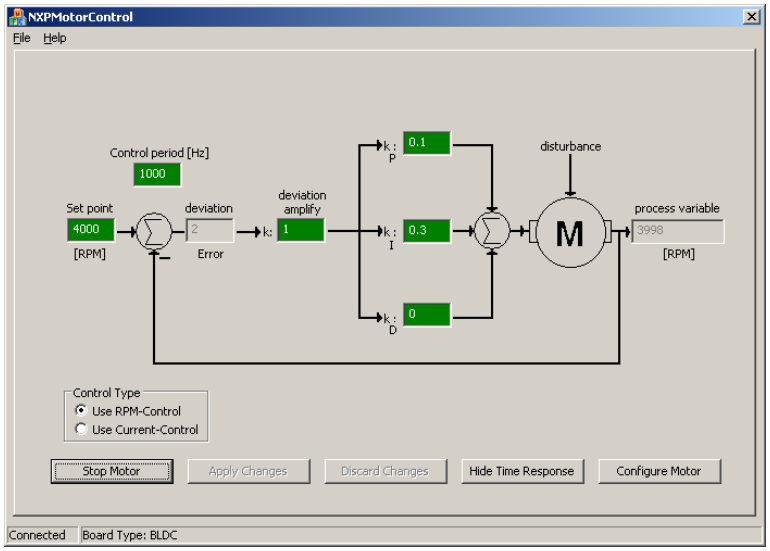


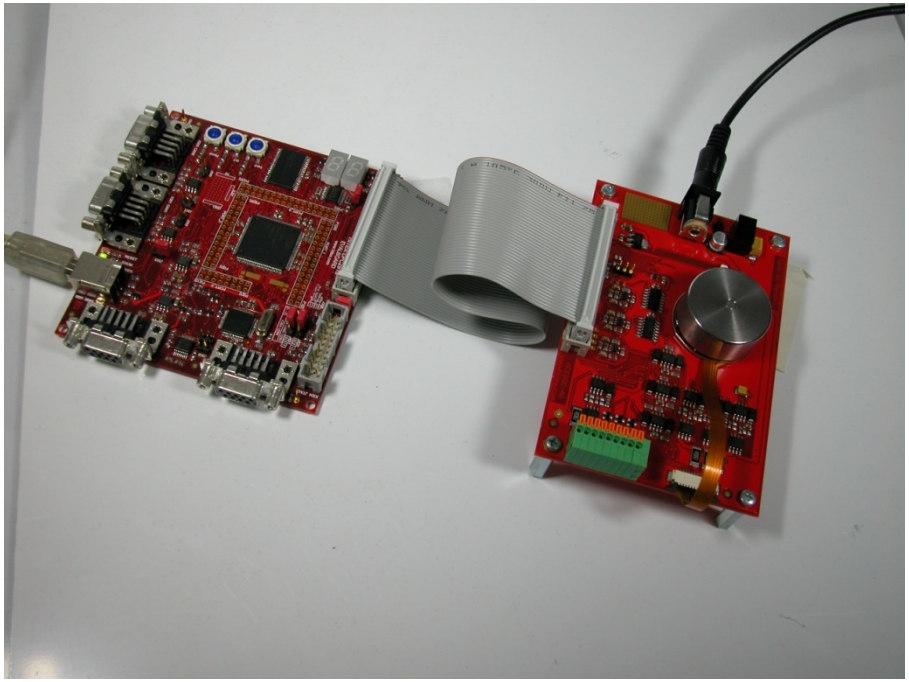
Hitex LPC2919 Board



Keil LPC2919 Board

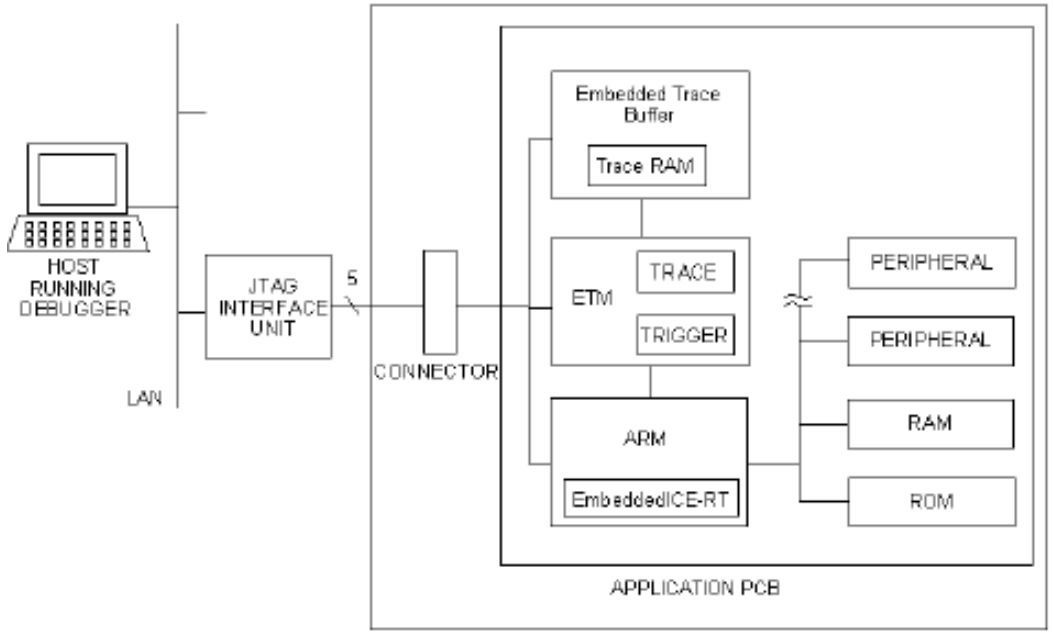
Motor Control Application





hitex DEVELOPMENT TOOLS

ETM, ETB


HOST
RUNNING
DEBUGGER
LAN
JTAG
INTERFACE
UNIT
5
CONNECTOR
Embedded Trace
Buffer
Trace RAM
ETM
TRACE
TRIGGER
ARM
EmbeddedICE-RT
PERIPHERAL
PERIPHERAL
RAM
ROM
APPLICATION PCB


USB
for ARM® Processors
IAR
SYSTEMS
JTAG SWD