ERRATA SHEET

Date: 2009 October 14
Document Release: Version 1.3
Device Affected: LPC1758

This errata sheet describes both the functional problems and any deviations from the electrical specifications known at the release date of this document.

Each deviation is assigned a number and its history is tracked in a table at the end of the document.

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NXP
Semiconductors

founded by Philips

Document revision history

Rev	Date	Description
1.3	October 14 2009	Added MCPWM.1
1.2	August 17 2009	Added Ethernet.1
1.1	July 06 2009	Added PCLKSELx.1
1.0	April 10 2009	First version

Identification

The typical LPC1758 devices have the following top-side marking:

LPC1758xxx

xxxxxxx

xxYYWW R[x]

The last/second to last letter in the third line (field ‘R’) will identify the device revision. This Errata Sheet covers the following revisions of the LPC1758:

Revision Identifier (R)	Comment
‘-’	Initial device revision

Field ‘YY’ states the year the device was manufactured. Field ‘WW’ states the week the device was manufactured during that year.

Errata Overview - Functional Problems

Functional Problem	Short Description	Device Revision the problem occurs in
PLL0.1	PLL0 (Main PLL) remains enabled and connected in Deep Sleep and Power-down modes	-
PCLKSELx.1	Peripheral Clock Selection Registers must be set before enabling and connecting PLL0	-
Ethernet.1	Ethernet Media Independent Interface Management (MIIM) Signals	-
MCPWM.1	Input pins (MCI0-2) on the Motor Control PWM peripheral are not functional	-

Errata Overview - AC/DC Deviations

AC/DC Deviation	Short Description	Device Revision the deviation occurs in
n/a	n/a	n/a

Errata Notes

Notes	Short Description	Device Revision the note applies to
n/a	n/a	n/a

Functional Problems of LPC1758

PLL0.1: PLL0 (Main PLL) remains enabled and connected in Deep Sleep and Power-down modes.

Introduction: If the main PLL (PLL0) is enabled and connected before entering Deep Sleep or Power-down modes, main PLL (PLL0) automatically turns off and disconnects after the chip enters Deep Sleep mode or Power-down mode leading to reduced power consumption.

Problem: If the main PLL (PLL0) is enabled and connected before entering Deep Sleep or Power-down modes, it will remain enabled and connected after the chip enters Deep Sleep mode or Power-down mode causing the power consumption to be higher.

Workaround: In the software, user must disable and disconnect the main PLL (PLL0) before entering Deep Sleep and Power-down modes to reduce the power consumption. This must be done only if the main PLL (PLL0) was enabled and connected before entering Deep Sleep mode or Power-down mode.

The code below demonstrates the steps to disable and disconnect the main PLL0:

```
PLL0CON     &= ~(1<<1);                  /*  Disconnect the main PLL (PLL0) */
PLL0FEED    = 0xAA;                     /*  Feed */
PLL0FEED    = 0x55;                      /* Feed */
while ((PLL0STAT & (1<<25)) != 0x00);      /*  Wait for main PLL (PLL0) to disconnect */
PLL0CON     &= ~(1<<0);                 /*  Turn off the main PLL (PLL0) */
PLL0FEED    = 0xAA;                      /*  Feed */
PLL0FEED    = 0x55;                      /*  Feed */
while ((PLL0STAT & (1<<24)) != 0x00);      /*  Wait for main PLL (PLL0) to shut down */
/************** Then enter into Deep sleep mode or Power-down mode *************************/
```

PCLKSELx.1: Peripheral Clock Selection Registers must be set before enabling and connecting PLL0

Introduction: A pair of bits in the Peripheral Clock Registers (PCLKSEL0 and PCLKSEL1) controls the rate of the clock signal that will be supplied to APB0 and APB1 peripherals.

Problem: If the Peripheral Clock Registers (PCLKSEL0 and PCLKSEL1) are set or changed after PLL0 is enabled and connected, the value written into the Peripheral Clock Selection Registers may not take effect. It is not possible to change the Peripheral Clock Selection settings once PLL0 is enabled and connected.

Workaround: Peripheral Clock Selection Registers must be set before enabling and connecting PLL0.

Ethernet.1: Ethernet Media Independent Interface Management (MIIM) Signals

Introduction: The LPC1758 has Ethernet interface, which interfaces between an off-chip Ethernet PHY using the RMII (Reduced Media Interface Management) protocol, and the on-chip Media Independent Interface Management (MIIM) serial bus. The off-chip Ethernet PHY registers are accessible via the Media Independent Interface Management (MIIM) interface. This interface consists of the Ethernet MIIM clock (ENET_MDC) signal and Ethernet MIIM data input and output (ENET_MDIO) signal.

Problem: The LPC1758 does not support the MIIM signals.

Workaround: The MIIM interface signals can be emulated in software by utilizing GPIO. There is a software implementation available. Please see Application Note (AN10859) on www.nxp.com.

MCPWM.1: Input pins (MCI0-2) on the Motor Control PWM peripheral are not functional

Introduction: On the LPC1758, the Motor Control PWM (MCPWM) peripheral is optimized for three-phase AC and DC motor control applications and can also be used in applications which require timing, counting, capture, and comparison. The MCPWM contains three input pins (MCI0-2) for PWM channels 0, 1, and 2. The inputs can be used as feedbacks for controlling brushless DC motors with Hall sensors, and also can be used to trigger a Timer/Counter's (TC) capture or increment a channel's TC when MCPWM is configured as a timer/counter.

Problem: The input pins (MCI0-2) are not functional.

Workaround: The GPIO interrupts on port 0 or port 2 can be used instead of the MCPWM MCI0-2 pins. The GPIO interrupts give the ability to trigger an interrupt on both the rising and falling edge; therefore, all six states of the connected hall sensor can be detected through an interrupt.