MPC89L556X2

8-Bit Micro-controller

Features

- 8-bit 80C52-compatible Microcontroller
  - Fully instruction set compatible
  - Pin-to-pin package compatible with standard 80C52
- Power voltage range: V_{CC}= 2.4V ~ 3.6V
- Optional 12 clocks or 6 clocks per machine cycles operation
- Operating speed: Up to 45MHz for both 12 clocks and 6 clocks per machine cycle
- Memory architecture
  - 512 bytes on-chip RAM
  - 64K bytes on-chip flash memory
  - 64K bytes program and data memory address spaces
  - Provides In-system programming (ISP) to update the program code
- 8 channels of an 8-bit A/D converter, shared with the port 1
- Four 8-bit bi-directional I/O Ports (P0, P1, P2, P3) and P4.0~P4.3, and except P1 is not 5V-tolerant, P0/2/3/4 all are 5V-tolerant
- Three 16-bit programmable timer/counters, Timer2 is an up/down counter with programmable clock output on P1.0
- One watchdog timer
- One enhanced UART, provides frame-error detection and hardware address- recognition
- Power saving mode
  - Idle and Power-down modes
  - Waking up the power-down mode by P3.2 and P3.3
- Dual DPTR for fast-moving external data memory
- 6-source and 4-level interrupt structure
- Inhibit ALE-signal output for the low EMI
- 3-level code protection
- Packages:
  - PDIP 40: MPC89L556X2
  - PLCC 44: MPC89L556X2P
  - PQFP 44: MPC89L556X2F

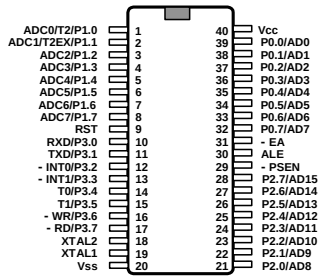
General Description

MPC89L556X2 is a powerful 8-bit 80C52-compatible Microcontroller with advanced embedded flash memory technology. It contains a 64kx8 Flash memory, a 512x8 RAM, a watch-dog timer, a full duplex UART, 3 timer/counters, dual DPTR, and 8 channels of 8-bit analog-to-digital converter. In additional, MPC89L556X2 is designed with an new accelerative architecture, its speed can executes twice faster than a conventional 80C52 series, and the users can easily change the 12 clocks to 6 clocks per machine cycle operation on the programmer.

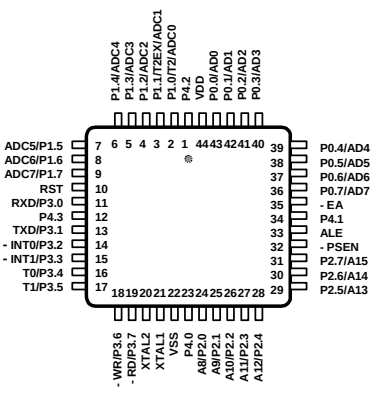
Pin Description

PIN Name	I/O	Description
P0.0 ~ P0.7	I/O	Port 0 is bi-directional I/O port with an open-drain. Port 0 is also the multiplexed low-order address and data bus during accesses to the external program and data memory.
P1.0 ~ P1.7	I/O	Port 1 is a general purpose I/O port with the internal pull-ups and also provides the alternate functions for the analog input channels of an 8-bit A/D converter: ADC0/T2/P1.0: ADC0 or Timer/Counter 2 external count input/Clock-out ADC1/T2EX/P1.1: ADC1 or Timer/Counter 2 Reload/Capture/Direction control ADC2/P1.2 ~ ADC7/P1.7: ADC2 ~ADC7 analog signal inputs
P2.0 ~ P2.7	I/O	Port 2 is an 8-bit bi-directional I/O port with internal pull-ups. Except acting as GPIO, Port 2 outputs the high-order address byte during accessing the external data and program memory.
P3.0 ~ P3.7	I/O	Port 3 is a GPIO with internal pull-ups and also serves the special functions of the conventional 80C52 series, as listed below: RXD/P3.0: Serial input TXD/P3.1: Serial output $\overline{INT0}$/P3.2: External interrupt 0 $\overline{INT1}$/P3.3: External interrupt 1 T0/P3.4: Timer 0 external Input T1/P3.5: Timer 1 external Input $\overline{WR}$/P3.6: External data memory write strobe $\overline{RD}$/P3.7: External data memory read strobe
P4.0 ~ P4.3	I/O	Port 4 is an extended I/O port such like Port 1, but it can be available only on 44-PLCC and 44-PQFP.
RST	I	A high level on this pin for at least two machine cycles to reset this device.
XTAL1	I	Input to the oscillator amplifier.
XTAL2	O	Output from the oscillator amplifier, and also is the inversion of XTAL1.
$\overline{EA}$	I	$\overline{EA}$ (External Access) has to be externally held low to enable the device to fetch code from the external program memory.
$\overline{PSEN}$	O	$\overline{PSEN}$ (Program Strobe Enable) is low active, when the read strobe to the external program memory.
V_{SS}	I	Ground input.
V_{DD}	I	Power supply input.

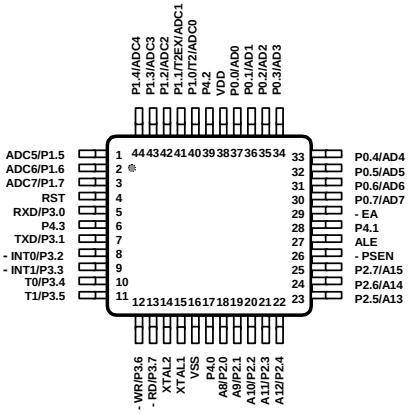
Pin Configurations



MPC89L556X2

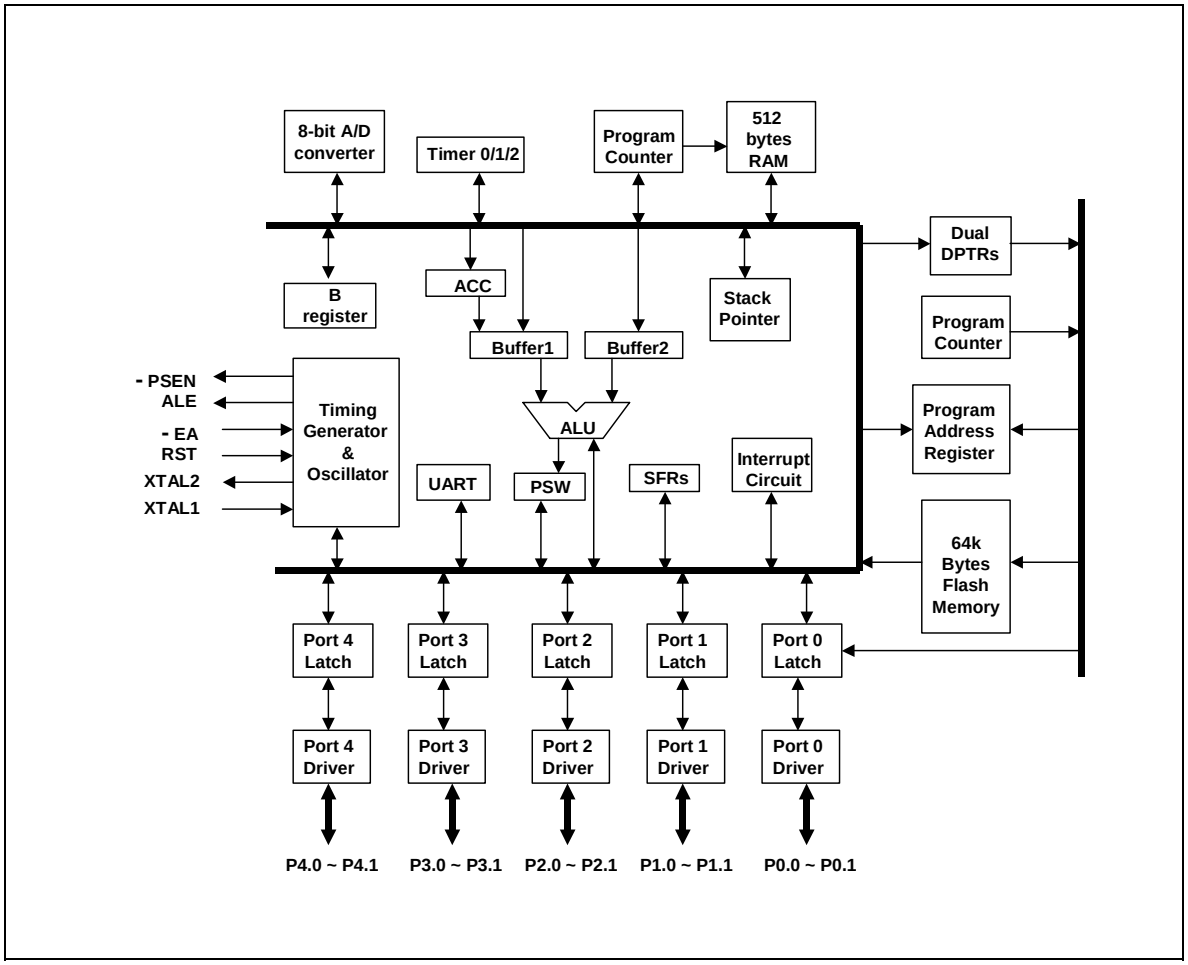


MPC89L556X2P



MPC89L516X2F

Block Diagram



Special Function Registers

SYMBOL	DESCRIPTION	ADDRESS	BIT ADDRESS AND SYMBOL MSB							LSB	INITAL VALUE
+ P0	Port 0	80H	**87H** AD7	**86H** AD6	**85H** AD5	**84H** AD4	**83H** AD3	**82H** AD2	**81H** AD1	**80H** AD0	11111111B
SP	Stack Pointer	81H									00000111B
DPL	Data Pointer Low	82H									00000000B
DPH	Data Pointer High	83H									00000000B
PCON	Power Control	87H	SMOD	-	-	POF	GF1	GF0	PD	IDL	00XX0000B
+ TCON	Timer Control	88H	**9FH** TF1	**9EH** TR1	**9DH** TF0	**9CH** TR0	**9BH** IE1	**9AH** IT1	**89H** IE0	**88H** IT0	00000000B
TMOD	Timer Mode	89H	GATE	C/-T	M1	M0	GATE	C/-T	M1	M0	00000000B
TL0	Timer Low 0	8AH									00000000B
TL1	Timer Low 1	8BH									00000000B
TH0	Timer High 0	8CH									00000000B
TH1	Timer High 1	8DH									00000000B
AUXR	Auxiliary	8EH	-	-	-	-	-	-	-	AO	XXXXXXX0B
+ P1	Port 1	90H	**97H** -	**96H** -	**95H** -	**94H** -	**93H** -	**92H** -	**91H** T2EX	**90H** T2	11111111B
P1SFAD	Port 1 Special Function	97H	EAI7	EAI6	EAI5	EAI4	EAI3	EAI2	EAI1	EAI0	00000000B
+ SCON	Serial Control	98H	**9FH** SM0/FE	**9EH** SM1	**9DH** SM2	**9CH** REN	**9BH** TB8	**9AH** RB8	**99H** TI	**98H** RI	00000000B
SBUF	Serial Data Buffer	99H									XXXXXXXXB
+ P2	Port 2	A0H	**A7H** A15	**A6H** A14	**A5H** A13	**A4H** A12	**A3H** A11	**A2H** A10	**A1H** A9	**A0H** A8	11111111B
AUXR1	Auxiliary 1	A2H	-	-	-	-	-	-	-	DPS	XXXXXXX0B
+ IE	Interrupt Enable	A8H	**AFH** EA	**AEH** EAD	**ADH** ET2	**ACH** ES	**ABH** ET1	**AAH** EX1	**A9H** ET0	**A8H** EX0	00000000B
SADDR	Slave Address	A9H									00000000B
+ P3	Port 3	B0H	**B7H** -RD	**B6H** -WR	**B5H** T1	**B4H** T0	**B3H** -INT1	**B2H** -INT0	**B1H** TXD	**B0H** RXD	11111111B
IPH	Interrupt Priority High	B7H	-	-	PT2H	PSH	PT1H	PX1H	PT0H	PX0H	X0000000B
+ IP	Interrupt Priority	B8H	**BFH** -	**BEH** PAD	**BDH** PT2	**BCH** PS	**BBH** PT1	**BAH** PX1	**B9H** PT0	**B8H** PX0	X0000000B
SADEN	Slave Address Mask	B9H									00000000B
+ P4	Port 4	C0H	**C7H** -	**C6H** -	**C5H** -	**C4H** -	**C3H** P4.3	**C2H** P4.2	**C1H** P4.1	**C0H** P4.0	XXXXXX11B

SYMBOL	DESCRIPTION	ADDRESS	BIT ADDRESS AND SYMBOL MSB							LSB	INITAL VALUE
ADCON	ADC control	C5H	-	-	-	ADCI	ADCS	CHS2	CHS1	CHS0	XXX00000B
ADAT	ADC result	C6H									XXXXXXXXB
+ T2CON	Timer 2 Control	C8H	**CFH** TF2	**CEH** EXF2	**CDH** RCLK	**CCH** TCLK	**CBH** EXEN2	**CAH** TR2	**C9H** C/-T2	**C8H** CP/-RL	00000000B
T2MOD	Timer2 Mode Control	C9H	-	-	-	-	-	-	T2OE	DCEN	XXXXXX00B
RCAP2L	Timer2 Capture Low	CAH									00000000B
RCAP2H	Timer2 Capture High	CBH									00000000B
TL2	Timer Low 2	CCH									00000000B
TH2	Timer High 2	CDH									00000000B
+ PSW	Program Status Word	D0H	**D7H** CY	**D6H** AC	**D5H** F0	**D4H** RS1	**D3H** RS0	**D2H** OV	**D1H** -	**D0H** P	000000X0B
+ ACC	Accumulator	E0H	**E7H**	**E6H**	**E5H**	**E4H**	**E3H**	**E2H**	**E1H**	**E0H**	00000000B
WDTCR	Watch-dog Timer	E1H	-	-	WDEN	WDCL	WDIDL	PS2	PS1	PS0	XX000000B
IFD	ISP Flash Data	E2H									00000000B
IFADRH	ISP High Flash Address	E3H									00000000B
IFADRL	ISP Low Flash Address	E4H									00000000B
IFMT	ISP Mode Table	E5H	-	-	-	-					XXXX0000B
SCMD	ISP Sequential Command Data	E6H									XXXXXXXXB
ISPCR	ISP Control Register	E7H	ISPEN	BS	SRST	-	-	ICK2	ICK1	ICK0	000XX000B
+ B	B Register	F0H	**F7H**	**F6H**	**F5H**	**F4H**	**F3H**	**F2H**	**F1H**	**F0H**	00000000B

Notes:

1.The SFRs that are marked with a plus sign (**+**) are both byte-addressable and bit-addressable.

Functional Description

The MPC89L556X2 architecture consists of an enhanced 80C52 micro-controller, a 64k bytes flash memory, 512 bytes on-chip RAM, three timer/counters, a serial port, dual DPTR and 8 channels of 8-bit analog-to-digital converter. The micro-controller supports fully compatible instruction with standard 80C52, and also can address both a 64K program memory space and a 64K data memory space.

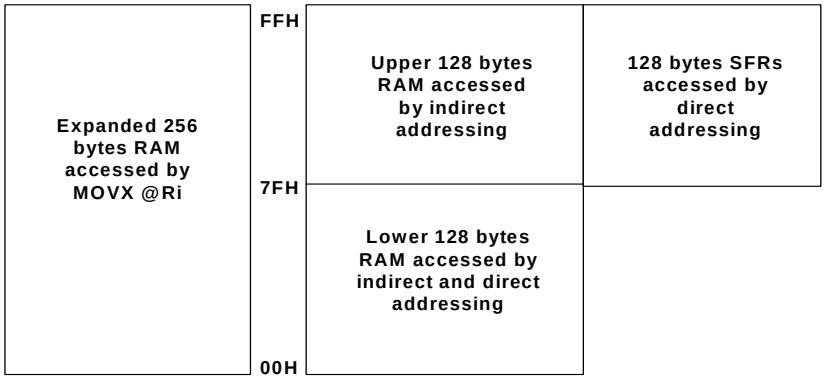
Memory Structure

There are 256 bytes on-chip RAM, 256 bytes on-chip expanded RAM (EX-RAM) and a 64k bytes flash memory available for MPC89L556X2. The internal data memory space is divided into four blocks: the lower 128 bytes RAM, the upper 128 bytes RAM, 128 bytes SFR and 256 bytes expanded RAM.

The four blocks are:

- The lower 128 bytes (00H~7FH) are accessed by direct and indirect addressing
- The upper 128 bytes (80H~FFH) are accessed by indirect addressing only
- The special function registers (SFR: 80H~FFH) are accessed by direct addressing only
- The 256 bytes expanded RAM (EX-RAM: 00H~ FFH) are indirectly accessed by the move external data memory instruction, MOVX @Ri, only

The on-Chip RAM is mapped as the following figure. MPC89L556X2 also provides an expanded 256 bytes of RAM on the chip. These bytes are only accessed by the two instructions, using MOVX A, @Ri for the reading and MOVX @Ri, A for the writing. When these two instructions are executed, there is no influence on P0. This is different from the standard 80C52 which P0 emits the address and is accessed the data in/out. In other words, only MOVX @Ri instruction is fixed to access on-chip 256 bytes EX-RAM, and for MOVX @DPTR instruction, it is used to access the external data memory higher than EX-RAM, and can be addressing up to 64K bytes.



Timer/Counter

MPC89L556X2 has three timer/counters. All of them are the same with the standard 80C52. But Timer2 supports the auto-reload up-down mode, which is a new-added function.

1. Timer0 and Timer1

These Timers can be configured as four modes: 1. Mode0 is 13-bit counter, 2. Mode1 is 16-bit counter, 3. Mode2 is 8-bit counter with automatic reload. 4. Mode3 can separate two 8-bit counters, and these modes are all the same with the standard 80C52.

2. Timer2

Timer2 has four operation modes: Capture mode, Auto-reload up-only mode, Auto-reload up-down mode and Baud-rate generator mode. MPC89L556X2's Timer 2 also provides a programmable clock-out on P1.0.

Auto-Reload Up-Only Mode

In Auto-reload up-only mode of the standard 80C52, Timer2 can be configured to count up with a software-defined value to be reloaded. When reset is applied the DCEN =0 and CP/$\overline{RL2}$ =0, Timer2 is at the auto-reload up-only mode. An overflow on Timer2 or 1-to-0 transition on T2EX pin will load RCAP2H and RCAP2L contents onto Timer2, also set TF2 and EXF2, respectively (See Figure 1).

Auto-Reload Up-Down Mode

Auto-reload up-down mode is a new-added powerful function. Timer2 can be configured to count up or down. When DCEN =1 and CP/$\overline{RL2}$ =0, Timer2 is at the auto-reload up-down mode. The counting direction is determined by T2EX pin. If T2EX=0, counting up, otherwise counting down. An overflow on Timer2 will set TF2 and toggle EXF2. EXF2 cannot generate the interrupt request in this mode. If the counting direction is DOWN, the overflow loads #FFFFh onto Timer2. Otherwise, the overflow would load RCAP2H, RCAP2L contents onto Timer2 if the counting direction is UP (See Figure 2).

Programmable Clock-out

When T2OE bit (in the T2MOD) is set and C/$\overline{T}$ (in T2CON) bit is cleared, Timer 2 overflow pulse will toggle P1.0 pin latch to generate a 50% duty clock. In this clock-out mode, Timer 2's rollovers will not generate an interrupt. The clock-out frequency is determined by the following equation:

Oscillator frequency / (N x (65536 – RCAP2H, RCAP2L)),

Where: N=2 for 6 clock mode, N=4 for 12 clock mode,

(RCAP2H, RCAP2L)= the content of RCAP2H and RCAP2L stored as a 16-bit integer-unsigned.

TMOD (Timer Mode register, Address: 0C9H)

LSB

-	-	-	-	-	-	T2OE	DCEN

- T2OE: Timer 2 Output Enable. It enables the clock-out function of Timer 2 on P1.0 by setting.
- DCEN: Down Count Enable. It allows Timer 2 to be configured as an up/down counter by setting.

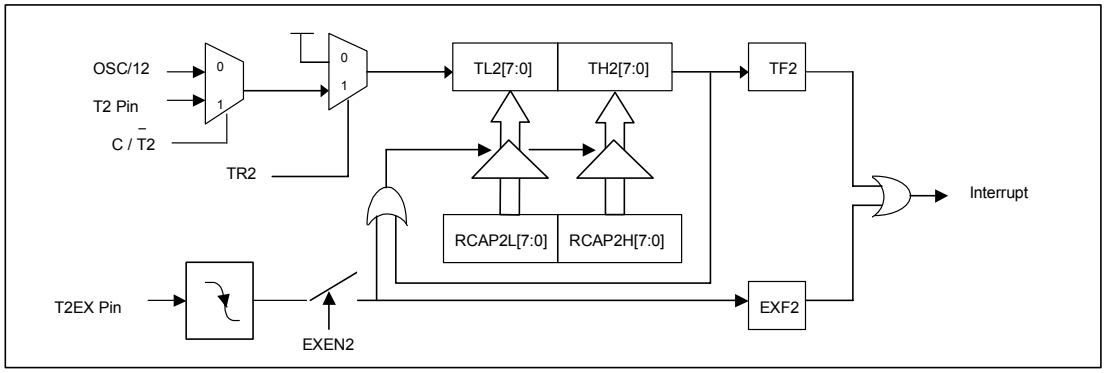


Figure 1: Auto-Reload Up-only Mode

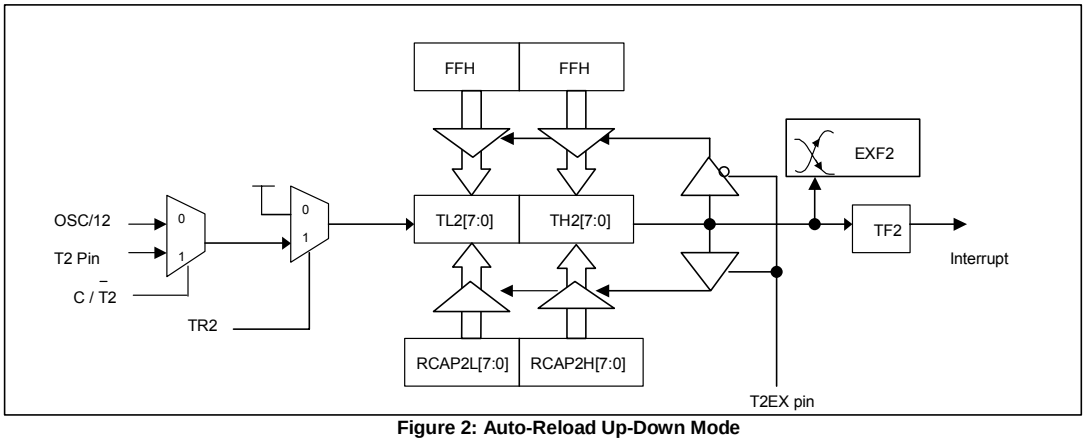


Figure 2: Auto-Reload Up-Down Mode

Interrupt Structure

MPC89L556X2 has a 6-source and 4-level interrupt structures. Each interrupt source can be individually enabled or disabled by setting or clearing a bit in the IE SFR. This register also contains a global disable bit (EA), which can be reset all interrupts to disable at once. Each interrupt source has two corresponding bits to represent its priority. One is located in IPH SFR, and the other is placed in the IP SFR. Higher-priority interrupt request will not be interrupted by lower-priority interrupt request. If both interrupt requests from different priority levels are received simultaneously, the request from the higher priority would be serviced. If both interrupt requests from the same priority levels are received simultaneously, an internal polling sequence determines which request would be serviced. The following interrupt table shows the internal polling sequence in the same priority level and the interrupt vector address.

Interrupt Vector and Priority Table

Source	Vector Address	Priority Level
External interrupt 0	03H	1 (Highest)
Timer 0	0BH	2
External interrupt 1	13H	3
Timer 1	1BH	4
Serial port	23H	5
Timer 2	2BH	6
ADC	33H	7 (Lowest)

IE (Interrupt Enable register, Address: 0A8H)

LSB

EA	-	ET2	ES	ET1	EX1	ET0	EX0

- EA: Global disables all interrupts when cleared, EA=0.
- ET2: When set, enables Timer 2 interrupt.
- ES: When set, enables the serial port interrupt.
- ET1: When set, enables Timer 1 interrupt.
- EX1: When set, enables external interrupt 1.
- ET0: When set, enables Timer 0 interrupt.
- EX0: When set, enables external interrupt 0.

IP (Interrupt Priority register, Address: 0B8H)

LSB

-	-	PT2	PS	PT1	PX1	PT0	PX0

- PT2: PT2=1 sets the Timer 2 to high priority level.
- PS: PS=1 sets the serial port to high priority level.
- PT1: PT1=1 sets the Timer 1 to high priority level.
- PX1: PX1=1 sets the external interrupt 1 to high priority level.
- PT0: PT0=1 sets the Timer 0 to high priority level.
- PX0: PX0=1 sets the external interrupt 0 to high priority level.

IPH (Interrupt Priority High register, Address: 0B7H)

LSB

-	-	PT2H	PSH	PT1H	PX1H	PT0H	PX0H

- PT2H: PT2H=1 sets the Timer 2 to higher priority level.
- PSH: PSH=1 sets the serial port to higher priority level.
- PT1H: PT1H=1 sets the Timer 1 to higher priority level.
- PX1H: PX1H=1 sets the external interrupt 1 to higher priority level.
- PT0H: PT0H=1 sets the Timer 0 to higher priority level.
- PX0H: PX0H=1 sets the external interrupt 0 to higher priority level.

There are three SFRs (IE, IP and IPH) to form the 4-level priority interrupt. The priority of each interrupt is determined as the following table:

Interrupt Priority Level Table

IPH	IP	Interrupt Priority Level
1	1	Level 3(Highest)
1	0	Level 2
0	1	Level 1
0	0	Level 0 (Lowest)

I/O Ports

MPC89L556X2's port structure has the same I/O ports as the standard 80C52, and an expanded bit-addressable port 4. The address of the port 4 is 0C0H. The port 4 has only 4 pins (P4.0 ~ P4.3), and is also available on 44-pin PLCC and 44-pin PQFP. Therefore, only four bits (P4<3:0>) in the P4 SFR can be used. In additional, the port 1 pins are also shared with the 8-bit A/D converter inputs (ADC0~ADC7).

Analog-to-Digital-Converter (ADC)

The ADC on MPC89L556X2 is an 8-bit resolution, successive-approximation approach, medium-speed A/D converter. V_{REFP}/V_{REFM} is the positive/negative reference voltage input for internal voltage-scaling DAC use, the typical sink current on it is 600uA ~ 1mA. For MPC89L556X2, these two references are internally tied to VDD and GND, separately.

Conversion is invoked since ADCS bit is set. The converter takes around 7.5 machine cycles to sample analog input data and extra 9.5 machine cycles is needed in successive-approximation steps. Total conversion time is 17 machine cycles, which no matter what system clock is. Analog input source comes from Port1 with the corresponding P1SFAD bits set. One of the eight-channels is multiplexed by analog multiplexer into the comparator. When conversion is completed, the result will be saved onto ADC register if and only if ADCI is not set. After the result are loaded onto ADC register, ADCI will be set and generate interrupt. ADCI should be cleared by software, not be automatically cleared by hardware. The ADC's interrupt vectors to a ROM space address, #33H.

ADCON (ADC Control Register, Address: 0C5H)

LSB

-	-	-	ADCI	ADCS	CHS2	CHS1	CHS0

CHS2 ~ CHS0: Used to select analog input channel from P1 pins.

ADCS: ADC start bit, which enable ADC conversion.

ADCI: ADC interrupt flag.

CHS2	CHS1	CHS0	Analog Input Channel
0	0	0	P1.0
0	0	1	P1.1
0	1	0	P1.2
0	1	1	P1.3
1	0	0	P1.4
1	0	1	P1.5
1	1	0	P1.6
1	1	1	P1.7

Note: The corresponding bits in P1SFAD need to be set if Port1 are used for ADC channels.

ADC (ADC Result Register, Address: 0C6H)

LSB

7	6	5	4	3	2	1	0

The ADC result can be calculated from the following formula: $256 \times (V_{IN} - V_{GND}) / (V_{VDD} - V_{GND})$

P1SFAD (P1 Special Function for ADC analog input, Address: 097H)

LSB

7	6	5	4	3	2	1	0

When set to “1”, it enables the bit of Port1 to become A/D input, and its internal pull-high resistor is disabled.

WatchDog Timer (WDT)

The Watchdog timer (WDT) is organized as a 15-bit free-running counter that will generate the reset to MPC89L556X2 if the WDT overflow. The WDT is very useful for the system that may be sensitive by the power glitches. The power noise and the disturbances of the electro-magnetic devices will cause the abnormal operation. By clearing this WDT periodically, the user can easily recover this uncertain error. MPC89L556X2 has a programmable pre-scale (PS0~PS2) to as the time base source of the WDT. To enable the WDT by setting the WDEN bit in the WDTCR SFR, then the 15-bit free-running counter starts to count with the pre-scale value. It will generate the reset signal when the overflow occurs. Generally, the user must clear the 15-bit free-running counter and the pre-scale by writing 1 to the WDCL bit in the WDTCR SFR before WDT's overflow occurs.

The WDT period is determined by the following equation:

(N x Pre-scale x 2^{15}) / Oscillator frequency, where: N=12 for 12 clock mode, N=6 for 6 clock mode.

WDTCR (Watchdog Timer Control register, Address: 0E1H, Write-only)

LSB

-	-	WDEN	WDCL	WDIDL	PS2	PS1	PS0

- WDEN: WDT enable bit. When set, WDT is started.
- WDCL: WDT clear bit. When set, WDT will recount. Hardware will automatically clear this bit.
- WDIDL: When set, WDT is enabled in the idle mode. When clear, WDT is disabled in the idle mode.
- PS0~PS2: Pre-scale value of Watchdog timer is shown as the bellowed table:

PS2	PS1	PS0	Pre-scale	WDT period @20MHz and 12 clocks mode
0	0	0	2	39.3 mS
0	0	1	4	78.6 mS
0	1	0	8	157.3 mS
0	1	1	16	314.6 mS
1	0	0	32	629.1 mS
1	0	1	64	1.25 S
1	1	0	128	2.5 S
1	1	1	256	5 S

Dual DPTR

There are two 16-bit DPTR registers that address the external memory. A DPS bit in the AUXR1 SRF is used to switch between DPTR0 and DPTR1.

AUXR1 (Auxiliary register 1, Address: 0A2H)

LSB

-	-	-	-	-	-	-	DPS

- When DPS=0, MPC89L556X2 selects DPTR0, and when DPS=1, then MPC89L556X2 selects DPTR1.

Reset

The RESET pin, which is the input to the schmitt trigger, is the input for chip reset. The level change of RST-pin has to keep at least two-machine cycle.

Power-Saving and EMI-Reduced Modes

MPC89L556X2 has two power-saving modes: idle mode and power-down mode. The following table shows the status of I/O ports during the idle and power-down modes. MPC89L556X2 also provides the EMI-reduced mode.

Mode	Program Memory	ALE	$\overline{\text{PSEN}}$	Port 0	Port 1	Port 2	Port 3
Idle	Internal	1	1	Data	Data	Data	Data
Idle	External	1	1	Float	Data	Address	Data
Power-Down	Internal	0	0	Data	Data	Data	Data
Power-Down	External	0	0	Float	Data	Data	Data

Idle Mode

When the IDL bit in the PCON SFR is set, MPC89L556X2 enters the idle mode. In this mode, the internal clock is frozen the micro-controller, but the peripherals, interrupt, timer, watchdog timer and serial port will continue to be worked. There are two ways to exit the idle mode. One way is to enable any interrupt, and the other way is to pull RST-pin to high.

Power-down Mode

When the PD bit in the PCON SFR is set, MPC89L556X2 enters the power-down mode. In this mode, the on-chip oscillator is stopped, and the contents of on-chip RAM and SFRs are maintained. There are two ways to wake-up MPC89L556X2 from power-down mode, RST-pin and $\overline{\text{INT0}}$ / $\overline{\text{INT1}}$ pins. When using RST-pin, there will be carefully to keep RST-pin active for at least 10ms in order for a stable clock.

This power-down mode can be woken-up by either RST-pin or $\overline{\text{INT0}}$ / $\overline{\text{INT1}}$ pins while $\overline{\text{INT0}}$ or $\overline{\text{INT1}}$ external interrupt is enabled. When MPC89L556X2 is woken-up by RST-pin, the program code will execute from the address 0000H, and if it is woken-up by $\overline{\text{INT0}}$ or $\overline{\text{INT1}}$ pin, then the program code will run the instruction which follows the instruction making MPC89L556X2 into the power-down mode. The example instructions are as follows:

```
ORL     PCON, #02H    ; Enable the power-down mode
NOP                   ; Need to add this “NOP” instruction for waking-up by INT0 or INT1 pin
```

EMI-Reduce d Mode

When set the AO bit in the AUXR SFR (Address: 08EH), MPC89L556X2 will disable the ALE output if no external access is needed.

On-Chip Flash Memory Characteristics

MPC89L556X2's on-chip flash memory is divided into two blocks, one is the main memory which contains 64k bytes user code. The other is the information memory, which consists two option registers, which are OR0 and OR1. It is used for the security and changing the operating speed.

Security And Speed Bits

MPC89L556X2's information memory has two option registers, OR0 and OR1, to determine the security and the operating speed. They are only used on the programmer. Three-level code protections are implemented in MPC89L556X2 by clearing these bits in the OR0 register. This code-protected operation is only done on the programmer. The first level is the LOCK bit. If the LOCK bit is cleared to 0, the data read-out on the programmer will always be 0FFH. The ENCRYPT bit is the second level protection. Clearing the ENCRYPT bit will encrypt the data while reading out the data on the programmer. The third level protection is MOVCL, clearing the MOVCL bit will disable the MOVC operation when the execution is from the external memory. There is another optional register (OR1) for selecting one operating speed between 12T and 6T, to select in MPC89L556X2 by clearing the EN6T bit in the OR1 register. If 6T is selected, the performance will be increased twice than the conventional 80C52 series. The default speed of MPC89L556X2 is the same as the conventional 80C52 that need 12 clocks for each machine instruction cycle.

OR0 (Option Register 0, Address: 10000H):

							LSB
ISP_SA3	ISP_SA2	ISP_SA1	ISP_SA0	HWEN_ISP	MOVCL	ENCRYPT	LOCK

Note: It locates at flash memory address, 10000H, and can be only programmed on the programmer.

- MOVCL: MOVC instructions lock bit. When it is selected (clearing to 0), MOVC instructions executed from the external program memory will be inhibited the access of the code from the internal memory. When this bit is 1, then the MOVC instruction has no any limitation
- ENCRYPT: Encryption bit. When it is selected (clearing to 0), the code dumping out from the programmer is encrypted. When this bit is 1, the encryption is disabled.
- LOCK: Lock bit. When it is selected (clearing to 0), the code reading out from the programmer is always 0FFH.
- ISP_SA0 ~ ISP_SA3: ISP space adjustment bit. These bits are used for the ISP operation only, and the details please see "In-system programming application note".
- HWEN_ISP: Hardware enable ISP bit. This bit is also used for the ISP operation only, and the details please see "In-system programming application note"

OR1 (Option Register 1, Address: 10001H):

LSB

-	-	-	-	-	EN6T	-	-

Note: It locates at flash memory address, 10001H, and can be only programmed on the programmer.

- EN6T: Enhanced 6T bit. When it is selected (clearing to 0), the speed of MPC89L556X2 will change to 6 clocks for each machine instruction cycle. When this bit is 1(default value), the operating speed maintains 12 clocks.

Absolute Maximum Ratings

PARAMETER	RATING	MIN.	MAX.	UNIT
Voltage on any pin except V_{DD}/V_{SS} and P1	Vpin	-0.5	5.5	V
Operating Temperature	T_A	0	+70	℃
Storage Temperature	T_{ST}	-40	+125	℃

Note: Exposure to conditions beyond those listed under Absolute Maximum Ratings may adversely affect the life and reliability of the device.

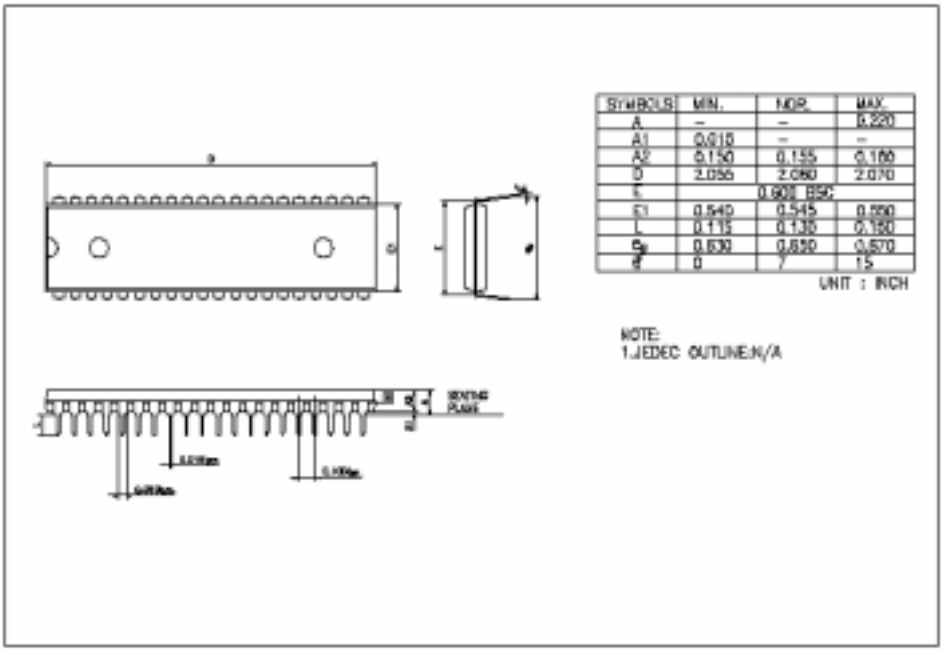
DC Characteristics

V_{SS} = 0V, TA = 25 ℃ and 12 clocks per machine cycle ,unless otherwise specified

Symbol	Parameter	Test Condition	Specification			Unit
			Min.	Typ.	Max.	
Icc	Operating Current @20MHz	Vcc=3.3V	-	-	12	mA
Iidle	Idle Mode Current @ 20MHz	Vcc=3.3V	-	-	6	mA
Ipd	Power Down Current	Vcc=3.3V	-	-	50	uA
V_{IL}	Input High Voltage (P0, P1, P2, P3, P4, - EA)	3.0V < Vcc <3.6V	0.8	-	-	V
V_{IH1}	Input High Voltage (P0, P1, P2, P3, P4, - EA)	3.0V < Vcc <3.6V	-	-	2.0	V
V_{IH2}	Input High Voltage (XTAL1, RST)	3.0V < Vcc <3.6V	-	-	2.2	V
I_{OL1}	Output Low Voltage (P1, P2, P3, P4)	Vcc=3.3V, Vpin=0.45V	-	6	-	mA
I_{OL2}	Output Low Voltage (P0, ALE, PSEN)	Vcc=3.3V, Vpin=0.45V	-	12	-	mA
I_{OH1}	Output High Voltage (P1, P2, P3, P4)	Vcc=3.3V, Vpin=2.4V	-	250	-	uA
I_{OH2}	Output High Voltage (P0, ALE, PSEN)	Vcc=3.3V, Vpin=2.4V	-	12	-	mA
I_{LK}	Input Leakage Current (P0, - EA)		-	-	10	uA
AVin	Analog input voltage		AV_{SS}-0.2	-	AV_{DD}+0.2	V
E_{ADC}	ADC conversion error		-	1	3	LSB
R_{RST}	Internal Reset Pull-down Resistance	Vcc=3.3V	-	100	-	KΩ

Package Dimensions

40-pin DIP (MPC89L556X2)

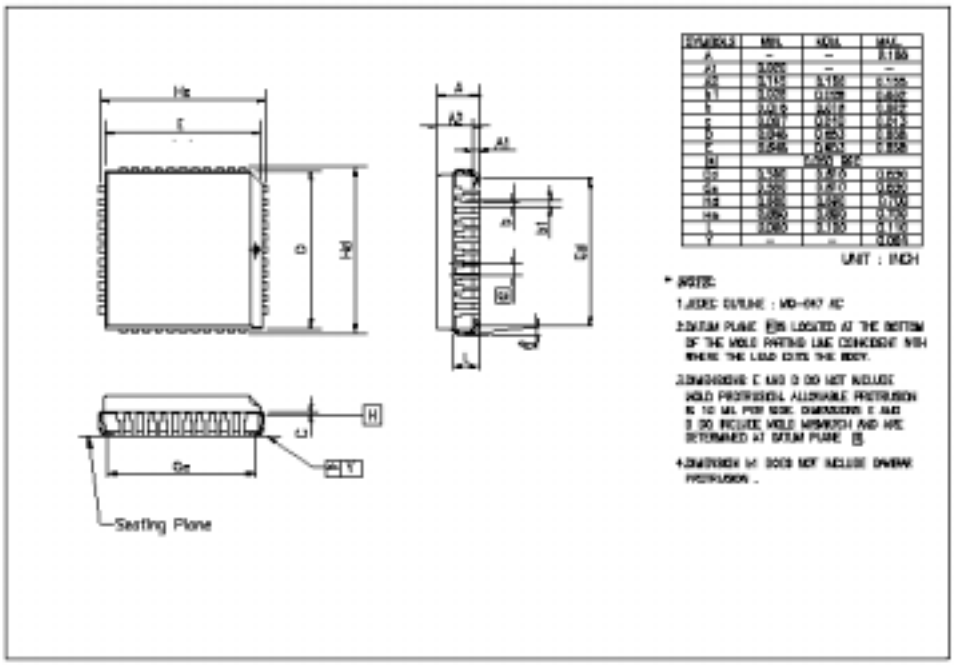


SYMBOLS	MIN.	NOR.	MAX.
A	–	–	0.220
A1	0.010	–	–
A2	0.150	0.155	0.160
D	2.055	2.060	2.070
E		0.600 BSC	
E1	0.540	0.545	0.550
L	0.115	0.120	0.130
eB	0.630	0.650	0.670
θ	0	7	15

UNIT : INCH

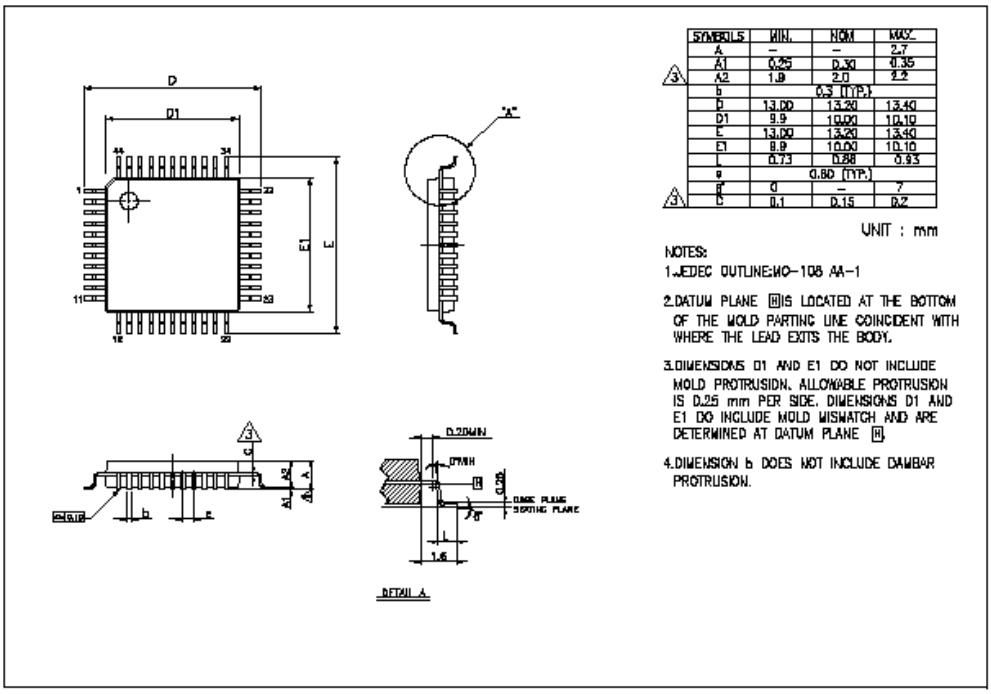
NOTE:
1.JEDEC OUTLINE:N/A

44-pin PLCC (MPC89L516X2P)



UNIT : INCH

44-pin PQFP (MPC89L516X2F)



SYMBOLS	MIN.	NOM	MAX.
A	–	–	2.7
A1	0.25	0.30	0.35
A2	1.9	2.0	2.2
b		0.3 (TYP.)	
D	13.00	13.20	13.40
D1	9.9	10.00	10.10
E	13.00	13.20	13.40
E1	9.9	10.00	10.10
L	0.73	0.88	0.93
e		0.80 (TYP.)	
θ	0	–	7
c	0.1	0.15	0.2

Version History

Version	Date	Page	Description
A1	2003/10		Initial issue