FEATURES

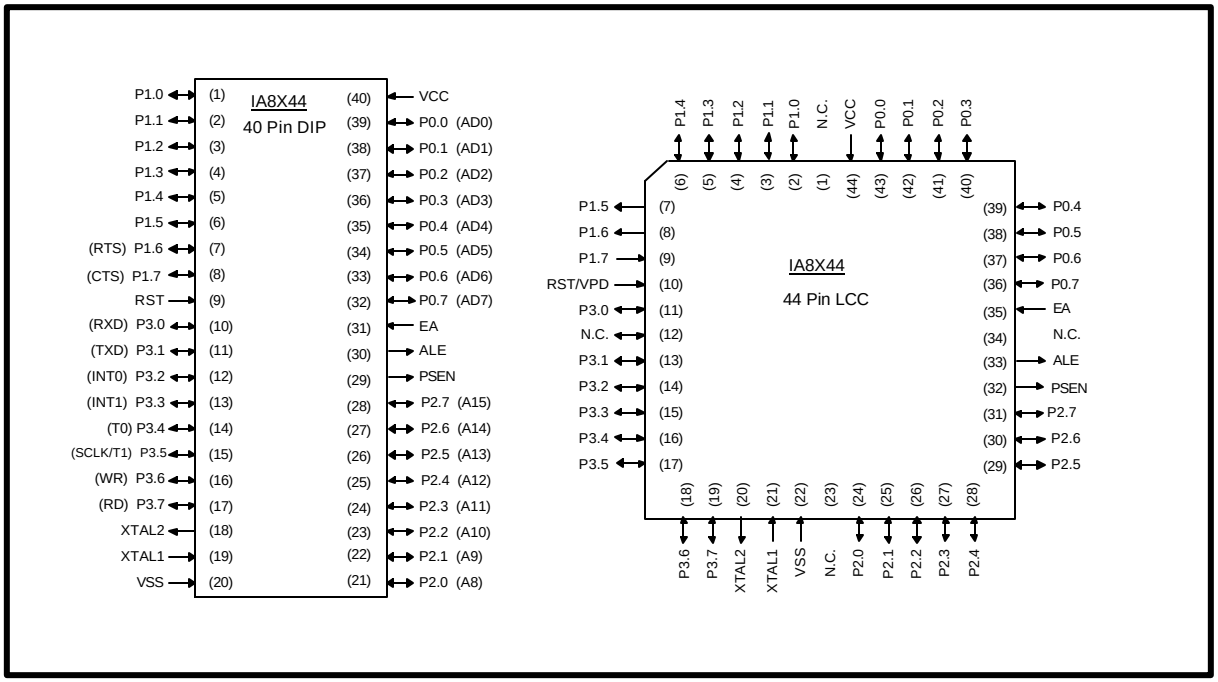
- **Form, Fit, and Function Compatible with the Intel® 8X44**
- **Packaging options available: 40 Pin Plastic Dual In-Line Package (PDIP), 44 Pin Plastic Leaded Chip Carrier (PLCC)**
- **8-Bit Control Unit**
- **8-Bit Arithmetic-Logic Unit with 16-Bit multiplication and division**
- **12 MHz clock**
- **Four 8-Bit Input / Output ports**
- **Two 16-Bit Timer/Counters**
- **Serial Interface Unit with SDLC/HDLC compatibility**
- **2.4 Mbps maximum serial data rate**
- **Two Level Priority Interrupt System**
- **5 Interrupt Sources**
- **Internal Clock prescaler and Phase generator**
- **192 Bytes of Read/Write Data Memory Space**
- **64kB External Program Memory Space**
- **64kB External Data Memory Space**
- **4kB Internal ROM (IA8044 only)**

IA8044/IA8344 Variants

IA8044	4kB internal ROM with R0117 version 2.1 firmware, 192 byte internal RAM (Expandable to 256 Bytes), 64kB external program and data space.
IA8344	192 byte internal RAM, 64kB external program and data space.

The IA8044/IA8344 is a "plug-and-play" drop-in replacement for the original IC. innovASIC produces replacement ICs using its MILES™, or Managed IC Lifetime Extension System, cloning technology. This technology produces replacement ICs far more complex than "emulation" while ensuring they are compatible with the original IC. MILES™ captures the design of a clone so it can be produced even as silicon technology advances. MILES™ also verifies the clone against the original IC so that even the "undocumented features" are duplicated. This data sheet documents all necessary engineering information about the IA8044/IA8344 including functional and I/O descriptions, electrical characteristics, and applicable timing.

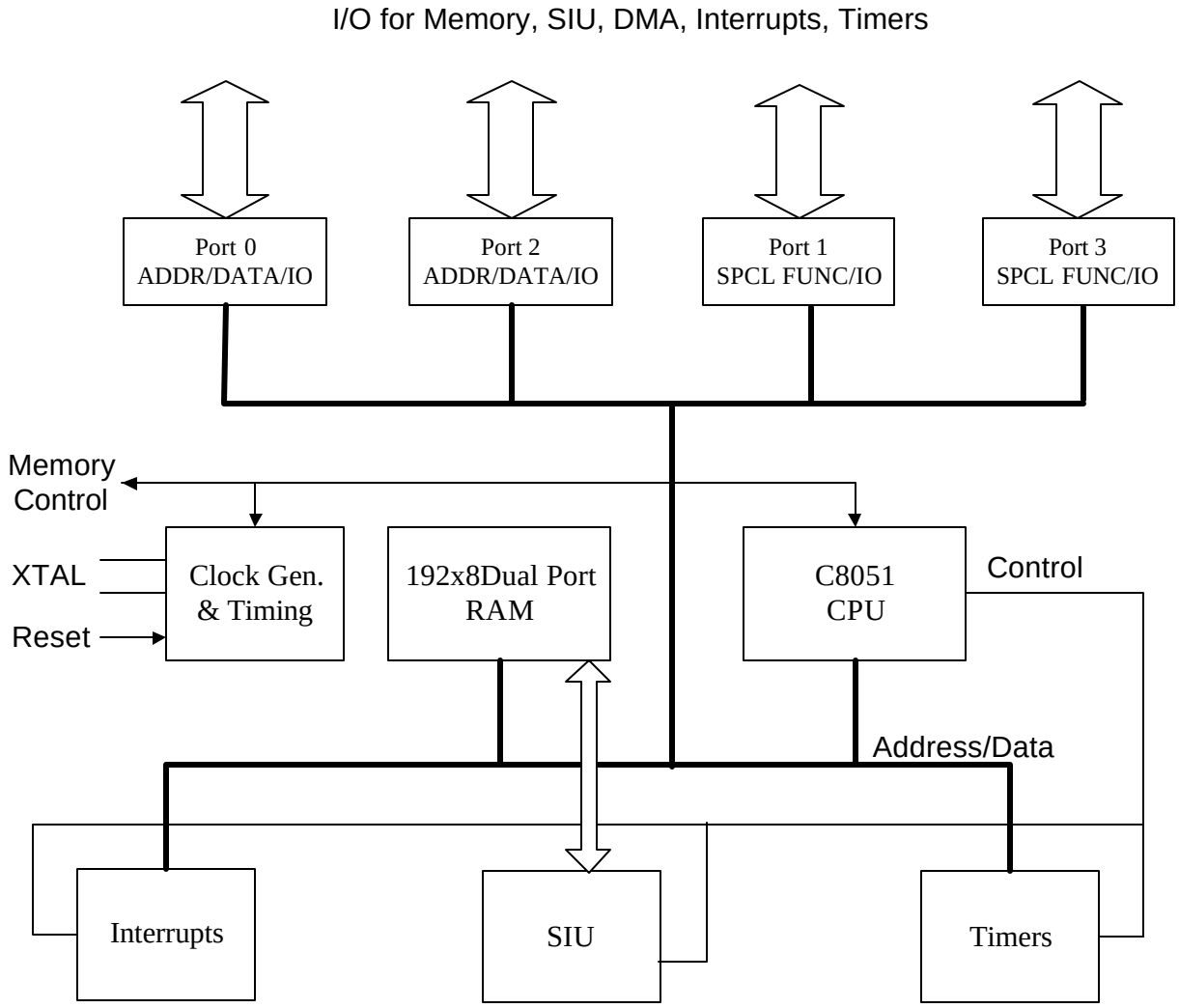
Package Pinout



DESCRIPTION

The IA8044/IA8344 is a form, fit and function compatible part to the Intel® 8X44 SDLC communications controller. The IA8044/IA8344 is a Fast Single-Chip 8-Bit Microcontroller with an integrated SDLC/HDLC serial interface controller. The IA8044/IA8344 is a fully functional 8-Bit Embedded Controller that executes all ASM51 instructions and has the same instruction set as the Intel 80C51. The IA8044/IA8344 can access the instructions from two types of program memory, serves software and hardware interrupts, provides an interface for serial communications and a timer system. The IA8044/IA8344 is fully compatible with the Intel® 8X44 series. The functional block diagram is shown below.

Functional Block Diagram



I/O Characteristics

The table below describes the I/O characteristics for each signal on the IC. The signal names correspond to the signal names on the pinout diagrams provided**.** The table below provides the I/O description of the IA8044 and the IA8344.

Name	Type	Description
RST	I	Reset. This pin when held high for two machine cycles while the oscillator is running will cause the chip to reset.
ALE	O	Address Latch Enable. Used to latch the address on the falling edge for external memory accesses.
PSEN	O	Program Store Enable. When low acts as an output enable for external program memory.
EA	I	External Access. When held low EA will cause the IA8044/IA8344 to fetch instructions from external memory.
P0.7 – P0.0	I/O	Port 0. 8 bit I/O port and low order multiplexed address/data byte for external accesses.
P1.7 – P1.0	I/O	Port 1. 8 bit I/O port. Two bits have alternate functions, P1.6 (RTS) and P1.7 (CTS).
P2.7 – P2.0	I/O	Port 2. 8 bit I/O port. It also functions as the high order address byte during external accesses.
P3.7 – P3.0	I/O	Port 3. 8 bit I/O port. Port 3 bits also have alternate functions as described below. P3.0 – RXD. Receive data input for SIU or direction control for P3.1 dependent upon datalink configuration. P3.1 – TXD. Transmit data output for SIU or data input/output dependent upon datalink configuration. Also enables diagnostic mode when cleared. P3.2 – INT0. Interrupt 0 input or gate control input for counter 0. P3.3 – INT1. Interrupt 1 input or gate control input for counter 1. P3.4 – T0. Input to counter 0. P3.5 – SCLK/T1. SCLK input to SIU or input to counter 1. P3.6 – WR. External memory write signal. P3.7 – RD. External memory read signal.
XTAL1	I	Crystal Input 1. Connect to VSS when external clock is used on XTAL2. May be connected to a crystal (with XTAL2), or may be driven directly with a clock source (XTAL2 not connected).
XTAL2	O	Crystal Input 2. May be connected to a crystal (with XTAL1), or may be driven directly with an inverted clock source (XTAL1 tied to ground).
VSS	P	Ground.
VCC	P	+5V power.

Memory Organization

Program Memory

Program Memory includes interrupt and Reset vectors. The interrupt vectors are spaced at 8-byte intervals, starting from 0003H for External Interrupt 0.

Reset Vectors

Location	Service
0003H	External Interrupt 0
000BH	Timer 0 overflow
0013H	External Interrupt 1
001BH	Timer 1 overflow
0023H	SIU Interrupt

These locations may be used for program code, if the corresponding interrupts are not used (disabled). The Program Memory space is 64K, from 0000H to FFFFH. The lowest 4K of program code (0000H to 0FFFH) can be fetched from external or internal Program Memory. This selection is made by strapping pin 'EA' (External Address) to GND or VCC. If during reset, 'EA' is held low, all the program code is fetched from external memory. If, during reset, 'EA' is held high, the lowest 4K of program code (0000H to 0FFFH) is fetched from internal memory (ROM).

Data Memory

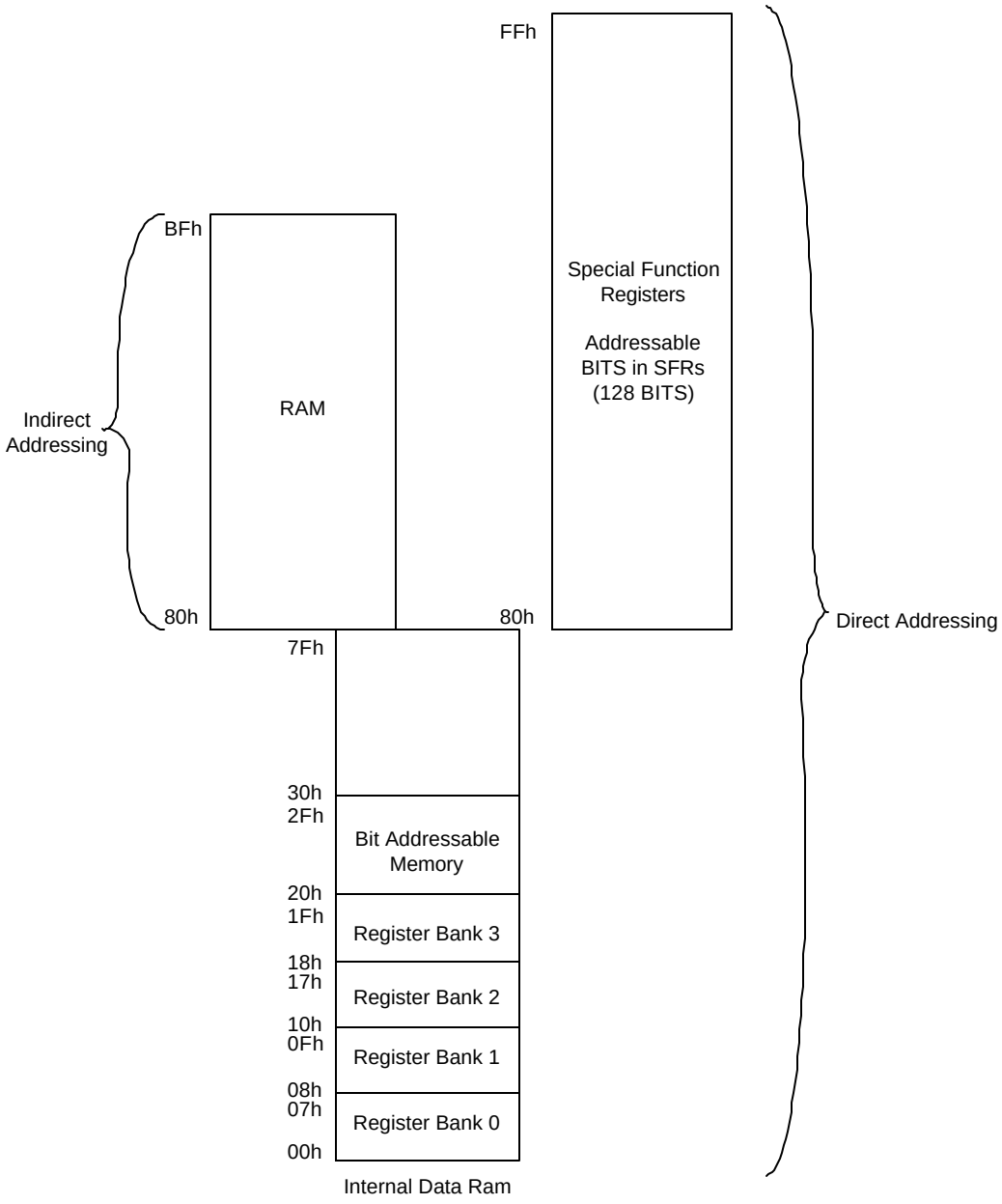
External Data Memory

The IA8044/IA8344 Microcontroller core incorporates the Harvard architecture, with separate code and data spaces. The code from external memory is fetched by 'psen' strobe, while data is read from RAM by bit 7 of P3 (read strobe) and written to RAM by bit 6 of P3 (write strobe). The External Data Memory space is active only by addressing through use of the 16 bit Data Pointer Register (DPTR). A smaller subset of external data memory (8 bit addressing) may be accessed by using the MOVX instruction with register indexed addressing.

Internal Data Memory

The Internal Data Memory address is always 1 byte wide. The memory space is 192 bytes large (00H to BFH), and can be accessed by either direct or indirect addressing. The Special Function Registers occupy the upper 128 bytes. This SFR area is available only by direct addressing. Internal memory which overlaps the SFR address space is only accessible by indirect addressing.

Internal Memory



8044 Internal Data Memory Addresses
00h to FFh

Bit Addressable Memory

Both the internal RAM and the Special Function Registers have locations that are bit addressable in addition to the byte addressable locations.

SFR Bit Addressable Locations

Byte Address	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	Register
F0h	F7h	F6h	F5h	F4h	F3h	F2h	F1h	F0h	B
E0h	E7h	E6h	E5h	E4h	E3h	E2h	E1h	E0h	ACC
D8h	DFh	DEh	DDh	DCh	DBh	DAh	D9h	D8h	NSNR
D0h	D7h	D6h	D5h	D4h	D3h	D2h	D1h	D0h	PSW
C8h	CFh	CEh	CDh	CCh	CBh	CAh	C9h	C8h	STS
B8h	BFh	BEh	BDh	BCh	BBh	BAh	B9h	B8h	IP
B0h	B7h	B6h	B5h	B4h	B3h	B2h	B1h	B0h	P3
A8h	AFh	AEh	ADh	ACh	ABh	AAh	A9h	A8h	IE
A0h	A7h	A6h	A5h	A4h	A3h	A2h	A1h	A0h	P2
90h	97h	96h	95h	94h	93h	92h	91h	90h	P1
88h	8Fh	8Eh	8Dh	8Ch	8Bh	8Ah	89h	88h	TCON
80h	87h	86h	85h	84h	83h	82h	81h	80h	P0

Internal RAM Bit Addressable Locations

Byte Address	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
30h-BFh	Upper Internal Ram locations							
2Fh	7Fh	7Eh	7Dh	7Ch	7Bh	7Ah	79h	78h
2Eh	77h	76h	75h	74h	73h	72h	71h	70h
2Dh	6Fh	6Eh	6Dh	6Ch	6Bh	6Ah	69h	68h
2Ch	67h	66h	65h	64h	63h	62h	61h	60h
2Bh	5Fh	5Eh	5Dh	5Ch	5Bh	5Ah	59h	58h
2Ah	57h	56h	55h	54h	53h	52h	51h	50h
29h	4Fh	4Eh	4Dh	4Ch	4Bh	4Ah	49h	48h
28h	47h	46h	45h	44h	43h	42h	41h	40h
27h	3Fh	3Eh	3Dh	3Ch	3Bh	3Ah	39h	38h
26h	37h	36h	35h	34h	33h	32h	31h	30h
25h	2Fh	2Eh	2Dh	2Ch	2Bh	2Ah	29h	28h
24h	27h	26h	25h	24h	23h	22h	21h	20h
23h	1Fh	1Eh	1Dh	1Ch	1Bh	1Ah	19h	18h
22h	17h	16h	15h	14h	13h	12h	11h	10h
21h	0Fh	0Eh	0Dh	0Ch	0Bh	0Ah	09h	08h
20h	07h	06h	05h	04h	03h	02h	01h	00h
18h-1Fh	Register Bank 3							
10h-17h	Register Bank 2							
08h-0Fh	Register Bank 1							
00h-07h	Register Bank 0							

Instruction Set

The 8X44 architecture and instruction set are identical to the 8051's. The following tables give a survey of the instruction set of the IA8044/IA8344 Microcontroller core.

Arithmetic Operations

Mnemonic	Description	Byte	Cycle
ADD A,Rn	Add register to accumulator	1	1
ADD A, direct	Add direct byte to accumulator	2	1
ADD A,@Ri	Add indirect RAM to accumulator	1	1
ADD A,#data	Add immediate data to accumulator	2	1
ADDC A,Rn	Add register to accumulator with carry flag	1	1
ADDC A,direct	Add direct byte to A with carry flag	2	1
ADDC A,@Ri	Add indirect RAM to A with carry flag	1	1
ADDC A,#data	Add immediate data to A with carry flag	2	1
SUBB A,Rn	Subtract register from A with borrow	1	1
SUBB A,direct	Subtract direct byte from A with borrow	2	1
SUBB A,@Ri	Subtract indirect RAM from A with borrow	1	1
SUBB A,#data	Subtract immediate data from A with borrow	2	1
INC A	Increment accumulator	1	1
INC Rn	Increment register	1	1
INC direct	Increment direct byte	2	1
INC @ Ri	Increment indirect RAM	1	1
DEC A	Decrement accumulator	1	1
DEC Rn	Decrement register	1	1
DEC direct	Decrement direct byte	2	1
DEC @Ri	Decrement indirect RAM	1	1
INC DPTR	Increment data pointer	1	2
MUL A,B	Multiply A and B	1	4
DIV A,B	Divide A by B	1	4
DA A	Decimal adjust accumulator	1	1

Logic Operations

Mnemonic	Description	Byte	Cycle
ANL A,Rn	AND register to accumulator	1	1
ANL A,direct	AND direct byte to accumulator	2	1
ANL A,@Ri	AND indirect RAM to accumulator	1	1
ANL A,#data	AND immediate data to accumulator	2	1
ANL direct,A	AND accumulator to direct byte	2	1
ANL direct,#data	AND immediate data to direct byte	3	2
ORL A,Rn	OR register to accumulator	1	1
ORL A,direct	OR direct byte to accumulator	2	1
ORL A,@Ri	OR indirect RAM to accumulator	1	1
ORL A,#data	OR immediate data to accumulator	2	1
ORL direct,A	OR accumulator to direct byte	2	1
ORL direct,#data	OR immediate data to direct byte	3	2
XRL A,Rn	Exclusive OR register to accumulator	1	1
XRL A,direct	Exclusive OR direct byte to accumulator	2	1
XRL A,@Ri	Exclusive OR indirect RAM to accumulator	1	1
XRL A,#data	Exclusive OR immediate data to accumulator	2	1
XRL direct,A	Exclusive OR accumulator to direct byte	2	1
XRL direct,#data	Exclusive OR immediate data to direct byte	3	2
CLR A	Clear accumulator	1	1
CPL A	Complement accumulator	1	1
RL A	Rotate accumulator left	1	1
RLC A	Rotate accumulator left through carry	1	1
RR A	Rotate accumulator right	1	1
RRC A	Rotate accumulator right through carry	1	1
SWAP A	Swap nibbles within the accumulator	1	1

Data Transfer

Mnemonic	Description	Byte	Cycle
MOV A,Rn	Move register to accumulator	1	1
MOV A,direct	Move direct byte to accumulator	2	1
MOV A,@Ri	Move indirect RAM to accumulator	1	1
MOV A,#data	Move immediate data to accumulator	2	1
MOV Rn,A	Move accumulator to register	1	1
MOV Rn,direct	Move direct byte to register	2	2
MOV Rn,#data	Move immediate data to register	2	1
MOV direct,A	Move accumulator to direct byte	2	1
MOV direct,Rn	Move register to direct byte	2	2
MOV direct,direct	Move direct byte to direct byte	3	2
MOV direct,@Ri	Move indirect RAM to direct byte	2	2
MOV direct,#data	Move immediate data to direct byte	3	2
MOV @Ri,A	Move accumulator to indirect RAM	1	1
MOV @Ri,direct	Move direct byte to indirect RAM	2	2
MOV @ Ri, #data	Move immediate data to indirect RAM	2	1
MOV DPTR, #data16	Load data pointer with a 16-bit constant	3	2
MOVC A,@A + DPTR	Move code byte relative to DPTR to accumulator	1	2
MOVC A,@A + PC	Move code byte relative to PC to accumulator	1	2
MOVX A,@Ri	Move external RAM (8-bit addr.) to A	1	2
MOVX A,@DPTR	Move external RAM (16-bit addr.) to A	1	2
MOVX @Ri,A	Move A to external RAM (8-bit addr.)	1	2
MOVX @DPTR,A	Move A to external RAM (16-bit addr.)	1	2
PUSH direct	Push direct byte onto stack	2	2
POP direct	Pop direct byte from stack	2	2
XCH A,Rn	Exchange register with accumulator	1	1
XCH A,direct	Exchange direct byte with accumulator	2	1
XCH A,@Ri	Exchange indirect RAM with accumulator	1	1
XCHD X,@ Ri	Exchange low-order nibble indir. RAM with A	1	1

Boolean Manipulation

Mnemonic	Description	Byte	Cycle
CLR C	Clear carry flag	1	1
CLR bit	Clear direct bit	2	1
SETB C	Set carry flag	1	1
SETB bit	Set direct bit	2	1
CPL C	Complement carry flag	1	1
CPL bit	Complement direct bit	2	1
ANL C,bit	AND direct bit to carry flag	2	2
ANL C,bit	AND complement of direct bit to carry	2	2
ORL C,bit	OR direct bit to carry flag	2	2
ORL C,bit	OR complement of direct bit to carry	2	2
MOV C,bit	Move direct bit to carry flag	2	1
MOV bit,C	Move carry flag to direct bit	2	2

Program Branches

Mnemonic	Description	Byte	Cycle
ACALL addr11	Absolute subroutine call	2	2
LCALL addr16	Long subroutine call	3	2
RET Return	from subroutine	1	2
RETI Return	from interrupt	1	2
AJMP addr11	Absolute jump	2	2
LJMP addr16	Long jump	3	2
SJMP rel	Short jump (relative addr.)	2	2
JMP @A + DPTR	Jump indirect relative to the DPTR	1	2
JZ rel	Jump if accumulator is zero	2	2
JNZ rel	Jump if accumulator is not zero	2	2
JC rel	Jump if carry flag is set	2	2
JNC rel	Jump if carry flag is not set	2	2
JB bit,rel	Jump if direct bit is set	3	2
JNB bit,rel	Jump if direct bit is not set	3	2
JBC bit,rel	Jump if direct bit is set and clear bit	3	2
CJNE A,direct,rel	Compare direct byte to A and jump if not equal	3	2
CJNE A,#data,rel	Compare immediate to A and jump if not equal	3	2
CJNE Rn,#data rel	Compare immed. to reg. and jump if not equal	3	2
CJNE @Ri,#data,rel	Compare immed. to ind. and jump if not equal	3	2
DJNZ Rn,rel	Decrement register and jump if not zero	2	2
DJNZ direct,rel	Decrement direct byte and jump if not zero	3	2
NOP	No operation	1	1

Special Function Registers

The IA8044/IA8344 contains the following special function registers:

ACC	Accumulator
B	B register *
PSW	program Status Word *
SP	Stack Pointer
DPTR	Data Pointer (DPH and DPL)
P0	Port 0 *
P1	Port 1 *
P2	Port 2 *
P3	Port 3 *
IP	Interrupt Priority *
IE	Interrupt Enable *
TMOD	Timer/Counter Mode
TCON	Timer/Counter Control *
TH0	Timer/Counter 0 high byte
TL0	Timer/Counter 0 low byte
TH1	Timer/Counter 1 high byte
TL1	Timer/Counter 1 low byte
SMD	Serial Mode
STS	SIU Status and Command *
NSNR	SIU Send/Receive Count *
STAD	SIU Station Address
TBS	Transmit Buffer Start Address
TBL	Transmit Buffer Length
TCB	Transmit Control Byte
RBS	Receive Buffer Start Address
RBL	Receive Buffer Length
RFL	Receive Field Length
RCB	Receive Control Byte
DMA CNT	DMA Count
FIFO	FIFO contents (3 bytes)
SIUST	SIU State Counter

* - These registers are bit addressable.

Ports

Ports P0, P1, P2 and P3 are Special Function Registers. The contents of the SFR can be observed on corresponding pins on the chip. Writing a '1' to any of the ports causes the corresponding pin to be at high level (VCC), and writing a '0' causes the corresponding pin to be held at low level (GND).

All four ports on the chip are bi-directional. Each of them consists of a Latch (SFR P0 to P3), an output driver, and an input buffer, so the CPU can output or read data through any

of these ports if they are not used for alternate purposes.

Ports P0, P1, P2 and P3 can perform some alternate functions. Ports P0 and P2 are used to access external memory. In this case, port 'p0' outputs the multiplexed lower 8 bits of address with 'ale' strobe high and then reads/writes 8 bits of data. Port P2 outputs the higher 8 bits of address. Keeping 'ea' pin low (tied to GND) activates this alternate function for ports P0 and P2.

Port P3 and P1 can perform some alternate functions. The pins of Port P3 are multifunctional. They can perform additional functions as shown below.

Pin	Symbol	Function
P3.0	RxD	Serial input pin. Setting the appropriate bits in the Special Function Register SCON activates this function. Serial input data at pin P3.0 is strobed to the serial input register and can then be read by the CPU from the Special Function Register SBUF.
P3.1	TxD	Serial output pin. Setting the appropriate bits in the Special Function Register SCON and writing data to be transmitted to the Special Function Register SBUF activates this function. Note that SBUF is used to read and transmit data. The function it performs is determined by the CPU operation (read or write).
P3.2	INT0	External interrupt 0 is activated on the falling edge by setting the appropriate bits in Special Function Register IE (Interrupt Enable)
P3.3	INT1	External interrupt 1 is activated on the falling edge by setting the appropriate bits in the Special Function Register IE (Interrupt Enable)
P3.4	T0	Timer/Counter 0 external input. Setting the appropriate bits in the Special Function Registers TCON and TMOD activates this function.
P3.5	T1	Timer/Counter 1 external input. Setting the appropriate bits in the Special Function Registers TCON and TMOD activates this function.
P3.6	WR	External Data Memory write strobe, active LOW. This function is activated by a CPU write access to External Data Memory (MOV @DPTR, A).
P3.7	RD	External Data Memory read strobe, active LOW. This function is activated by a CPU read access to External Data Memory (MOV A, @DPTR).
P1.6	RTS	Request To Send output.
P1.7	CTS	Clear To Send input.

Timers / Counters

Timers 0 and 1

The C8051 has two 16-bit timer / counter registers: Timer 0 and Timer 1. Both can be configured for counter or timer operations. In timer mode, the register is incremented every machine cycle, which means that it counts up after every 12 oscillator periods. In counter mode, the register is incremented when the falling edge is observed at the corresponding input pin T0 or T1. Since it takes 2 machine cycles to recognize a 1-to-0 event, the maximum input count rate is 1 / 24 of the oscillator frequency. There are no restrictions on the duty cycle, however to ensure proper recognition of 0 or 1 state, an input should be stable for at least 1 machine cycle (12 clock periods).

Four operating modes can be selected for Timer 0 and Timer 1. Two Special Function Registers (TMOD and TCON) are used to select the appropriate mode.

Reset

A reset is accomplished by holding the RST pin high for at least two machine cycles (24 oscillator periods) while the oscillator is running. The CPU responds by generating an internal reset, which is executed during the second cycle in which RST is high.

The internal reset sequence writes '0's to all SFRs except the port-latches, the Stack Pointer, SIUST and unused bits of registers.

Reset Values

Register	Reset value
PC	0000H
ACC	00000000B
B	00000000B
PSW	00000000B
SP	00000111B
DPTR	0000H
P0 – P3	11111111B
IP	XXX00000B
IE	0XX00000B
TMOD	00000000B
TCON	00000000B
TH0	00000000B
TL0	00000000B
TH1	00000000B
TL1	00000000B
SMD	00000000B
STS	00000000B
NSNR	00000000B
STAD	00000000B
TBS	00000000B
TBL	00000000B
TCB	00000000B
RBS	00000000B
RBL	00000000B
RFL	00000000B
RCB	00000000B
DMA CNT	00000000B
FIFO1	00000000B
FIFO2	00000000B
FIFO3	00000000B
SIUST	00000001B

Interrupts

The IA8044/IA8344 provides 5 interrupt sources. There are 2 external interrupts accessible through pins INT0 and INT1, edge or level sensitive (falling edge or low level). There are, also, internal interrupts associated with Timer 0 and Timer 1, and an internal interrupt from the SIU.

External Interrupts

The choice between external interrupt level or transition activity is made by setting IT1 and IT0 bits in the Special Function Register TCON.
When the interrupt event happens, a corresponding Interrupt Control Bit is set (IT0 or IT1). This control bit triggers an interrupt if the appropriate interrupt bit is enabled.
When the interrupt service routine is vectored, the corresponding control bit (IT0 or IT1) is cleared provided that the edge triggered mode was selected. If level mode is active, the external requesting source controls flags IT0 or IT1 by the logic level on pins INT0 or INT1 (0 or 1).

Timer0 and Timer 1 Interrupts

Timer 0 and 1 interrupts are generated by TF0 and TF1 flags, which are set by the rollover of Timer 0 and 1, respectively. When an interrupt is generated, the flag that caused this interrupt is cleared by the hardware, if the CPU accessed the corresponding interrupt service vector. This can be done only if this interrupt is enabled in the IE register.

Serial Interface Unit Interrupt

The SIU generates an interrupt when a frame is received or transmitted. No interrupts are generated for a received frame with errors.

Interrupt Priority Level Structure

There are two priority levels in the IA8044/IA8344, and any interrupt can be individually programmed to a high or low priority level. Modifying the appropriate bits in the Special Function Register IP can accomplish this. A low priority interrupt service routine will be interrupted by a high priority interrupt. However, the high priority interrupt can not be interrupted.

If two interrupts of the same priority level occur, an internal polling sequence determines which of them will be processed first. This polling sequence is a second priority structure defined as follows:

IE0 1 – highest
TF0 2
IE1 3
TF1 4
SIU – lowest

Interrupt Handling

The interrupt flags are sampled during each machine cycle. The samples are polled during the next machine cycle. If an interrupt flag is captured, the interrupt system will generate an LCALL instruction to the appropriate service routine, provided that this is not disabled by the following conditions:

1. An interrupt of the same or higher priority is processed
2. The current machine cycle is not the last cycle of the instruction (the instruction can not be interrupted).
3. The instruction in progress is RETI or any write to IE or IP registers.

Note that if an interrupt is disabled and the interrupt flag is cleared before the blocking condition is removed, no interrupt will be generated, since the polling cycle will not sample any active interrupt condition. In other words, the interrupt condition is not remembered. Every polling cycle is new.

SIU – Serial Interface Unit

The SIU is a serial interface customized to support SDLC/HDLC protocol. As such it supports Zero Bit insertion/deletion, Flags automatic access recognition and a 16 bit CRC. The SIU has two modes of operation AUTO and FLEXIBLE. The AUTO mode uses a subset of the SDLC protocol implemented in hardware. This frees the CPU from having to respond to every frame but limits the frame types. In the FLEXIBLE mode every frame is under CPU control and therefore more options are available. The SIU is controlled by and communicates to the CPU by using several special function registers (SFRs). Data transmitted to or received by the SIU is stored in the 192 byte internal RAM in blocks referred to as the transmit and receive buffers. The SIU can support operation in one of three serial data link configurations: 1) half-duplex, point-to-point, 2) half-duplex, multipoint, 3) loop.

SIU Special Function Registers

The CPU controls the SIU and receives status from the SIU via eleven special function registers. The Serial Interface Unit Control Registers are detailed below:

Serial Mode Register (SMD):

The serial mode register sets the operational mode of the SIU. The CPU can read and write SMD. The SIU can read SMD. To prevent conflicts between CPU and SIU accesses to SMD the CPU should write SMD only when RTS and RBE bits in the STS register are both zero. SMD is normally only accessed during initialization. This register is byte addressable.

SMD (C9H)

Bit:	7	6	5	4	3	2	1	0
	SCM2	SCM1	SCM0	NRZI	LOOP	PFS	NB	NFCS

SMD.0	NFCS	When set selects No FCS field contained in the SDLC frame.
SMD.1	NB	Non-buffered mode. No control field contained in SDLC frame.
SMD.2	PFS	Pre-frame sync mode. When set causes two bytes to be transmitted before the first flag of the frame for DPLL synchronization. If NRZI is set 00H is transmitted otherwise 55H. This ensures that 16 transitions are sent.
SMD.3	LOOP	When set selects loop configuration.
SMD.4	NRZI	When set selects NRZI encoding otherwise NRZ.
SMD.5	SCM0	Select clock mode - bit 0.
SMD.6	SCM1	Select clock mode - bit 1.
SMD.7	SCM2	Select clock mode - bit 2.

SMD Select Clock Mode Bits

SCM 2 1 0	Clock Mode	Data Rate (Bits/sec)*
0 0 0	Externally clocked	0 – 2.4M**
0 0 1	Undefined	
0 1 0	Self clocked, timer overflow	244 – 62.5K
0 1 1	Undefined	
1 0 0	Self clocked, external 16X	0 – 375K
1 0 1	Self clocked, external 32X	0 – 187.5K
1 1 0	Self clocked, internal fixed	375K
1 1 1	Self clocked, internal fixed	187.5K

* based on a12 MHz crystal frequency

** 0 – 1M bps in loop configuration

Status/Command Register (STS):

The Status/Command register provides SIU control from and status to the CPU. The SIU can read the STS and can write certain bits in the STS. The CPU can read and write the STS. Accessing the STS by the CPU via 2 cycle instructions (JBC bit,rel and MOV bit,C) should not be used. STS is bit addressable.

STS (C8H)

Bit:	7	6	5	4	3	2	1	0
	TBF	RBE	RTS	SI	BOV	OPB	AM	RBP

STS.0	RBP	Receive buffer protect. When set prevents writing of data into the receive buffer. Causes RNR response instead of RR in AUTO mode.
STS.1	AM	Auto mode. If NB is cleared AM selects the AUTO mode when set. If NB is set AM selects the addressed mode when set. The SIU can clear AM.
STS.2	OPB	Optional poll bit. When set the SIU will AUTO respond to an optional poll (UP with P=0). The SIU can set or clear the OPB.
STS.3	BOV	Receive buffer overrun. The SIU can set or clear BOV.
STS.4	SI	SIU interrupt. This bit is set by the SIU and should be cleared by the CPU before returning from the interrupt routine.
STS.5	RTS	Request to send. This bit is set when the SIU is ready to transmit or is transmitting. May be written by the SIU in AUTO mode.
STS.6	RBE	Receive buffer empty. RBE is set by the CPU when it is ready to receive a frame or has just read the buffer. It is cleared by the SIU when a frame has been received.
STS.7	TBF	Transmit buffer full. TBF is set by the CPU to indicate that the transmit buffer is ready and cleared by the SIU.

Send/Receive count register (NSNR):

The NSNR contains both the transmit and receive sequence numbers in addition to the tally error indications. The CPU can read and write the STS. Accessing the STS by the CPU via 2 cycle instructions (JBC bit,rel and MOV bit,C) should not be used. The SIU can read and write the NSNR. NSNR is bit addressable.

NSNR (D8H)

Bit:	7	6	5	4	3	2	1	0
	NS2	NS1	NS0	SES	NR2	NR1	NR0	SER

NSNR.0	SER	Sequence error receive. NS (P) ? NR (S).
NSNR.1	NR0	Receive sequence counter, Bit 0.
NSNR.2	NR1	Receive sequence counter, Bit 1.
NSNR.3	NR2	Receive sequence counter, Bit 2.
NSNR.4	SES	Sequence error send. NR (P) ? NS (S) and NR (P) ? NS (S) + 1.
NSNR.5	NS0	Send sequence counter, Bit 0.
NSNR.6	NS1	Send sequence counter, Bit 1.
NSNR.7	NS2	Send sequence counter, Bit 2.

Data Clocking Options

The SIU may be clocked in one of two ways, with an external clock or in a self-clocked mode.

In the external clocked mode a serial clock must be provided on SCLK. This clock must be synchronized to the serial data. Incoming data is sampled at the rising edge of SCLK. Outgoing data is shifted out at the falling edge of SCLK.

In the self-clocked mode the SIU uses a reference clock and the serial data to reproduce the serial data clock. The reference clock can be an external source applied to SCLK, the IA8044/IA8344's internal clock or the timer 1 overflow. The reference clock must be 16x or 32x the data rate. A DPLL uses the reference clock and the serial data to adjust the sample time to the center of the serial bit. It does this by adjusting from a serial data transition in increments of 1/16 of a bit time.

The maximum data rate in the externally clocked mode is 2.4Mbps in half-duplex configuration and 1.0Mbps in a loop configuration. The maximum data rate in the self-clocked mode with an external clock is 375Kbps. The maximum data rate in the self-clocked mode with an internal clock will depend on the frequency of the IA8044/IA8344's input clock. An IA8044/IA8344 using a 12MHz input clock can operate at a maximum data rate of 375Kbps.

Operational Modes

The SIU operates in one of two modes, AUTO or FLEXIBLE. The mode selected determines how much intervention is required by the CPU when receiving frames. In both modes short frames, aborted frames, and frames with CRC errors will be ignored.

AUTO mode allows the SIU to recognize and respond to specific SDLC frames without the CPUs intervention. This provides for a faster turnaround time but restricts the operation of the SIU. When in AUTO mode the SIU can only act as a normal response secondary station and responses will adhere to IBM's SDLC definitions.

When receiving in the AUTO mode the SIU receives the frame and examines the control byte. It will then take the appropriate action for that frame. If the frame is an information frame the SIU will load the receive buffer, interrupt the CPU and make the required response to the primary station. The SIU in AUTO mode can also respond to the following commands from the primary station.

RR (Receive ready),
RNR (Receive Not Ready),
REJ (Reject),
UP (Unnumbered Poll) also called NSP (Non-Sequenced Poll) or ORP (Optional Response Poll).

In AUTO mode when the transmit buffer is full the SIU can transmit an information frame when polled for information. After transmission the SIU waits for acknowledgement from the receiving station. If the response is positive the SIU interrupts the CPU. If the response is negative the SIU retransmits the frame. The SIU can send the following responses to the primary station.

RR (Receive Ready),
RNR (Receive Not Ready).

The FLEXIBLE mode requires the CPU to control the SIU for both transmitting and receiving. This slows response time but allows full SDLC and HDLC compatibility as well as variations. In FLEXIBLE mode the SIU can act as a primary station. The SIU will interrupt the CPU after completion of a transmission without waiting for a positive acknowledgement from the receiving station.

Frame Format Options

The various frame formats available with the IA8044/IA8344 are the standard SDLC format, the no control field format, the no control field and no address field format and the no FCS field format.

The standard SDLC format consists of an opening flag, an 8-bit address field, an 8-bit control field, and n-byte information field, a 16-bit frame check sequence field and a closing flag. The FCS is generated by the CCIT-CRC polynomial (X16 +X12 + X5 + 1). The address and control fields may not be extended. The address is contained in STAD and the control filed is contained in either RCB or TCB. This format is supported by both AUTO and FLEXIBLE modes.

The no control field format is only supported by the FLEXIBLE mode. In this format TCB and RCB are not used and the information field starts immediately after the address field.

The no control field and no address field format is only supported by the FLEXIBLE mode. In this format STAD, TCB and RCB are not used and the information field starts immediately after the opening flag. This option can only be used with the no control field option.

The no FCS field format prevents an FCS from being generated during transmission or being checked during reception. This option may be used in conjunction with the other frame format options. This option will work with both FLEXIBLE and AUTO modes. In AUTO mode it could cause protocol violations.

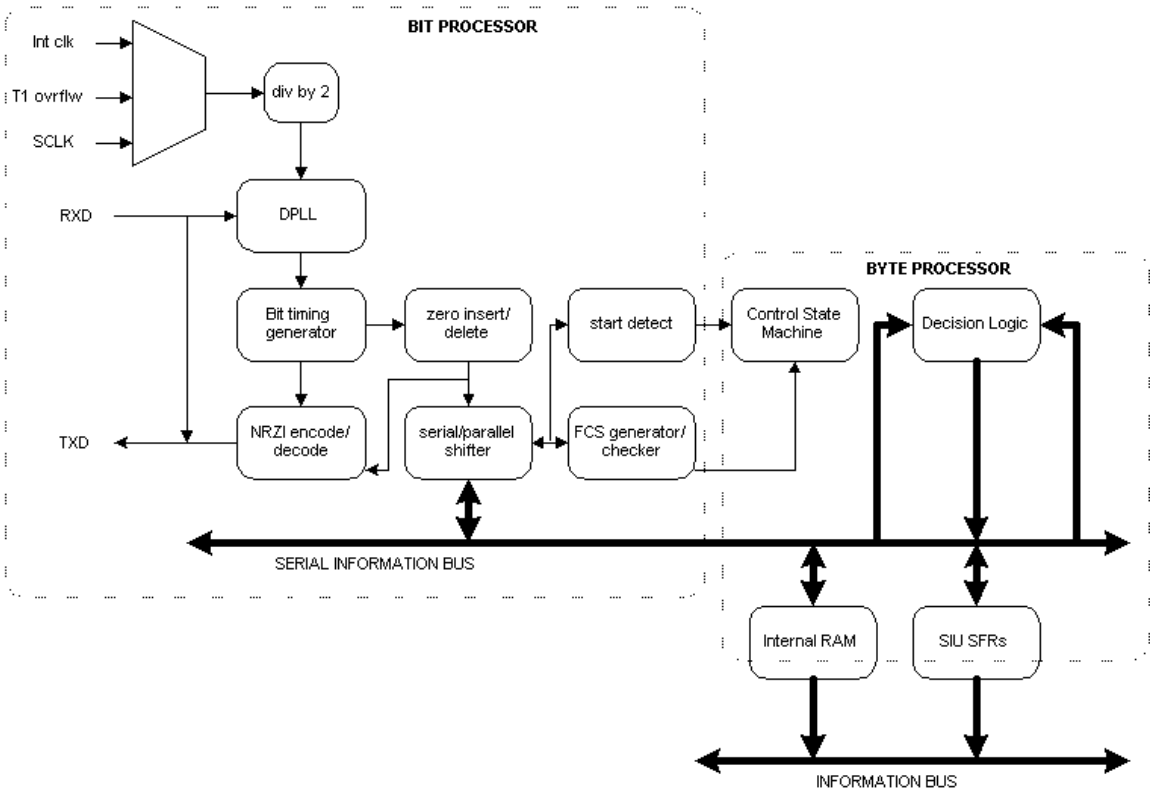
HDLC Restrictions

The IA8044/IA8344 supports a subset of the HDLC protocol. The differences include the restriction by the IA8044/IA8344 of the serial data to be in 8-bit increments. In contrast HDLC allows for any number of bits in the information field. HDLC provides an unlimited address field and an extended frame number sequencing. HDLC does not support loop configuration.

SIU Details

The SIU is composed of two functional blocks with each having several sub blocks. The two blocks are called the bit processor (BIP) and the byte processor (BYP).

Bit and Byte Processors



BIP

The BIP consists of the DPLL, NRZI encoder/decoder, serial/parallel shifter, zero insertion/deletion, shutoff logic and FCS generation/checking. The NRZI logic compares the current bit to the previous bit to determine if the bit should be inverted. The serial shifter converts the outgoing byte data to bit data and incoming bit data to byte data. The zero insert/delete circuitry inserts and deletes zeros and also detects flags, go-aheads (GA) and aborts. The pattern 1111110 is detected as an early go-ahead that can be turned into a flag in loop configurations. The shutoff detector is a three bit counter that is used to detect a sequence of eight zeros, which is the shutoff command in loop mode transmissions. It is cleared whenever a one is detected. The FCS logic performs the generation and checking of the FCS value according to the polynomial described above. The FCS register is set to all 1's prior to each calculation. If a CRC error is generated on a receive frame the SIU will not interrupt the CPU and the error will be cleared upon receiving an opening flag.

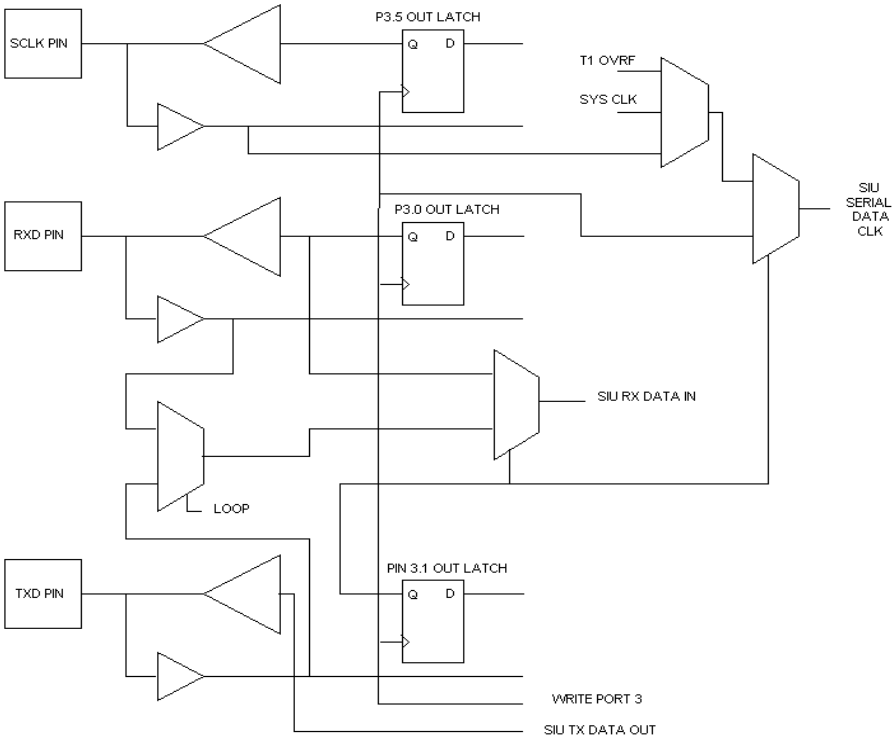
BYP

The BYP contains registers and controllers used to perform the manipulations required for SDLC communications. The BYP registers may be accessed by the CPU (see SFR section above). The BYP contains the SIU state machine which controls transmission and reception of frames.

Diagnostics

A diagnostic mode is included with the IA8044/IA8344 to allow testing of the SIU. Diagnostics use port pins P3.0 and P3.1. Writing a 0 to P3.1 enables the diagnostic mode. When P3.1 is cleared writing data to P3.0 has the effect of writing a serial data stream to the SIU. P3.0 is the serial data and any write to port 3 will clock SCLK. The transmit data may be monitored on P3.1 with any write to port 3 again clocking SCLK. In the test mode P3.0 and P3.1 pins are placed in the high impedance state.

Diagnostic Signal Routing



AC/DC Parameters

Absolute Maximum Ratings:

Ambient temperature under bias.....-40°C to +85°C
Storage temperature.....- 40°C to 150°C
Power Supply (V_{DD}).....-0.3 to +6VDC
Voltage on any pin to VSS.....-0.3 to (V_{DD} +0.3)
Power dissipation.....See Note 1

DC Characteristics

Symbol	Parameter	Min	Typ	Max	Unit
VIL	Input Low Voltage	-	-	0.8	V
VIH	Input High Voltage	2.0	-	-	V
VOL	Output Low Voltage (IOL= 4mA)	-	-	0.4	V
VOH	Output High Voltage (IOH= 4mA)	3.5	-	-	V
RPU	Pull-Up Resistance (Ports 1,2,3)	-	50	-	KΩ
RPD	Pull-Down Resistance (RST)	-	50	-	KΩ
IIL	Input Low Current (Ports 1, 2, 3)	-100		1	µA
IIL1	Input Low Current (all other inputs)	-1		1	mA
IIH	Input High Current (RST)	-1	-	100	µA
IIH1	Input High Current (all other inputs)	-1		1	µA
IOZ	Tri-state Leakage Current (Port 0,1,2,3)	-10		10	µA
ICC	Power Supply Current:			See Note 1	mA
CIO	Pin Capacitance	-	4	-	pF

Notes:

1. Power dissipation characterization is in progress. Values will be provided upon completion of this process.

A.C. Characteristics[1]

External Program Memory Characteristics

Symbol	Parameter	12 MHz Osc		Variable Clock 1/TCLCL = 3.5 MHz TO 12 MHz		Unit
		Min	Max	Min	Max	
TLHLL	ALE Pulse Width					ns
TAVLL	Address Valid to ALE Low					ns
TLLAX[2]	Address Hold After ALE Low					ns
TLLIV	ALE Low to Valid Instr. In.					ns
TLLPL	ALE Low to PSENn Low					ns
TPLPH	PSENn Pulse Width					
TPLIV	PSENn Low to Valid Instr. In					
TPXIX	Input Instr. Hold After PSENn					ns
TPXIZ[3]	Input Instr. Float After PSENn					ns
TPXAV[3]	PSENn to Address Valid					ns
TAVIV	Address to Valid Instr. In					
TAZPL	Address Float to PSENn					ns

Notes:
1. Actual values will provided for the External Program Memory Characteristics, External Data Memory Characteristics, and Serial Interface Characteristics tables (pp. 26 – 27) upon completion of device testing. Values from the original device data sheet may be used to characterize parameters in the interim.
2.TLLAX for access to program memory is different from TLLAX for data memory.
3. Interfacing RUPI-44 devices with float times up to 75ns is permissible. This limited bus contention will not cause any damage to Port 0 drivers

External Data Memory Characteristics

Symbol	Parameter	12 MHz Osc		Variable Clock 1/TCLCL = 3.5 MHz TO 12 MHz		Unit
		Min	Max	Min	Max	
TRLRH	RDn Pulse Width					ns
TWLWH	WRn Pulse Width					ns
TLLAX	Address Hold After ALE					ns
TRLDV	RDn Low to Valid Data In.					ns
TRHDX	Data Hold After RDn					ns
TRHDZ	Data Float After RDn					ns
TLLDV	ALE Low to Valid Data In					ns
TAVDV	Address to Valid Data In.					ns
TLLWL	ALE Low to RDn or WRn Low					ns
TAVWL	Address to RDn or WRn Low					ns
TQVWX	Data Valid to WRn Transistion					
TQVWH	Data Setup Before WRn High					ns
TWHQX	Data Held After WRn					ns
TRLAZ	RDn Low to Address Float					ns
TWHLH	RDn or WRn High to ALE High					

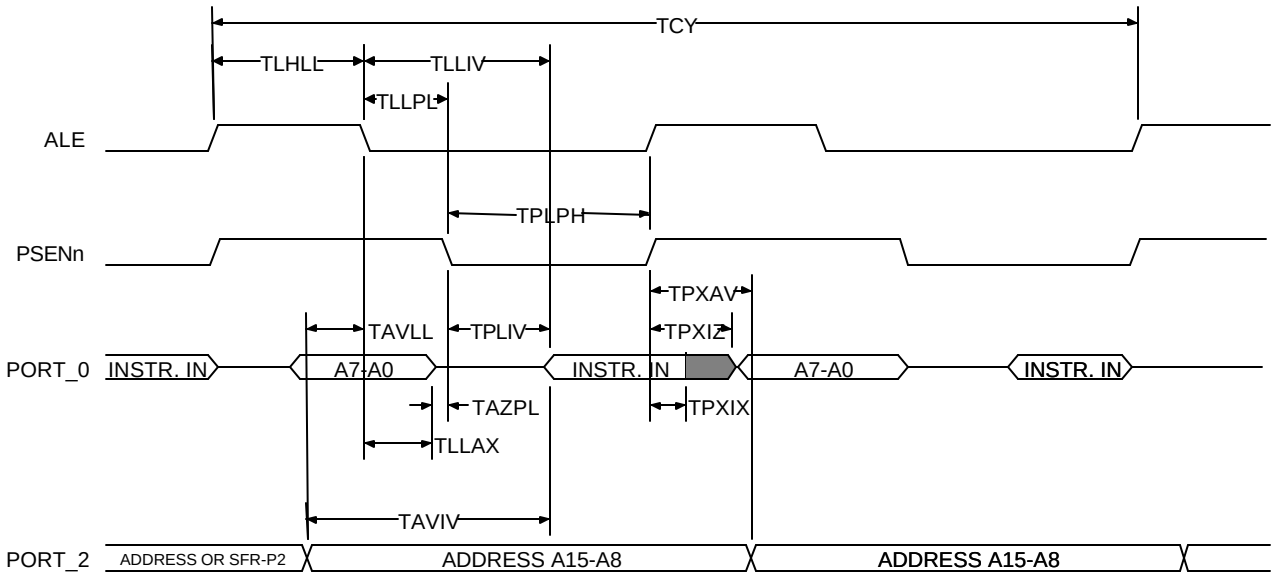
Serial Interface Characteristics

Symbol	Parameter	Min	Max	Unit
TDCY	Data Clock			ns
TDCL	Data Clock Low			ns
TDCH	Data Clock High			ns
tTD	Transmit Data Delay			ns
tDSS	Data Setup Time			ns
tDHS	Data Hold Time			ns

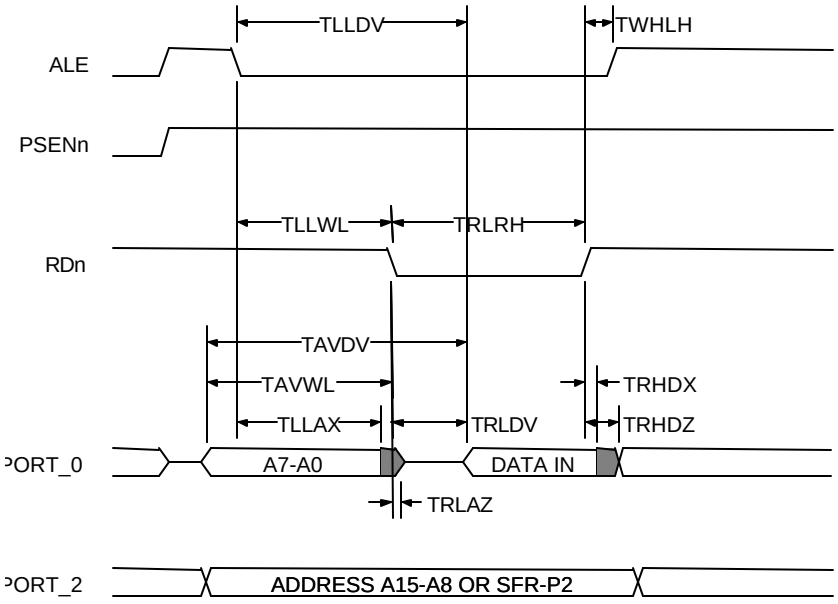
Waveforms

Memory Access

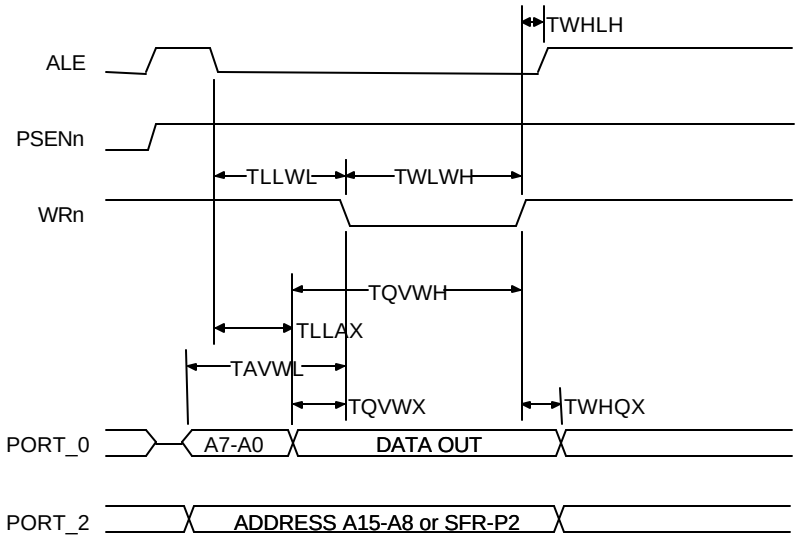
Program Memory Read Cycle



Data Memory Read Cycle

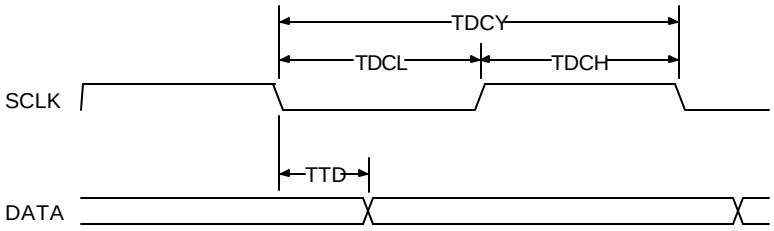


Data Memory Write Cycle

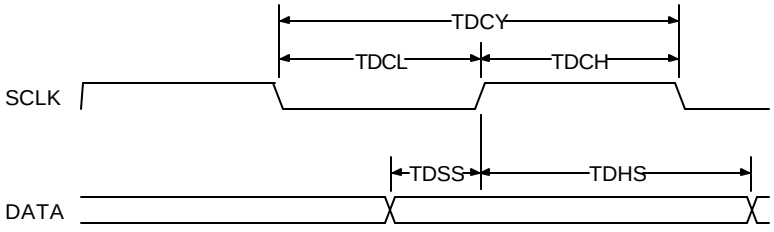


Serial I/O Waveforms

Synchronous Data Transmission

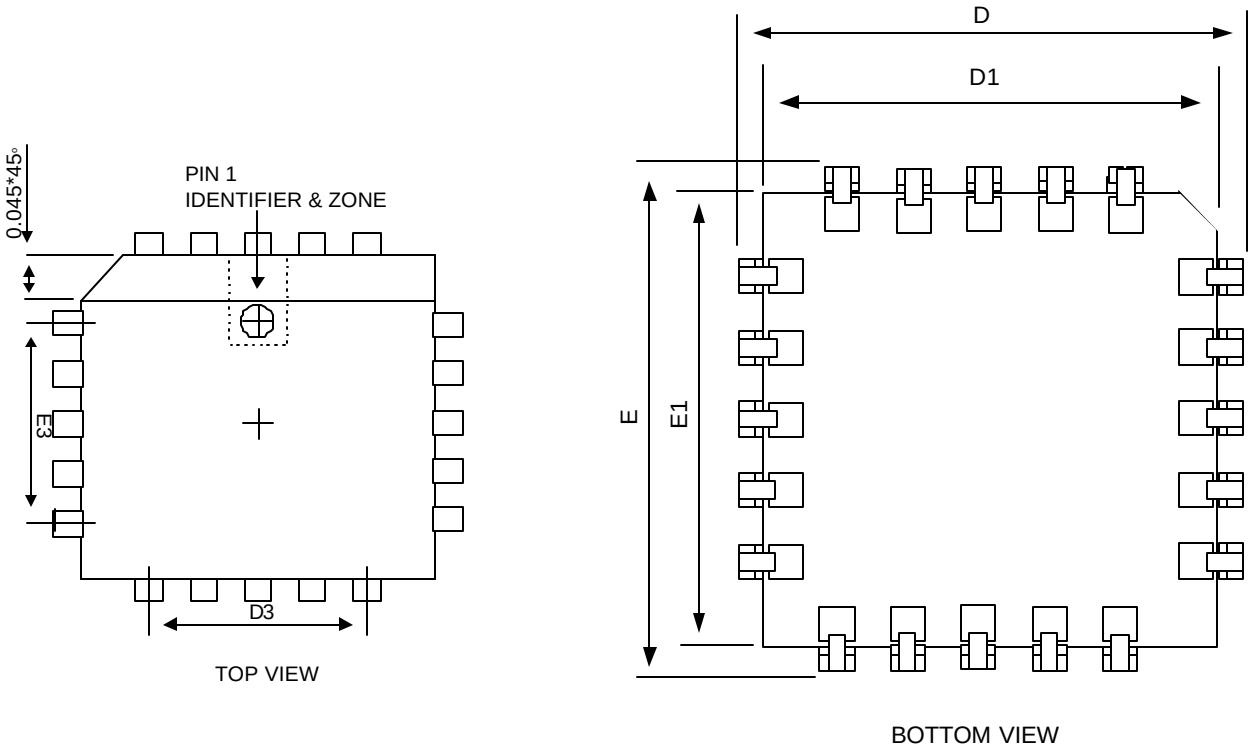


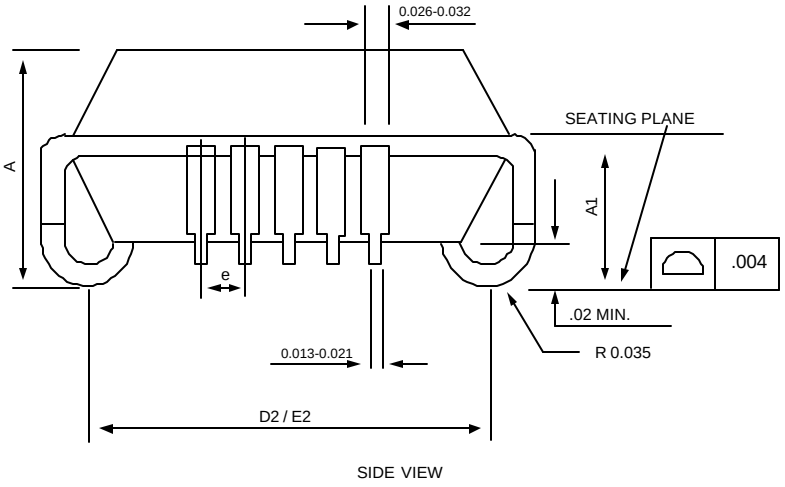
Synchronous Data Reception



Packaging Information

PLCC Package

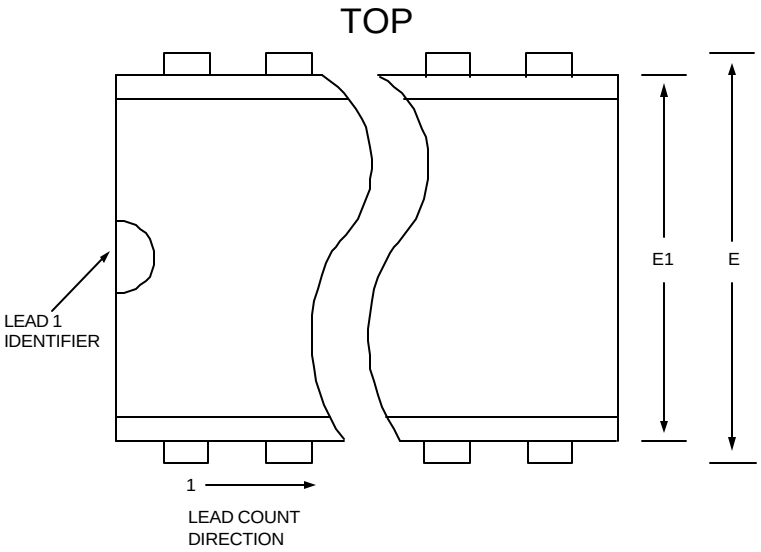


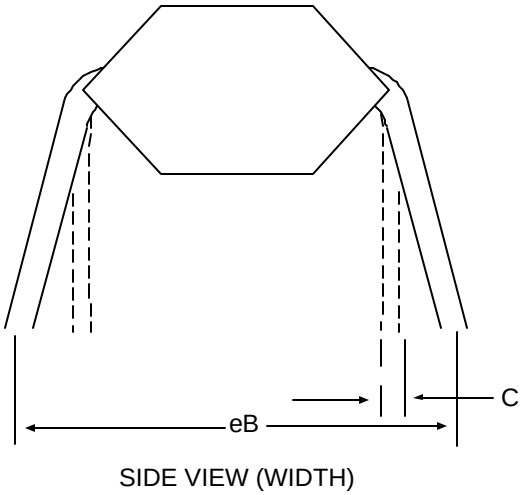


Package Dimensions for 44 Lead PLCC

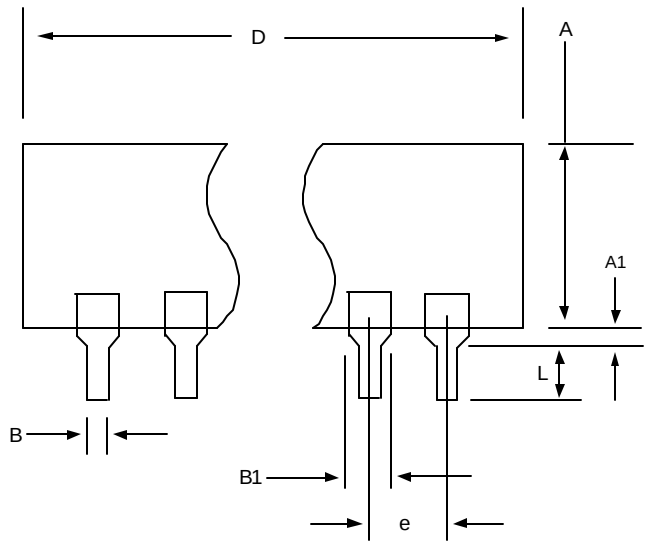
Symbol	Typical (in Inches)
A	0.180
A1	0.110
D1	0.653
D2	0.610
D3	0.500
E1	0.653
E2	0.610
E3	0.500
e	0.050
D	0.690
E	0.690

PDIP Package





SIDE VIEW (WIDTH)



SIDE VIEW (LENGTH)

Package Dimensions for 40 Lead PDIP (600 mil.)

Symbol	Typical (in Inches)
A	0.155
A1	0.010
B	0.018
B1	0.050
C	0.010
D	2.055
E	0.600
E1	0.545
e	0.100
eB	0.650
L	0.130

• Ordering Information

Part Number	Temperature Grade
IA8044-PDW40I-00	Industrial
IA8044-PLC44I-00	Industrial
IA8344-PDW40I-00	Industrial
IA8344-PLC44I-00	Industrial

• Cross Reference to Original Part Numbers

innovASIC Part Number	IntelÒ Part Number
IA8044-PLC44I	❑ N8044AH
	❑ N8044AH-R0117
IA8044-PDW40I	❑ P8044
	❑ P8044AH
	❑ P8044AH-R0117
	❑ TP8044AH
	❑ TP8044AH-R0117
IA8344-PLC44I	❑ N8344AH
	❑ TN8344AH
IA8344-PDW40I	❑ P8344
	❑ P8344AH
	❑ TP8344AH

• Errata

There is no errata for this device.