XMC4500

Microcontroller Series
for Industrial Applications

XMC4000 Family

ARM® Cortex™-M4
32-bit processor core

PRELIMINARY

Data Sheet
V0.6 2012-02

Microcontrollers

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About this Document

This Data Sheet is addressed to embedded hardware and software developers. It provides the reader with detailed descriptions about the ordering designations, available features, electrical and physical characteristics of the XMC4500 series devices.

The document describes the characteristics of a superset of the XMC4500 series devices. For simplicity, the various device types are referred to by the collective term XMC4500 throughout this manual.

XMC4000 Family User Documentation

The set of user documentation includes:

- **Reference Manual**
  – decribes the functionality of the superset of devices.
- **Data Sheets**
  – list the complete ordering designations, available features and electrical characteristics of derivative devices.
- **Errata Sheets**
  – list deviations from the specifications given in the related Reference Manual or Data Sheets. Errata Sheets are provided for the superset of devices.

Attention: Please consult all parts of the documentation set to attain consolidated knowledge about your device.

Application related guidance is provided by **Users Guides** and **Application Notes**.

Please refer to **http://www.infineon.com/xmc4000** to get access to the latest versions of those documents.

1 Summary of Features

The XMC4500 devices are members of the XMC4000 family of microcontrollers based on the ARM Cortex-M4 processor core. The XMC4000 is a family of high performance and energy efficient microcontrollers optimized for Industrial Connectivity, Industrial Control, Power Conversion, Sense & Control.

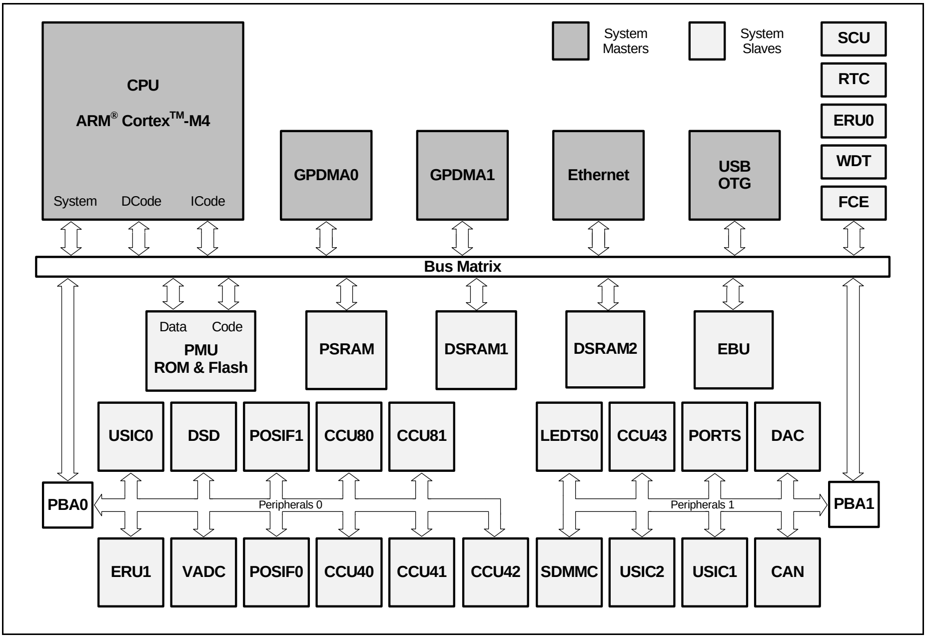


Figure 1 System Block Diagram

CPU Subsystem

- CPU Core
  - High Performance 32-bit ARM Cortex-M4 CPU
  - 16-bit and 32-bit Thumb2 instruction set
  - DSP/MAC instructions
  - System timer (SysTick) for Operating System support
- Floating Point Unit
- Memory Protection Unit
- Nested Vectored Interrupt Controller
- Two General Purpose DMA with up-to 12 channels
- Event Request Unit (ERU) for programmable processing of external and internal service requests

- Flexible CRC Engine (FCE) for multiple bit error detection

On-Chip Memories

- 16 KB on-chip boot ROM
- 112 KB on-chip high-speed program memory
- 64 KB on-chip high speed data memory
- 32 KB on-chip high-speed communication
- 1024 KB on-chip Flash Memory with 4 KB instruction cache

Communication Peripherals

- Ethernet MAC module capable of 10/100 Mbit/s transfer rates
- Universal Serial Bus, USB 2.0 host, Full-Speed OTG, with integrated PHY
- Controller Area Network interface (MultiCAN), Full-CAN/Basic-CAN with 3 nodes, 64 message objects, data rate up to 1MBit/s
- Six Universal Serial Interface Channels (USIC),providing 6 serial channels, usable as UART, double-SPI, quad-SPI, IIC, IIS and LIN interfaces
- LED and Touch-Sense Controller (LEDTS) for Human-Machine interface
- SD and Multi-Media Card interface (SDMMC) for data storage memory cards
- External Bus Interface Unit (EBU) enabling communication with external memories and off-chip peripherals

Analog Frontend Peripherals

- Four Analog-Digital Converters (VADC) of 12-bit resolution, 8 channels each, with input out-of-range comparators
- Delta Sigma Demodulator with four channels, digital input stage for A/D signal conversion
- Digital-Analogue Converter (DAC) with two channels of 12-bit resolution

Industrial Control Peripherals

- Two Capture/Compare Units 8 (CCU8) for motor control and power conversion
- Four Capture/Compare Units 4 (CCU4) for use as general purpose timers
- Two Position Interfaces (POSIF) for servo motor positioning
- Window Watchdog Timer (WDT) for safety sensitive applications
- Die Temperature Sensor (DTS)
- Real Time Clock module with alarm support
- System Control Unit (SCU) for system configuration and control

Input/Output Lines

- Programmable port driver control module (PORTS)
- Individual bit addressability

- Tri-stated in input mode
- Push/pull or open drain output mode
- Boundary scan test support over JTAG interface

On-Chip Debug Support

- Full support for debug features: 8 breakpoints, CoreSight, trace
- Various interfaces: ARM-JTAG, SWD, single wire trace

Packages

- PG-LFBGA-144
- PG-LQFP-144
- PG-LQFP-100

1.1 Ordering Information

The ordering code for an Infineon microcontroller provides an exact reference to a specific product. The code "XMC4<DDD>-<PPPP><T><FFFF>" identifies:

- <DDD> the derivatives function set
- <PPPP> the package type
- <T> the temperature range:
  - F: -40°C to 85°C
  - K: -40°C to 125°C
- <FFFF> the Flash memory size.

For ordering codes for the XMC4500 please contact your sales representative or local distributor.

This document describes several derivatives of the XMC4500 group, some descriptions may not apply to a specific product. Please see **Table 1**.

For simplicity the term **XMC4500** is used for all derivatives throughout this document.

1.2 Device Types

These device types are available and can be ordered through Infineon's direct and/or distribution channels.

Table 1 Synopsis of XMC4500 Device Types

Derivative[1)]	Flash Memory	Package	Note
XMC4500-E144F1024	1024 Kbytes	LFBGA-144	
XMC4500-F144x1024	1024 Kbytes	LQFP-144	
XMC4500-F144x768	768 Kbytes	LQFP-144	

Table 1 Synopsis of XMC4500 Device Types (cont'd)

Derivative[1)]	Flash Memory	Package	Note
XMC4504-F144x512	512 Kbytes	LQFP-144	No Ethernet, No USB, No MultiCAN
XMC4500-F100x1024	1024 Kbytes	LQFP-100	
XMC4500-F100x768	768 Kbytes	LQFP-100	
XMC4502-F100x768	768 Kbytes	LQFP-100	No Ethernet
XMC4504-F100x512	512 Kbytes	LQFP-100	No Ethernet, No USB, No MultiCAN

1) x is a placeholder for available temperature range.

1.3 Definition of Feature Variants

The XMC4500 types are offered with several memory sizes. **Table 2** describes the location of the available Flash memory, **Table 3** describes the location of the available SRAMs.

Table 2 Flash Memory Ranges

Total Flash Size	Cached Range	Uncached Range
512 Kbytes	$0800\ 0000_H$ – $0807\ FFFF_H$	$0C00\ 0000_H$ – $0C07\ FFFF_H$
768 Kbytes	$0800\ 0000_H$ – $080B\ FFFF_H$	$0C00\ 0000_H$ – $0C0B\ FFFF_H$
1,088 Kbytes	$0800\ 0000_H$ – $080F\ FFFF_H$	$0C00\ 0000_H$ – $0C0F\ FFFF_H$

Table 3 RAM Memory Ranges

Total Flash Size	Program SRAM	System Data SRAM	Communication Data SRAM
128 Kbytes	$1000\ 0000_H$ – $1000\ FFFF_H$	$2000\ 0000_H$ – $2000\ FFFF_H$	–
160 Kbytes	$1000\ 0000_H$ – $1000\ FFFF_H$	$2000\ 0000_H$ – $2000\ FFFF_H$	$3000\ 0000_H$ – $3000\ 7FFF_H$

2 General Device Information

This section summarizes the logic symbols and package pin configurations with a detailed list of the functional I/O mapping.

2.1 Logic Symbols

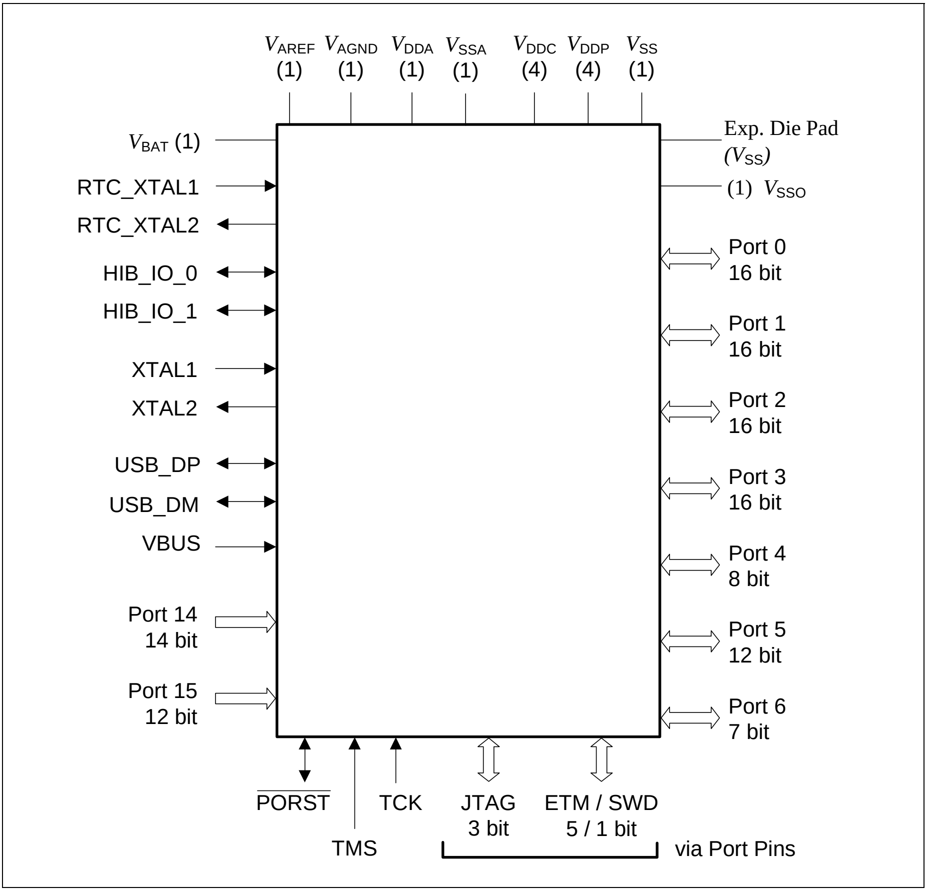


Figure 2 XMC4500 Logic Symbol PG-LQFP-144

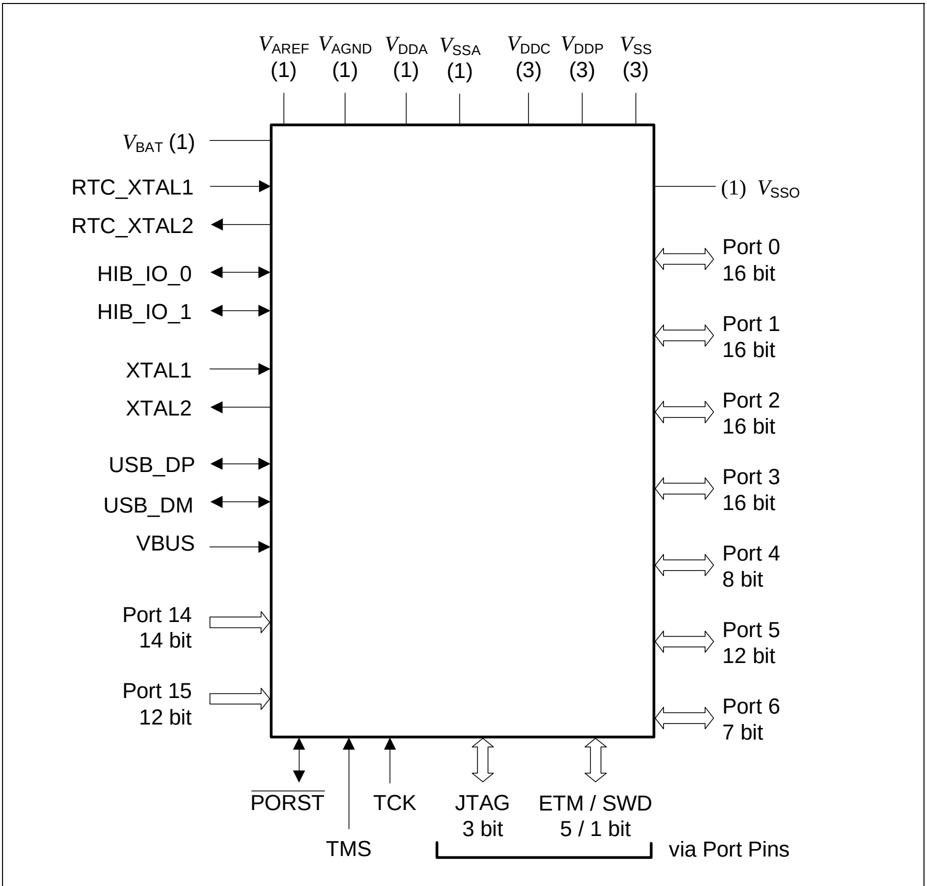


Figure 3 XMC4500 Logic Symbol PG-LFBGA-144

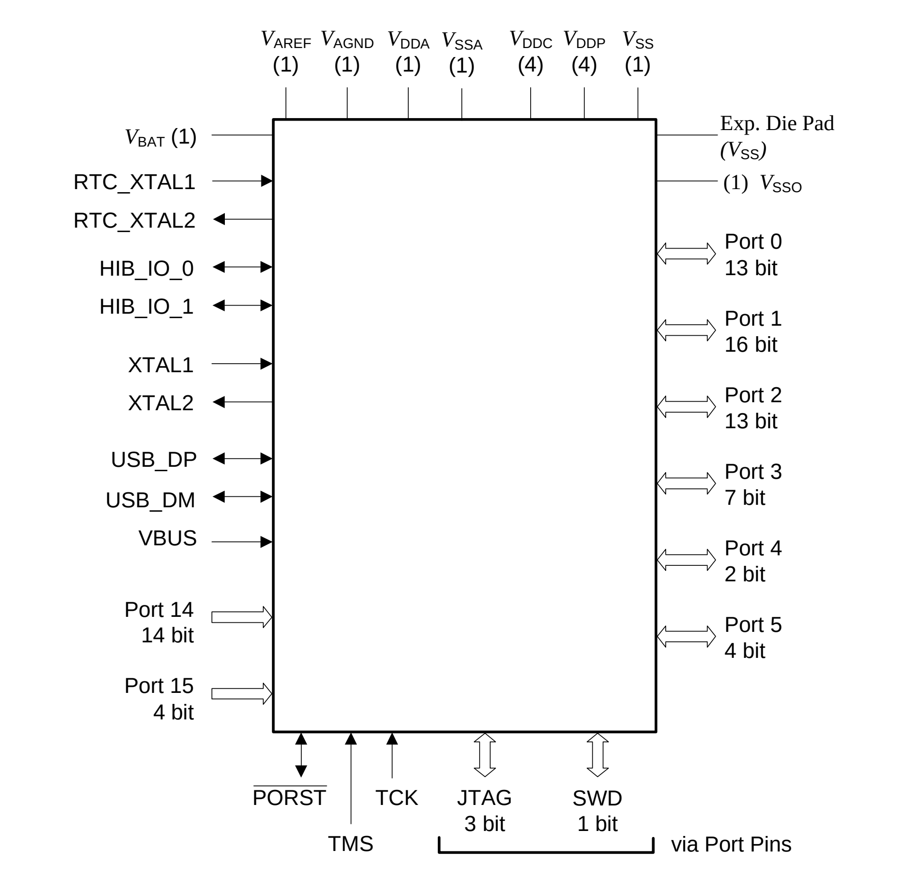


Figure 4 XMC4500 Logic Symbol PG-LQFP-100

2.2 Pin Configuration and Definition

The following figures summarize all pins, showing their locations on the four sides of the different packages.

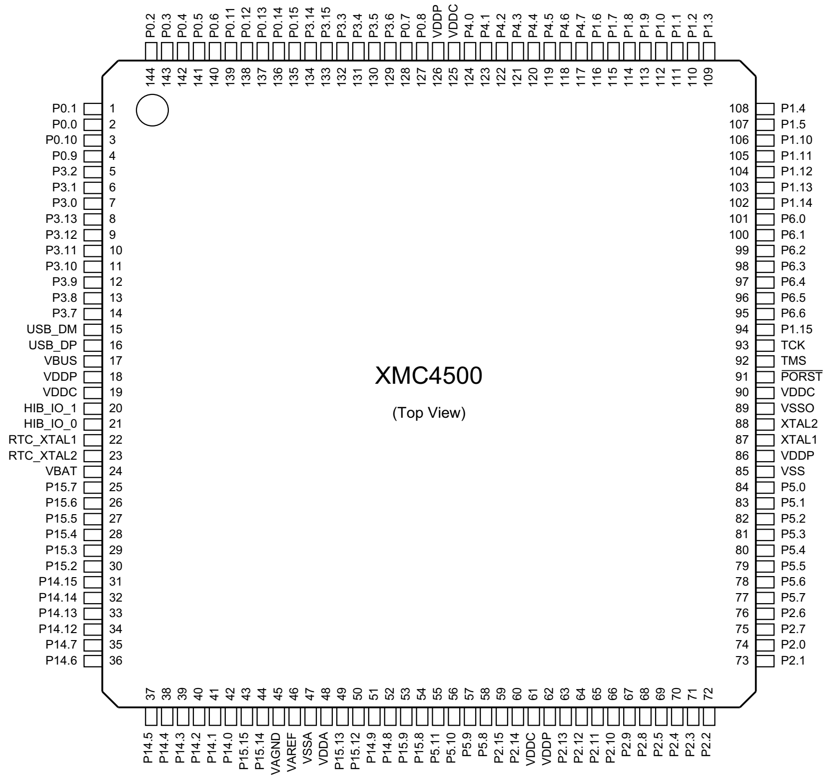


Figure 5 XMC4500 PG-LQFP-144 Pin Configuration (top view)

	1	2	3	4	5	6	7	8	9	10	11	12	
A	VSS	VDDC	P0.2	P0.3	P0.5	P0.6	P3.6	P0.8	P4.1	P1.8	VDDP	VSS	A
B	VDDP	P3.1	P3.2	P0.10	P0.4	P3.5	P0.7	P4.0	P1.6	P1.7	P1.9	VDDC	B
C	P3.0	P3.13	P0.1	P0.0	P0.13	P0.15	P4.4	P4.6	P4.7	P1.4	P1.2	P1.3	C
D	USB_DM	P3.12	P3.11	P0.9	P0.12	P3.14	P3.15	P4.5	P1.0	P1.5	P1.11	P1.10	D
E	USB_DP	VBUS	P3.8	P3.7	P0.11	P0.14	P3.4	P4.2	P1.1	P1.14	P1.12	P1.13	E
F	RTC_XTAL2	RTC_XTAL1	HIB_IO_1	HIB_IO_0	P3.9	P3.10	P3.3	P4.3	P6.1	P6.4	P6.5	P6.6	F
G	VBAT	P15.3	P15.5	P15.4	P15.6	P15.7	TMS	TCK	P6.3	P6.0	$\overline{\text{PORST}}$	P1.15	G
H	P15.2	P14.15	P14.14	P14.13	P5.10	P5.8	P5.2	P5.1	P5.0	P6.2	XTAL1	XTAL2	H
J	P14.12	P14.7	P14.6	P14.3	P5.11	P2.15	P5.7	P5.5	P2.6	P5.3	P2.0	VSSO	J
K	P14.4	P14.5	P14.2	P15.15	P15.12	P5.9	P2.14	P5.6	P2.7	P5.4	P2.2	P2.1	K
L	VDDA	P14.1	P14.0	P15.14	P14.9	P15.9	P2.12	P2.10	P2.8	P2.4	P2.3	VDDP	L
M	VSSA	VAGND	VAREF	P15.13	P14.8	P15.8	P2.13	P2.11	P2.9	P2.5	VDDC	VSS	M
	1	2	3	4	5	6	7	8	9	10	11	12	

XMC4500 - (top view)

Figure 6 XMC4500 PG-LFBGA-144 Pin Configuration (top view)

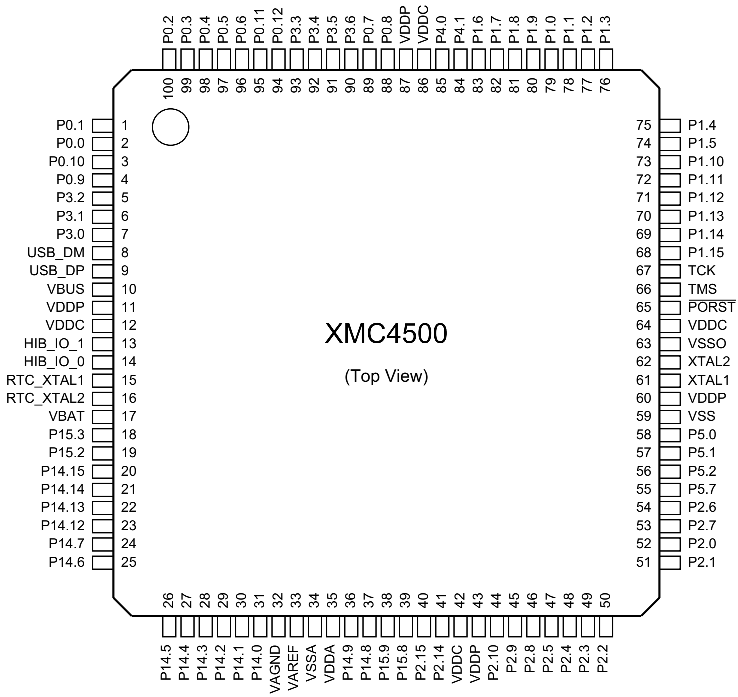


Figure 7 XMC4500 PG-LQFP-100 Pin Configuration (top view)

2.2.1 Package Pin Summary

The following general building block is used to describe each pin:

Table 4 Package Pin Mapping Description

Function	Package A	Package B	...	Pad Type	Notes
Name	N	Ax	...	A2	

The table is sorted by the “Function” column, starting with the regular Port pins (Px.y), followed by the dedicated pins (i.e. $\overline{\mathrm{PORST}}$) and supply pins.

The following columns, titled with the supported package variants, lists the package pin number to which the respective function is mapped in that package.

The “Pad Type” indicates the employed pad type (A1, A1+, A2, special=special pad, In=input pad, AN/DIG IN=analog and digital input, Power=power supply). Details about the pad properties are defined in the Electrical Parameters.

In the “Notes”, special information to the respective pin/function is given, i.e. deviations from the default configuration after reset.

Table 5 Package Pin Mapping

Function	LQFP 144	LFBGA 144	LQFP 100	Pad Type	Notes
P0.0	2	C4	2	A1+	
P0.0	2	C4	2	A1+	
P0.1	1	C3	1	A1+	
P0.2	144	A3	100	A2	
P0.3	143	A4	99	A2	
P0.4	142	B5	98	A2	
P0.5	141	A5	97	A2	
P0.6	140	A6	96	A2	
P0.7	128	B7	89	A2	After a system reset, this pin selects HW0.
P0.8	127	A8	88	A2	After a system reset, this pin selects HW0 with a weak pull-down active.
P0.9	4	D4	4	A2	
P0.10	3	B4	3	A1+	
P0.11	139	E5	95	A1+	

Table 5 Package Pin Mapping (cont'd)

Function	LQFP 144	LFBGA 144	LQFP 100	Pad Type	Notes
P0.12	138	D5	94	A1+	
P0.13	137	C5	-	A1+	
P0.14	136	E6	-	A1+	
P0.15	135	C6	-	A1+	
P1.0	112	D9	79	A1+	
P1.1	111	E9	78	A1+	
P1.2	110	C11	77	A2	
P1.3	109	C12	76	A2	
P1.4	108	C10	75	A1+	
P1.5	107	D10	74	A1+	
P1.6	116	B9	83	A2	
P1.7	115	B10	82	A2	
P1.8	114	A10	81	A2	
P1.9	113	B11	80	A2	
P1.10	106	D12	73	A1+	
P1.11	105	D11	72	A1+	
P1.12	104	E11	71	A2	
P1.13	103	E12	70	A2	
P1.14	102	E10	69	A2	
P1.15	94	G12	68	A2	
P2.0	74	J11	52	A2	
P2.1	73	K12	51	A2	After a system reset, this pin selects HW0.
P2.2	72	K11	50	A2	
P2.3	71	L11	49	A2	
P2.4	70	L10	48	A2	
P2.5	69	M10	47	A2	
P2.6	76	J9	54	A1+	
P2.7	75	K9	53	A1+	
P2.8	68	L9	46	A2	
P2.9	67	M9	45	A2	
P2.10	66	L8	44	A2	

Table 5 Package Pin Mapping (cont'd)

Function	LQFP 144	LFBGA 144	LQFP 100	Pad Type	Notes
P2.11	65	M8	-	A2	
P2.12	64	L7	-	A2	
P2.13	63	M7	-	A2	
P2.14	60	K7	41	A2	
P2.15	59	J6	40	A2	
P3.0	7	C1	7	A2	
P3.1	6	B2	6	A2	
P3.2	5	B3	5	A2	
P3.3	132	F7	93	A1+	
P3.4	131	E7	92	A1+	
P3.5	130	B6	91	A2	
P3.6	129	A7	90	A2	
P3.7	14	E4	-	A1+	
P3.8	13	E3	-	A1+	
P3.9	12	F5	-	A1+	
P3.10	11	F6	-	A1+	
P3.11	10	D3	-	A1+	
P3.12	9	D2	-	A2	
P3.13	8	C2	-	A2	
P3.14	134	D6	-	A1+	
P3.15	133	D7	-	A1+	
P4.0	124	B8	85	A2	
P4.1	123	A9	84	A2	
P4.2	122	E8	-	A1+	
P4.3	121	F8	-	A1+	
P4.4	120	C7	-	A1+	
P4.5	119	D8	-	A1+	
P4.6	118	C8	-	A1+	
P4.7	117	C9	-	A1+	
P5.0	84	H9	58	A1+	
P5.1	83	H8	57	A1+	
P5.2	82	H7	56	A1+	

Table 5 Package Pin Mapping (cont'd)

Function	LQFP 144	LFBGA 144	LQFP 100	Pad Type	Notes
P5.3	81	J10	-	A2	
P5.4	80	K10	-	A2	
P5.5	79	J8	-	A2	
P5.6	78	K8	-	A2	
P5.7	77	J7	55	A1+	
P5.8	58	H6	-	A2	
P5.9	57	K6	-	A2	
P5.10	56	H5	-	A1+	
P5.11	55	J5	-	A1+	
P6.0	101	G10	-	A2	
P6.1	100	F9	-	A2	
P6.2	99	H10	-	A2	
P6.3	98	G9	-	A1+	
P6.4	97	F10	-	A2	
P6.5	96	F11	-	A2	
P6.6	95	F12	-	A2	
P14.0	42	L3	31	AN/DIG_IN	
P14.1	41	L2	30	AN/DIG_IN	
P14.2	40	K3	29	AN/DIG_IN	
P14.3	39	J4	28	AN/DIG_IN	
P14.4	38	K1	27	AN/DIG_IN	
P14.5	37	K2	26	AN/DIG_IN	
P14.6	36	J3	25	AN/DIG_IN	
P14.7	35	J2	24	AN/DIG_IN	
P14.8	52	M5	37	AN/DAC/DIG_IN	
P14.9	51	L5	36	AN/DAC/DIG_IN	
P14.12	34	J1	23	AN/DIG_IN	
P14.13	33	H4	22	AN/DIG_IN	
P14.14	32	H3	21	AN/DIG_IN	
P14.15	31	H2	20	AN/DIG_IN	
P15.2	30	H1	19	AN/DIG_IN	

Table 5 Package Pin Mapping (cont'd)

Function	LQFP 144	LFBGA 144	LQFP 100	Pad Type	Notes
P15.3	29	G2	18	AN/DIG_IN	
P15.4	28	G4	-	AN/DIG_IN	
P15.5	27	G3	-	AN/DIG_IN	
P15.6	26	G5	-	AN/DIG_IN	
P15.7	25	G6	-	AN/DIG_IN	
P15.8	54	M6	39	AN/DIG_IN	
P15.9	53	L6	38	AN/DIG_IN	
P15.12	50	K5	-	AN/DIG_IN	
P15.13	49	M4	-	AN/DIG_IN	
P15.14	44	L4	-	AN/DIG_IN	
P15.15	43	K4	-	AN/DIG_IN	
USB_DP	16	E1	9	special	
USB_DM	15	D1	8	special	
HIB_IO_0	21	F4	14	A1 special	At the first power-up and with every reset of the hibernate domain this pin is configured as open-drain output and drives "0".
HIB_IO_1	20	F3	13	A1 special	At the first power-up and with every reset of the hibernate domain this pin is configured as input with no pull device active.
TCK	93	G8	67	A1	Weak pull-down active.
TMS	92	G7	66	A1+	Weak pull-up active.
$\overline{\text{PORST}}$	91	G11	65	special	Weak pull-up permanently active, strong pull-down controlled by EVR.
XTAL1	87	H11	61	clock_IN	
XTAL2	88	H12	62	clock_O	
RTC_XTAL1	22	F2	15	clock_IN	
RTC_XTAL2	23	F1	16	clock_O	
VBAT	24	G1	17	Power	
VBUS	17	E2	10	special	
VAREF	46	M3	33	AN_Ref	

Table 5 Package Pin Mapping (cont'd)

Function	LQFP 144	LFBGA 144	LQFP 100	Pad Type	Notes
VAGND	45	M2	32	AN_Ref	
VDDA	48	L1	35	AN_Power	
VSSA	47	M1	34	AN_Power	
VDDC	19	-	12	Power	
VDDC	61	-	42	Power	
VDDC	90	-	64	Power	
VDDC	125	-	86	Power	
VDDC	-	A2	-	Power	
VDDC	-	B12	-	Power	
VDDC	-	M11	-	Power	
VDDP	18	-	11	Power	
VDDP	62	-	43	Power	
VDDP	86	-	60	Power	
VDDP	126	-	87	Power	
VDDP	-	A11	-	Power	
VDDP	-	B1	-	Power	
VDDP	-	L12	-	Power	
VSS	85	-	59	Power	
VSS	-	A1	-	Power	
VSS	-	A12	-	Power	
VSS	-	M12	-	Power	
VSSO	89	J12	63	Power	
VSS	Exp. Pad	-	Exp. Pad	Power	**Exposed Die Pad** The exposed die pad is connected internally to V_{SS}. For proper operation, it is mandatory to connect the exposed pad to the board ground. For thermal aspects, please refer to the Package Parameters.

2.2.2 Port I/O Functions

The following general building block is used to describe each PORT pin:

Table 6 Port I/O Function Description

Function	Outputs			Inputs		
	ALT1	**ALTn**	**HWO0**	**HWI0**	**Input**	**Input**
P0.0		MODA.OUT	MODB.OUT	MODB.INA	MODC.INA	
Pn.y	MODA.OUT				MODA.INA	MODC.INB

Pn.y is the port pin name, defining the control and data bits/registers associated with it. As GPIO, the port is under software control. Its input value is read via Pn_IN.y, Pn_OUT defines the output value.

Up to four alternate output functions (ALT1/2/3/4) can be mapped to a single port pin, selected by Pn_IOCR.PC. The output value is directly driven by the respective module, with the pin characteristics controlled by the port registers (within the limits of the connected pad).

The port pin input can be connected to multiple peripherals. Most peripherals have an input multiplexer to select between different possible input sources.
The input path is also active while the pin is configured as output. This allows to feedback an output to on-chip resources without wasting an additional external pin.

By Pn_HWSEL it is possible to select between different hardware "masters" (HWO0/HWI0, HWO1/HWI1). The selected peripheral can take control of the pin(s). Hardware control overrules settings in the respective port pin registers.

2.2.2.1 Port I/O Function Table

Table 2-1 Port I/O Functions

Function	Outputs						Inputs									
	ALT1	ALT2	ALT3	ALT4	HWO0	HWO1	HWI0	HWI1	Input	Input	Input	Input	Input	Input	Input	Input
P0.0		CAN.N0_TXD	CCU80.OUT21	LEDTS0.COL2					U1C1.DX0D	ETH0.CLK_RMIIB	ERU0.0B0					
P0.1	USB.DRIVEVBUS	U1C1.DOUT0	CCU80.OUT11	LEDTS0.COL3						ETH0.CRS_DVB	ERU0.0A0					
P0.2		U1C1.SELO1	CCU80.OUT01		U1C0.DOUT3	EBU.AD0	U1C0.HWIN3	EBU.D0	ETH0.RXD0B		ERU0.3B3					
P0.3			CCU80.OUT20		U1C0.DOUT2	EBU.AD1	U1C0.HWIN2	EBU.D1	ETH0.RXD1B			ERU1.3B0				
P0.4	ETH0.TX_EN		CCU80.OUT10		U1C0.DOUT1	EBU.AD2	U1C0.HWIN1	EBU.D2		U1C0.DX0A	ERU0.2B3					
P0.5	ETH0.TXD0	U1C0.DOUT0	CCU80.OUT00		U1C0.DOUT0	EBU.AD3	U1C0.HWIN0	EBU.D3		U1C0.DX0B		ERU1.3A0				
P0.6	ETH0.TXD1	U1C0.SELO0	CCU80.OUT30			$\overline{\text{EBU.ADV}}$				U1C0.DX2A	ERU0.3B2		CCU80.IN2B			
P0.7	WWDT.SERVICE_OUT	U0C0.SELO0				EBU.AD6	DB.TDI	EBU.D6	U0C0.DX2B	DSD.DIN1A	ERU0.2B1		CCU80.IN0A	CCU80.IN1A	CCU80.IN2A	CCU80.IN3A
P0.8	SCU.EXTCLK	U0C0.SCLKOUT				EBU.AD7	$\overline{\text{DB.TRST}}$	EBU.D7	U0C0.DX1B	DSD.DIN0A	ERU0.2A1		CCU80.IN1B			
P0.9		U1C1.SELO0	CCU80.OUT12	LEDTS0.COL0	ETH0.MDO	$\overline{\text{EBU.CS1}}$	ETH0.MDIA		U1C1.DX2A	USB.ID	ERU0.1B0					
P0.10	ETH0.MDC	U1C1.SCLKOUT	CCU80.OUT02	LEDTS0.COL1					U1C1.DX1A		ERU0.1A0					
P0.11		U1C0.SCLKOUT	CCU80.OUT31			$\overline{\text{EBU.BREQ}}$			ETH0.RXERB	U1C0.DX1A	ERU0.3A2					
P0.12		U1C1.SELO0	CCU40.OUT3			$\overline{\text{EBU.HLDA}}$		$\overline{\text{EBU.HLDA}}$		U1C1.DX2B	ERU0.2B2					
P0.13		U1C1.SCLKOUT	CCU40.OUT2							U1C1.DX1B	ERU0.2A2					
P0.14		U1C0.SELO1	CCU40.OUT1		U1C1.DOUT3		U1C1.HWIN3						CCU42.IN3C			
P0.15		U1C0.SELO2	CCU40.OUT0		U1C1.DOUT2		U1C1.HWIN2						CCU42.IN2C			
P1.0	DSD.CGPWMN	U0C0.SELO0	CCU40.OUT3	ERU1.PDOUT3					U0C0.DX2A		ERU0.3B0		CCU40.IN3A			
P1.1	DSD.CGPWMP	U0C0.SCLKOUT	CCU40.OUT2	ERU1.PDOUT2			SDMMC.SDWC		U0C0.DX1A	POSIF0.IN2A	ERU0.3A0		CCU40.IN2A			
P1.2			CCU40.OUT1	ERU1.PDOUT1	U0C0.DOUT3	EBU.AD14	U0C0.HWIN3	EBU.D14		POSIF0.IN1A		ERU1.2B0	CCU40.IN1A			
P1.3		U0C0.MCLKOUT	CCU40.OUT0	ERU1.PDOUT0	U0C0.DOUT2	EBU.AD15	U0C0.HWIN2	EBU.D15		POSIF0.IN0A		ERU1.2A0	CCU40.IN0A			
P1.4	WWDT.SERVICE_OUT	CAN.N0_TXD	CCU80.OUT33	CCU81.OUT20	U0C0.DOUT1		U0C0.HWIN1		U0C0.DX0B	CAN.N1_RXDD	ERU0.2B0		CCU41.IN0C			
P1.5	CAN.N1_TXD	U0C0.DOUT0	CCU80.OUT23	CCU81.OUT10	U0C0.DOUT0		U0C0.HWIN0		U0C0.DX0A	CAN.N0_RXDA	ERU0.2A0	ERU1.0A0	CCU41.IN1C	DSD.DIN2B		
P1.6		U0C0.SCLKOUT			SDMMC.DATA1_OUT	EBU.AD10	SDMMC.DATA1_IN	EBU.D10	DSD.DIN2A							
P1.7		U0C0.DOUT0	DSD.MCLK2		SDMMC.DATA2_OUT	EBU.AD11	SDMMC.DATA2_IN	EBU.D11		DSD.MCLK2A						

Table 2-1 Port I/O Functions (cont'd)

Function	Outputs						Inputs									
	ALT1	**ALT2**	**ALT3**	**ALT4**	**HWO0**	**HWO1**	**HWI0**	**HWI1**	**Input**	**Input**	**Input**	**Input**	**Input**	**Input**	**Input**	**Input**
P1.8		U0C0.SELO1	DSD.MCLK1		SDMMC.DATA4_OUT	EBU.AD12	SDMMC.DATA4_IN	EBU.D12	CAN.N2_RXDA	DSD.MCLK1A						
P1.9		CAN.N2_TXD			SDMMC.DATA5_OUT	EBU.AD13	SDMMC.DATA5_IN	EBU.D13		DSD.MCLK0A						
P1.10	ETH0.MDC	U0C0.SCLKOUT	CCU81.OUT21				$\overline{\text{SDMMC.SDCD}}$						CCU41.IN2C			
P1.11		U0C0.SELO0	CCU81.OUT11		ETH0.MDO		ETH0.MDIC						CCU41.IN3C			
P1.12	ETH0.TX_EN	CAN.N1_TXD	CCU81.OUT01		SDMMC.DATA6_OUT	EBU.AD16	SDMMC.DATA6_IN	EBU.D16								
P1.13	ETH0.TXD0	U0C1.SELO3	CCU81.OUT20		SDMMC.DATA7_OUT	EBU.AD17	SDMMC.DATA7_IN	EBU.D17	CAN.N1_RXDC							
P1.14	ETH0.TXD1	U0C1.SELO2	CCU81.OUT10			EBU.AD18		EBU.D18								
P1.15	SCU.EXTCLK	DSD.MCLK2	CCU81.OUT00			EBU.AD19		EBU.D19		DSD.MCLK2B		ERU1.1A0				
P2.0		CCU81.OUT21	DSD.CGPWMN	LEDTS0.COL1	ETH0.MDO	EBU.AD20	ETH0.MDIB	EBU.D20			ERU0.0B3		CCU40.IN1C			
P2.1		CCU81.OUT11	DSD.CGPWMP	LEDTS0.COL0	DB.TDO/TRACESWO	EBU.AD21		EBU.D21	ETH0.CLK_RMIIA			ERU1.0B0	CCU40.IN0C			
P2.2	VADC.EMUX00	CCU81.OUT01	CCU41.OUT3	LEDTS0.LINE0	LEDTS0.EXTENDED0	EBU.AD22	LEDTS0.TSIN0A	EBU.D22	ETH0.RXD0A	U0C1.DX0A	ERU0.1B2		CCU41.IN3A			
P2.3	VADC.EMUX01	U0C1.SELO0	CCU41.OUT2	LEDTS0.LINE1	LEDTS0.EXTENDED1	EBU.AD23	LEDTS0.TSIN1A	EBU.D23	ETH0.RXD1A	U0C1.DX2A	ERU0.1A2	POSIF1.IN2A	CCU41.IN2A			
P2.4	VADC.EMUX02	U0C1.SCLKOUT	CCU41.OUT1	LEDTS0.LINE2	LEDTS0.EXTENDED2	EBU.AD24	LEDTS0.TSIN2A	EBU.D24	ETH0.RXERA	U0C1.DX1A	ERU0.0B2	POSIF1.IN1A	CCU41.IN1A			
P2.5	ETH0.TX_EN	U0C1.DOUT0	CCU41.OUT0	LEDTS0.LINE3	LEDTS0.EXTENDED3	EBU.AD25	LEDTS0.TSIN3A	EBU.D25	ETH0.CRS_DVA	U0C1.DX0B	ERU0.0A2	POSIF1.IN0A	CCU41.IN0A			
P2.6	U2C0.SELO4		CCU80.OUT13	LEDTS0.COL3	U2C0.DOUT3		U2C0.HWIN3		DSD.DIN1B	CAN.N1_RXDA	ERU0.1B3		CCU40.IN3C			
P2.7	ETH0.MDC	CAN.N1_TXD	CCU80.OUT03	LEDTS0.COL2					DSD.DIN0B			ERU1.1B0	CCU40.IN2C			
P2.8	ETH0.TXD0		CCU80.OUT32	LEDTS0.LINE4	LEDTS0.EXTENDED4	EBU.AD26	LEDTS0.TSIN4A	EBU.D26	DAC.TRIGGER5				CCU40.IN0B	CCU40.IN1B	CCU40.IN2B	CCU40.IN3B
P2.9	ETH0.TXD1		CCU80.OUT22	LEDTS0.LINE5	LEDTS0.EXTENDED5	EBU.AD27	LEDTS0.TSIN5A	EBU.D27	DAC.TRIGGER4				CCU41.IN0B	CCU41.IN1B	CCU41.IN2B	CCU41.IN3B
P2.10	VADC.EMUX10				DB.ETM_TRACEDATA3	EBU.AD28		EBU.D28								
P2.11	ETH0.TXER		CCU80.OUT22		DB.ETM_TRACEDATA2	EBU.AD29		EBU.D29								
P2.12	ETH0.TXD2		CCU81.OUT33	ETH0.TXD0	DB.ETM_TRACEDATA1	EBU.AD30		EBU.D30					CCU43.IN3C			
P2.13	ETH0.TXD3			ETH0.TXD1	DB.ETM_TRACEDATA0	EBU.AD31		EBU.D31					CCU43.IN2C			
P2.14	VADC.EMUX11	U1C0.DOUT0	CCU80.OUT21		DB.ETM_TRACECLK	$\overline{\text{EBU.BC0}}$				U1C0.DX0D			CCU43.IN0B	CCU43.IN1B	CCU43.IN2B	CCU43.IN3B

Table 2-1 Port I/O Functions (cont'd)

Function	Outputs						Inputs									
	ALT1	**ALT2**	**ALT3**	**ALT4**	**HWO0**	**HWO1**	**HWI0**	**HWI1**	**Input**	**Input**	**Input**	**Input**	**Input**	**Input**	**Input**	**Input**
P2.15	VADC.EMUX12		CCU80.OUT11	LEDTS0. LINE6	LEDTS0. EXTENDED6	$\overline{\text{EBU.BC1}}$	LEDTS0. TSIN6A		ETH0.COLA	U1C0.DX0C			CCU42.IN0B	CCU42.IN1B	CCU42.IN2B	CCU42.IN3B
P3.0	U2C1.SELO0	U0C1. SCLKOUT	CCU42.OUT0			$\overline{\text{EBU.RD}}$			U0C1.DX1B				CCU80.IN2C	CCU81.IN0C		
P3.1		U0C1.SELO0				EBU.RD/ $\overline{\text{EBU.WR}}$			U0C1.DX2B		ERU0.0B1		CCU80.IN1C			
P3.2	USB. DRIVEVBUS	CAN.N0_TXD		LEDTS0.COLA		$\overline{\text{EBU.CS0}}$					ERU0.0A1		CCU80.IN0C			
P3.3		U1C1.SELO1	CCU42.OUT3		SDMMC.LED			$\overline{\text{EBU.WAIT}}$		DSD.DIN3B			CCU42.IN3A	CCU80.IN3B		
P3.4	U2C1. MCLKOUT	U1C1.SELO2	CCU42.OUT2	DSD.MCLK3	SDMMC. BUS_POWER			$\overline{\text{EBU.HOLD}}$	U2C1.DX0B	DSD.MCLK3B			CCU42.IN2A	CCU80.IN0B		
P3.5	U2C1.DOUT0	U1C1.SELO3	CCU42.OUT1	U0C1.DOUT0	SDMMC.CMD_ OUT	EBU.AD4	SDMMC.CMD_I N	EBU.D4	U2C1.DX0A		ERU0.3B1		CCU42.IN1A			
P3.6	U2C1. SCLKOUT	U1C1.SELO4	CCU42.OUT0	U0C1. SCLKOUT	SDMMC.CLK_ OUT	EBU.AD5	SDMMC.CLK_I N	EBU.D5	U2C1.DX1B		ERU0.3A1		CCU42.IN0A			
P3.7		CAN.N2_TXD	CCU41.OUT3	LEDTS0. LINE0					U2C0.DX0C							
P3.8	U2C0.DOUT0	U0C1.SELO3	CCU41.OUT2	LEDTS0. LINE1					CAN.N2_RXDB				POSIF1.IN2B			
P3.9	U2C0. SCLKOUT	CAN.N1_TXD	CCU41.OUT1	LEDTS0. LINE2									POSIF1.IN1B			
P3.10	U2C0.SELO0	CAN.N0_TXD	CCU41.OUT0	LEDTS0. LINE3	U0C1.DOUT3		U0C1.HWIN3						POSIF1.IN0B			
P3.11	U2C1.DOUT0	U0C1.SELO2	CCU42.OUT3	LEDTS0. LINE4	U0C1.DOUT2		U0C1.HWIN2		CAN.N1_RXDB					CCU81.IN3C		
P3.12		U0C1.SELO1	CCU42.OUT2	LEDTS0. LINE5	U0C1.DOUT1		U0C1.HWIN1		CAN.N0_RXDC	U2C1.DX0D				CCU81.IN2C		
P3.13	U2C1. SCLKOUT	U0C1.DOUT0	CCU42.OUT1	LEDTS0. LINE6	U0C1.DOUT0		U0C1.HWIN0		U0C1.DX0D				CCU80.IN3C	CCU81.IN1C		
P3.14		U1C0.SELO3			U1C1.DOUT1		U1C1.HWIN1			U1C1.DX0B			CCU42.IN1C			
P3.15		U1C1.DOUT0			U1C1.DOUT0		U1C1.HWIN0			U1C1.DX0A			CCU42.IN0C			
P4.0			DSD.MCLK1		SDMMC. DATA0_OUT	EBU.AD8	SDMMC. DATA0_IN	EBU.D8	U1C1.DX1C	DSD.MCLK1B	U0C1.DX0E	U2C1.DX0C				
P4.1	U2C1.SELO0	U1C1. MCLKOUT	DSD.MCLK0	U0C1.SELO0	SDMMC. DATA3_OUT	EBU.AD9	SDMMC. DATA3_IN	EBU.D9	U2C1.DX2B	DSD.MCLK0B		U2C1.DX2A				
P4.2	U2C1.SELO1	U1C1.DOUT0		U2C1. SCLKOUT					U1C1.DX0C			U2C1.DX1A	CCU43.IN1C			
P4.3	U2C1.SELO2	U0C0.SELO5	CCU43OUT3										CCU43.IN3A			
P4.4		U0C0.SELO4	CCU43OUT2		U2C1.DOUT3		U2C1.HWIN3						CCU43.IN2A			
P4.5		U0C0.SELO3	CCU43OUT1		U2C1.DOUT2		U2C1.HWIN2						CCU43.IN1A			
P4.6		U0C0.SELO2	CCU43OUT0		U2C1.DOUT1		U2C1.HWIN1		CAN.N2_RXDC				CCU43.IN0A			
P4.7		CAN.N2_TXD			U2C1.DOUT0		U2C1.HWIN0		U0C0.DX0C				CCU43.IN0C			

Table 2-1 Port I/O Functions (cont'd)

Function	Outputs						Inputs									
	ALT1	**ALT2**	**ALT3**	**ALT4**	**HWO0**	**HWO1**	**HWI0**	**HWI1**	**Input**	**Input**	**Input**	**Input**	**Input**	**Input**	**Input**	**Input**
P5.0	U2C0.DOUT0	DSD.CGPWMN	CCU81.OUT33		U2C0.DOUT0		U2C0.HWIN0		U2C0.DX0B	ETH0.RXD0D	U0C0.DX0D		CCU81.IN0A	CCU81.IN1A	CCU81.IN2A	CCU81.IN3A
P5.1	U0C0.DOUT0	DSD.CGPWMP	CCU81.OUT32		U2C0.DOUT1		U2C0.HWIN1		U2C0.DX0A	ETH0.RXD1D			CCU81.IN0B			
P5.2	U2C0. SCLKOUT		CCU81.OUT23						U2C0.DX1A	ETH0. CRS_DVD			CCU81.IN1B			
P5.3	U2C0.SELO0		CCU81.OUT22		EBU.CKE	EBU.A20			U2C0.DX2A	ETH0.RXERD			CCU81.IN2B			
P5.4	U2C0.SELO1		CCU81.OUT13		$\overline{\text{EBU.RAS}}$	EBU.A21				ETH0.CRSD			CCU81.IN3B			
P5.5	U2C0.SELO2		CCU81.OUT12		$\overline{\text{EBU.CAS}}$	EBU.A22				ETH0.COLD						
P5.6	U2C0.SELO3		CCU81.OUT03		EBU.BFCLKO	EBU.A23			EBU.BFCLKI							
P5.7			CCU81.OUT02	LEDTS0.COLA	U2C0.DOUT2		U2C0.HWIN2									
P5.8		U1C0. SCLKOUT	CCU80.OUT01		EBU.SDCLKO	$\overline{\text{EBU.CS2}}$			ETH0.RXD2A	U1C0.DX1B						
P5.9		U1C0.SELO0	CCU80.OUT20	ETH0.TX_EN	EBU.BFCLKO	$\overline{\text{EBU.CS3}}$			ETH0.RXD3A	U1C0.DX2B						
P5.10		U1C0. MCLKOUT	CCU80.OUT10	LEDTS0. LINE7	LEDTS0. EXTENDED7		LEDTS0. TSIN7A		ETH0. CLK_TXA							
P5.11		U1C0.SELO1	CCU80.OUT00						ETH0.CRSA							
P6.0	ETH0.TXD2	U0C1.SELO1	CCU81.OUT31		DB. ETM_TRACECLK	EBU.A16										
P6.1	ETH0.TXD3	U0C1.SELO0	CCU81.OUT30		DB. ETM_TRACEDATA3	EBU.A17			U0C1.DX2C							
P6.2	ETH0.TXER	U0C1. SCLKOUT	CCU43OUT3		DB. ETM_TRACEDATA2	EBU.A18			U0C1.DX1C							
P6.3			CCU43OUT2						U0C1.DX0C	ETH0.RXD3B						
P6.4		U0C1.DOUT0	CCU43OUT1		EBU.SDCLKO	EBU.A19			EBU.SDCLKI	ETH0.RXD2B						
P6.5		U0C1. MCLKOUT	CCU43OUT0		DB. ETM_TRACEDATA1	EBU.BC2			DSD.DIN3A	ETH0. CLK_RMIID						
P6.6			DSD.MCLK3		DB. ETM_TRACEDATA0	EBU.BC3			DSD.MCLK3A	ETH0. CLK_TXB						
P14.0									VADC.G0CH0							
P14.1									VADC.G0CH1							
P14.2									VADC.G0CH2	VADC.G1CH2						
P14.3									VADC.G0CH3	VADC.G1CH3			CAN.N0_RXDB			
P14.4									VADC.G0CH4		VADC.G2CH0					
P14.5									VADC.G0CH5		VADC.G2CH1		POSIF0.IN2B			
P14.6									VADC.G0CH6				POSIF0.IN1B		G0ORC6	
P14.7									VADC.G0CH7				POSIF0.IN0B		G0ORC7	

Table 2-1 Port I/O Functions (cont'd)

Function	Outputs						Inputs									
	ALT1	**ALT2**	**ALT3**	**ALT4**	**HWO0**	**HWO1**	**HWI0**	**HWI1**	**Input**	**Input**	**Input**	**Input**	**Input**	**Input**	**Input**	**Input**
P14.8					DAC.OUT_0					VADC.G1CH0		VADC.G3CH2	ETH0.RXD0C			
P14.9					DAC.OUT_1					VADC.G1CH1		VADC.G3CH3	ETH0.RXD1C			
P14.12										VADC.G1CH4						
P14.13										VADC.G1CH5						
P14.14										VADC.G1CH6					G1ORC6	
P14.15										VADC.G1CH7					G1ORC7	
P15.2											VADC.G2CH2					
P15.3											VADC.G2CH3					
P15.4											VADC.G2CH4					
P15.5											VADC.G2CH5					
P15.6											VADC.G2CH6					
P15.7											VADC.G2CH7					
P15.8												VADC.G3CH0	ETH0. CLK_RMIIC			
P15.9												VADC.G3CH1	ETH0. CRS_DVC			
P15.12												VADC.G3CH4				
P15.13												VADC.G3CH5				
P15.14												VADC.G3CH6				
P15.15												VADC.G3CH7				
USB_DP																
USB_DM																
HIB_IO_0	HIBOUT	WWDT. SERVICE_OUT							WAKEUPA							
HIB_IO_1	HIBOUT	WWDT. SERVICE_OUT							WAKEUPB							
TCK							DB.TCK/ SWCLK									
TMS					DB.TMS/ SWDIO											
$\overline{\text{PORST}}$																
XTAL1									U0C0.DX0F	U0C1.DX0F	U1C0.DX0F	U1C1.DX0F	U2C0.DX0F	U2C1.DX0F		
XTAL2																
RTC_XTAL1											ERU0.1B1					
RTC_XTAL2																

3 Electrical Parameters

Attention: All parameters in this chapter are preliminary target values and may change based on characterization results.

3.1 General Parameters

3.1.1 Parameter Interpretation

The parameters listed in this section partly represent the characteristics of the XMC4500 and partly its requirements on the system. To aid interpreting the parameters easily when evaluating them for a design, they are marked with an two-letter abbreviation in column “Symbol”:

- **CC**
  Such parameters indicate **C**ontroller **C**haracteristics, which are a distinctive feature of the XMC4500 and must be regarded for a system design.
- **SR**
  Such parameters indicate **S**ystem **R**equirements, which must be provided by the application system in which the XMC4500 is designed in.

3.1.2 Absolute Maximum Ratings

Stresses above the values listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions may affect device reliability.

Table 7 Absolute Maximum Rating Parameters

Parameter	Symbol		Values			Unit	Note / Test Condition
			Min.	Typ.	Max.		
Storage temperature	T_{ST}	SR	-65	–	150	°C	–
Voltage at 3.3 V power supply pins with respect to V_{SS}	V_{DDP}	SR	–	–	4.3	V	–
Voltage on any Class A and dedicated input pin with respect to V_{SS}	V_{IN}	SR	-0.5	–	V_{DDP} + 0.5 or max. 4.3	V	whichever is lower
Voltage on any analog input pin with respect to V_{AGND}	V_{AIN} V_{AREF}	SR	-0.5	–	tbd	V	–
Input current on any pin during overload condition	I_{IN}		-10	–	+10	mA	
Absolute maximum sum of all input circuit currents for one port group during overload condition[1)]	ΣI_{IN}		-25	–	+25	mA	
Absolute maximum sum of all input circuit currents during overload condition	ΣI_{IN}		-100	–	+100	mA	

1) The port groups are defined in **Table 9**.

3.1.3 Pin Reliability in Overload

When receiving signals from higher voltage devices, low-voltage devices experience overload currents and voltages that go beyond their own IO power supplies specification.

Table 8 defines overload conditions that will not cause any negative reliability impact if all the following conditions are met:

- full operation life-time is not exceeded
- **Operating Conditions** are met for
  - pad supply levels (V_{DDP} or V_{DDA})
  - temperature

If a pin current is out of the **Operating Conditions** but within the overload parameters, then the parameters functionality of this pin as stated in the Operating Conditions can no longer be guaranteed. Operation is still possible in most cases but with relaxed parameters.

Note: An overload condition on one or more pins does not require a reset.

Table 8 Overload Parameters

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Input current on any digital pin during overload condition	I_{IN}	-5	–	+5	mA	
Absolute maximum sum of all input circuit currents for one port group during overload condition[1)]	I_{ING}	-20	–	+20	mA	
Input current on analog pins	I_{INANA}	-3	–	+3	mA	
Absolute sum of all input circuit currents during overload condition	ΣI_{INS}	-80	–	80	mA	

1) The port groups are defined in **Table 9**.

Note: A series resistor at the pin to limit the current to the maximum permitted overload current is sufficient to handle failure situations like short to battery without having any negative reliability impact on the operational life-time.

Table 9 Port Groups for Overload and Short-Circuit Current Sum Parameters

Group	Pins
1	P0.[15:0], P3.[15:0]
2	P14.[15:0], P15.[15:0]
3	P2.[15:0], P5.[11:0]
4	P1.[15:0], P4.[7:0], P6.[6:0]

3.1.4 Pad Driver and Pad Classes Summary

This section gives an overview on the different pad driver classes and its basic characteristics. More details (mainly DC parameters) are defined in the **Section 3.2.1**.

Table 10 Pad Driver and Pad Classes Overview

Class	Power Supply	Type	Sub-Class	Speed Grade	Load	Termination
A	3.3 V	LVTTL I/O, LVTTL outputs	**A1** (e.g. GPIO)	6 MHz	100 pF	No
			A1+ (e.g. serial I/Os)	25 MHz	50 pF	Series termination recommended
			A2 (e.g. ext. Bus)	80 MHz	15 pF	Series termination recommended

3.1.5 Operating Conditions

The following operating conditions must not be exceeded in order to ensure correct operation and reliability of the XMC4500. All parameters specified in the following tables refer to these operating conditions, unless noted otherwise.

Table 11 Operating Conditions Parameters

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Ambient Temperature	T_A SR	-40	–	125	°C	
Junction temperature	T_J SR	-40	–	150	°C	
Digital supply voltage	V_{DDP} SR	3.13[1]	3.3	3.63 [2]	V	
Core Supply Voltage	V_{DDC} CC	–[1]	1.3	–	V	Generated internally
Digital ground voltage	V_{SS} SR	0	–	–	V	
ADC analog supply voltage	V_{DDA} SR	3.0	3.3	3.6[2]	V	
Analog ground voltage for V_{DDA}	V_{SSA} SR	-0.1	0	0.1	V	
Battery Supply Voltage for Hibernate Domain	V_{BAT} SR	1.8	–	3.6	V	
USB Supply Voltage	V_{BUS} SR	3.0	–	3.6[2]	V	
System Frequency	f_{SYS} SR	–	–	120	MHz	
Short circuit current of digital outputs[3]	I_{SC} SR	-5	–	5	mA	
Absolute sum of short circuit currents per pin group[4]	ΣI_{SC_PG} CC	–	–	20	mA	
Absolute sum of short circuit currents of the device	ΣI_{SC_D} CC	–	–	100	mA	

1) See also the Supply Monitoring thresholds, **Chapter 3.3.2**.

2) Voltage overshoot to 4.0 V is permissible at Power-Up and $\overline{\text{PORST}}$ low, provided the pulse duration is less than 100 µs and the cumulated sum of the pulses does not exceed 1 h.

3) Applicable for digital outputs.

4) The port groups are defined in **Table 9**.

3.2 DC Parameters

3.2.1 Input/Output Pins

Table 12 Standard_Pads Parameters

Parameter	Symbol	Values		Unit	Note / Test Condition
		Min.	Max.		
Pin capacitance (digital inputs/outputs)	C_{IO} CC	–	10	pF	T_A = 25 °C; f = 1 MHz
Pull-down current	$\|I_{PDL}\|$ CC	150	–	µA	$V_i \geq 0.6 \times V_{DDP}$
		–	10	µA	$V_i \leq 0.36 \times V_{DDP}$
Pull-Up current	$\|I_{PUH}\|$ CC	–	10	µA	$V_i \geq 0.6 \times V_{DDP}$
		100	–	µA	$V_i \leq 0.36 \times V_{DDP}$
Input Hysteresis for pads of all A classes[1)]	$HYSA$ CC	$0.1 \times V_{DDP}$	–	V	T_A = 25 °C; f = 1 MHz
$\overline{\text{PORST}}$ spike filter always blocked pulse duration	t_{SF1} CC	–	10	ns	
$\overline{\text{PORST}}$ spike filter pass-through pulse duration	t_{SF2} CC	100	–	ns	
$\overline{\text{PORST}}$ pull-down current	t_{SF2} CC	13	–	mA	V_i = 1 V

1) Hysteresis is implemented to avoid metastable states and switching due to internal ground bounce. It can not be guaranteed that it suppresses switching due to external system noise.

Table 13 Standard_Pads Class_A1

Parameter	Symbol	Values		Unit	Note / Test Condition
		Min.	Max.		
Input leakage current	I_{OZA1} CC	-500	500	nA	$0\text{ V} \leq V_i \leq V_{DDP}$
Input high voltage	V_{IHA1} SR	$0.6 \times V_{DDP}$	$V_{DDP} + 0.3$	V	max. 3.6 V
Input low voltage	V_{ILA1} SR	-0.3	$0.36 \times V_{DDP}$	V	

Table 13 Standard_Pads Class_A1 (cont'd)

Parameter	Symbol	Values		Unit	Note / Test Condition
		Min.	Max.		
Output high voltage, POD[1)] = weak	V_{OHA1} CC	V_{DDP} - 0.4	–	V	$I_{OH} \geq$ -400 μA
		2.4	–	V	$I_{OH} \geq$ -500 μA
Output high voltage, POD[1)] = medium		V_{DDP} - 0.4	–	V	$I_{OH} \geq$ -1.4 mA
		2.4	–	V	$I_{OH} \geq$ -2 mA
Output low voltage	V_{OLA1} CC	–	0.4	V	$I_{OL} \leq$ 500 μA; POD[1)] = weak
		–	0.4	V	$I_{OL} \leq$ 2 mA; POD[1)] = medium
Fall time	t_{FA1} CC	–	150	ns	C_L = 20 pF; POD[1)] = weak
		–	50	ns	C_L = 50 pF; POD[1)] = medium
Rise time	t_{RA1} CC	–	150	ns	C_L = 20 pF; POD[1)] = weak
		–	50	ns	C_L = 50 pF; POD[1)] = medium

1) POD = Pin Out Driver

Table 14 Standard_Pads Class_A1+

Parameter	Symbol	Values		Unit	Note / Test Condition
		Min.	Max.		
Input leakage current	I_{OZA1+} CC	-1	1	μA	0 V $\leq V_i \leq V_{DDP}$
Input high voltage	V_{IHA1+} SR	0.6 × V_{DDP}	V_{DDP} + 0.3	V	max. 3.6 V
Input low voltage	V_{ILA1+} SR	-0.3	0.36 × V_{DDP}	V	
Output high voltage, POD[1)] = weak	V_{OHA1+} CC	V_{DDP} - 0.4	–	V	$I_{OH} \geq$ -400 μA
		2.4	–	V	$I_{OH} \geq$ -500 μA
Output high voltage, POD[1)] = medium		V_{DDP} - 0.4	–	V	$I_{OH} \geq$ -1.4 mA
		2.4	–	V	$I_{OH} \geq$ -2 mA
Output high voltage, POD[1)] = strong		V_{DDP} - 0.4	–	V	$I_{OH} \geq$ -1.4 mA
		2.4	–	V	$I_{OH} \geq$ -2 mA

Table 14 Standard_Pads Class_A1+ (cont'd)

Parameter	Symbol	Values		Unit	Note / Test Condition
		Min.	Max.		
Output low voltage	V_{OLA1+} CC	–	0.4	V	$I_{OL} \leq 500\ \mu A$; POD[1] = weak
		–	0.4	V	$I_{OL} \leq 2$ mA; POD[1] = medium
		–	0.4	V	$I_{OL} \leq 2$ mA; POD[1] = strong
Fall time	t_{FA1+} CC	–	150	ns	C_L = 20 pF; POD[1] = weak
		–	50	ns	C_L = 50 pF; POD[1] = medium
		–	28	ns	C_L = 50 pF; POD[1] = strong; edge = slow
		–	16	ns	C_L = 50 pF; POD[1] = strong; edge = soft;
Rise time	t_{RA1+} CC	–	150	ns	C_L = 20 pF; POD[1] = weak
		–	50	ns	C_L = 50 pF; POD[1] = medium
		–	28	ns	C_L = 50 pF; POD[1] = strong; edge = slow
		–	16	ns	C_L = 50 pF; POD[1] = strong; edge = soft

1) POD = Pin Out Driver

Table 15 Standard_Pads Class_A2

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.		Max.		
Input Leakage current	I_{OZA2} CC	-6		6	µA	0 V ≤ V_i < 0.5*V_{DDP} - 1 V; 0.5*V_{DDP} + 1 V <V_i ≤ V_{DDP}
		-3		3	µA	0.5*V_{DDP} - 1 V < V_i < 0.5*V_{DDP} + 1 V
Input high voltage	V_{IHA2} SR	0.6 × V_{DDP}		V_{DDP} + 0.3	V	max. 3.6 V
Input low voltage	V_{ILA2} SR	-0.3		0.36 × V_{DDP}	V	
Output high voltage, POD = weak	V_{OHA2} CC	V_{DDP} - 0.4		–	V	I_{OH} ≥ -400 µA
		2.4		–	V	I_{OH} ≥ -500 µA
Output high voltage, POD = medium		V_{DDP} - 0.4		–	V	I_{OH} ≥ -1.4 mA
		2.4		–	V	I_{OH} ≥ -2 mA
Output high voltage, POD = strong		V_{DDP} - 0.4		–	V	I_{OH} ≥ -1.4 mA
		2.4		–	V	I_{OH} ≥ -2 mA
Output low voltage, POD = weak	V_{OLA2} CC	–		0.4	V	I_{OL} ≤ 500 µA
Output low voltage, POD = medium		–		0.4	V	I_{OL} ≤ 2 mA
Output low voltage, POD = strong		–		0.4	V	I_{OL} ≤ 2 mA

Table 15 Standard_Pads Class_A2 (cont'd)

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.		Max.		
Fall time	t_{FA2} CC	–		150	ns	C_L = 20 pF; POD = weak
		–		50	ns	C_L = 50 pF; POD = medium
		–		3.7	ns	C_L = 50 pF; POD = strong; edge = sharp
		–		7	ns	C_L = 50 pF; POD = strong; edge = medium
		–		16	ns	C_L = 50 pF; POD = strong; edge = soft
Rise time	t_{RA2} CC	–		150	ns	C_L = 20 pF; POD = weak
		–		50	ns	C_L = 50 pF; POD = medium
		–		3.7	ns	C_L = 50 pF; POD = strong; edge = sharp
		–		7.0	ns	C_L = 50 pF; POD = strong; edge = medium
		–		16	ns	C_L = 50 pF; POD = strong; edge = soft

3.2.2 Analog to Digital Converters (ADCx)

Table 16 ADC Parameters (Operating Conditions apply)

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Analog reference voltage[5]	V_{AREF} SR	–	–	V_{DDA} + 0.05[1]	V	
Analog reference ground[5]	V_{AGND} SR	V_{SSM} - 0.05	–	V_{AREF} - 1	V	
Analog reference voltage range[2)5]	V_{AREF} - V_{AGND} SR	1	–	V_{DDA} + 0.1	V	
Analog input voltage	V_{AIN} SR	V_{AGND}	–	V_{DDA}	V	
Input leakage at analog inputs[3]	I_{OZ1} CC	-100	–	200	nA	$0.03 \times V_{DDA} < V_i < 0.97 \times V_{DDA}$;
		-500	–	100	nA	$0\ V \leq V_i \leq 0.03 \times V_{DDA}$;
		-100	–	500	nA	$0.97 \times V_{DDA} \leq V_i \leq V_{DDA}$;
Input leakage current at VAREF	I_{OZ2} CC	-1	–	1	µA	$0\ V \leq V_{AREF} \leq V_{DDA}$
Input leakage current at VAGND	I_{OZ3} CC	-1	–	1	µA	$0\ V \leq V_{AGND} \leq V_{DDA}$
Internal ADC clock	f_{ADCI} CC	1	–	30	MHz	V_{DDA} = 3.3 V
Switched capacitance at the analog voltage inputs[4]	C_{AINSW} CC	–	7	20	pF	
Total capacitance of an analog input	C_{AINTOT} CC	–	25	30	pF	
Switched capacitance at the positive reference voltage input[5)6]	C_{AREFSW} CC	–	15	30	pF	
Total capacitance of the voltage reference inputs[5]	$C_{AREFTOT}$ CC	–	20	40	pF	

Table 16 ADC Parameters (Operating Conditions apply) (cont'd)

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Total Unadjusted Error	TUE CC	-4	–	4	LSB	12-bit resolution; V_{DDA} = 3.3 V; $V_{AREF} = V_{DDA}$ 7)
Differential Non-Linearity Error8)	EA_{DNL} CC	-3	–	3	LSB	
Gain Error8)	EA_{GAIN} CC	-3.5	–	3.5	LSB	
Integral Non-Linearity8)	EA_{INL} CC	-3	–	3	LSB	
Offset Error8)	EA_{OFF} CC	-4	–	4	LSB	
Current through resistance for the ADC test (pull-down for AIN7)	I_{AIN7T} CC	–	15	tbd	mA	
Input current at VAREF input per module5)	I_{AREF} CC	–	–	75	µA	0 V ≤ V_{AREF} ≤ V_{DDA} 9) 10)
ON resistance of the analog input path	R_{AIN} CC	–	700	1 500	Ohm	V_{DDA} = 3.3 V
ON resistance for the ADC test (pull down for AIN7)	R_{AIN7T} CC	180	550	900	Ohm	
Resistance of the reference voltage input path	R_{AREF} CC	–	500	1 000	Ohm	

1) A running conversion may become imprecise in case the normal conditions are violated (voltage overshoot).

2) If the analog reference voltage is below V_{DDA}, then the ADC converter errors increase. If the reference voltage is reduced by the factor k (k<1), TUE, DNL, INL, Gain, and Offset errors increase also by the factor 1/k.

3) The leakage current definition is a continuous function, as shown in figure ADCx Analog Inputs Leakage. The numerical values defined determine the characteristic points of the given continuous linear approximation - they do not define step function.

4) The sampling capacity of the conversion C-network is pre-charged to $V_{AREF}/2$ before the sampling moment. Because of the parasitic elements, the voltage measured at AINx can deviate from $V_{AREF}/2$.

5) Applies to AINx, when used as auxiliary reference input.

6) This represents an equivalent switched capacitance. This capacitance is not switched to the reference voltage at once. Instead, smaller capacitances are successively switched to the reference voltage.

7) For 10-bit conversions, the errors are reduced to 1/4; for 8-bit conversions, the errors are reduced to 1/16.

8) The sum of DNL/INL/GAIN/OFF errors does not exceed the related total unadjusted error TUE.

9) I_{AREF_MAX} is valid for the minimum specified conversion time. The current flowing during an ADC conversion with a duration of up to t_c = 25 µs can be calculated with the formula $I_{AREF\_MAX} = Q_{CONV}/t_c$. Each conversion needs a total charge of Q_{CONV} = 150 pC from V_{AREF}.

10) All ADC conversions with a duration longer than t_c = 25 µs consume an I_{AREF_MAX} of 6 µA.

The power-up calibration of the ADC requires a maximum number of 4 352 f_{ADCI} cycles.

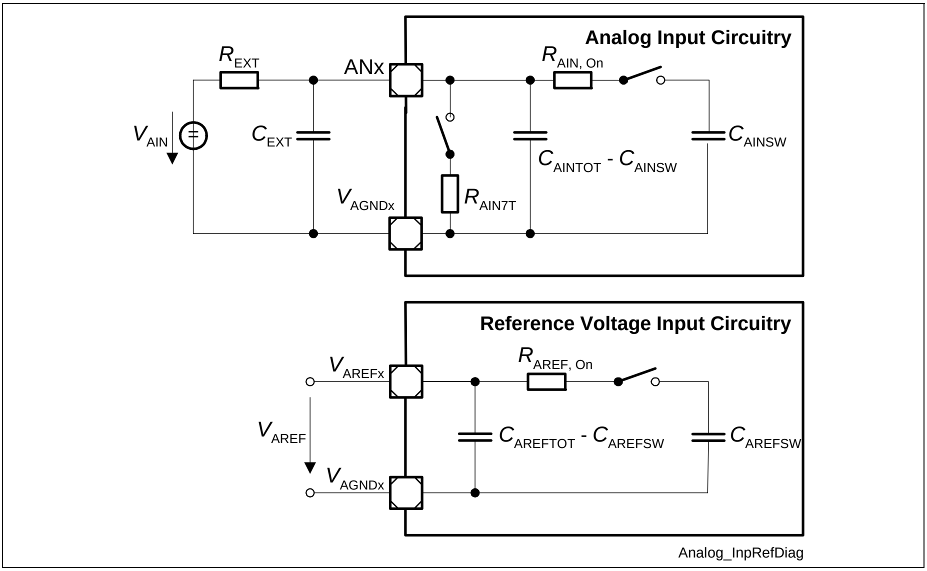


Figure 8 ADCx Input Circuits

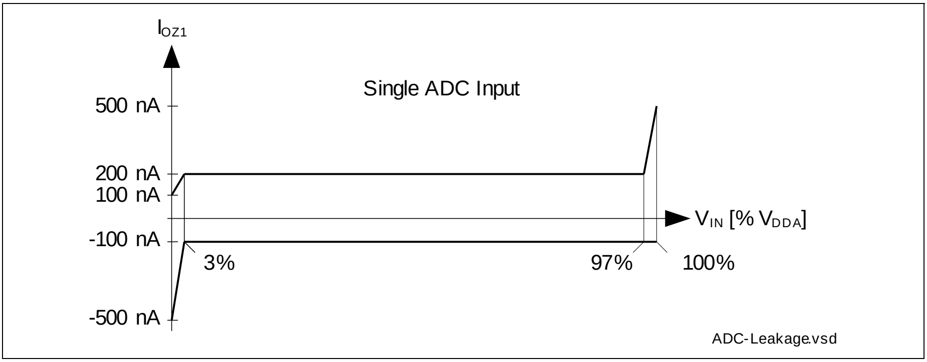


Figure 9 ADCx Analog Input Leakage Current

Conversion Time

Table 17 Conversion Time (Operating Conditions apply)

Parameter	Symbol		Values	Unit	Note
Conversion time	t_C	CC	$2 \times T_{ADC}$ + (2 + N + STC + PC +DM) $\times$ T_{ADCI}	µs	N = 8, 10, 12 for N-bit conversion $T_{ADC} = 1 / f_{PERIPH}$ $T_{ADCI} = 1 / f_{ADCI}$

- STC defines additional clock cycles to extend the sample time
- PC adds two cycles if post-calibration is enabled
- DM adds one cycle for an extended conversion time of the MSB

Conversion Time Examples

System assumptions:
f_{ADC} = 120 MHz i.e. t_{ADC} = 8.33 ns, DIVA = 3, f_{ADCI} = 30 MHz i.e. t_{ADCI} = 33.3 ns

According to the given formulas the following minimum conversion times can be achieved (STC = 0, DM = 0):

12-bit post-calibrated conversion (PC = 2):
$t_{CN12C} = (2 + 12 + 2) \times t_{ADCI} + 2 \times t_{ADC} = 16 \times 33.3$ ns $+ 2 \times 8.33$ ns = 550 ns

12-bit uncalibrated conversion:
$t_{CN12} = (2 + 12) \times t_{ADCI} + 2 \times t_{ADC} = 14 \times 33.3$ ns $+ 2 \times 8.33$ ns = 483 ns

10-bit uncalibrated conversion:
$t_{CN10} = (2 + 10) \times t_{ADCI} + 2 \times t_{ADC} = 12 \times 33.3$ ns $+ 2 \times 8.33$ ns = 417 ns

8-bit uncalibrated:
$t_{CN8} = (2 + 8) \times t_{ADCI} + 2 \times t_{ADC} = 10 \times 33.3$ ns $+ 2 \times 8.33$ ns = 350 ns

3.2.3 Digital to Analog Converters (DACx)

Note: These parameters are not subject to production test, but verified by design and/or characterization.

Table 18 DAC Parameters (Operating Conditions apply)

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
RMS supply current	I_{DD} CC	–	–	5	mA	without load currents of DAC outputs
Resolution	RES CC	–	12	–	Bit	
Update rate	f_{URATE_A} CC	–		2	Msample/s	data rate, where DAC can follow 64 LSB code jumps to ± 1LSB accuracy
Update rate	f_{URATE_F} CC	–		5	Msample/s	data rate, where DAC can follow 64 LSB code jumps to ± 4 LSB accuracy
Settling time	t_{SETTLE} CC	–	1	2	µs	at full scale jump, output voltage reaches target value ± 20 LSB
Slew rate	SR CC	2	5	–	V/µs	
Minimum output voltage	V_{OUT_MIN} CC	–	0.3	–	V	code value unsigned: 000_H; signed: 800_H
Maximum output voltage	V_{OUT_MAX} CC	–	2.5	–	V	code value unsigned: FFF_H; signed: $7FF_H$
Integral non-linearity	INL CC	–	–	±4	LSB	$R_L \geq 5$ kOhm, $C_L \leq 50$ pF
Differential non-linearity	DNL CC	–	–	±2	LSB	$R_L \geq 5$ kOhm, $C_L \leq 50$ pF
Offset error	ED_{OFF} CC		±20		mV	
Gain error	ED_{G_IN} CC	–	1.5	–	%	

Table 18 DAC Parameters (Operating Conditions apply) (cont'd)

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Startup time	$t_{STARTUP}$ CC	–	15	30	µs	time from output enabling till code valid ±16 LSB
3dB Bandwidth of Output Buffer	f_{C1} CC	2.5	5	–	MHz	verified by design
Output sourcing current	I_{OUT_SOURCE} CC	–	-30	–	mA	
Output sinking current	I_{OUT_SINK} CC	–	0.6	–	mA	
Output resistance	R_{OUT} CC	–	50	–	Ohm	
Load resistance	R_L SR	5	–	–	kOhm	
Load capacitance	C_L SR	–	–	50	pF	
Signal-to-Noise Ratio	*SNR* CC	–	70	–	dB	examination bandwidth < 25 kHz
Total Harmonic Distortion	*THD* CC	–	70	–	dB	examination bandwidth < 25 kHz
Power Supply Rejection Ratio	*PSRR* CC	–	56	–	dB	to V_{DDA} verified by design

3.2.4 Out-of-Range Comparator (ORC)

The Out-of-Range Comparator (ORC) triggers on analog input voltages (V_{AIN}) above the analog reference[1] (V_{AREF}) on selected input pins (GxORCy) and generates a service request trigger (GxORCOUTy).

Note: These parameters are not subject to production test, but verified by design and/or characterization.

The parameters in **Table 19** apply for the maximum reference voltage $V_{AREF} = V_{DDA} + 50$ mV.

Table 19 ORC Parameters (Operating Conditions apply)

Parameter	Symbol		Values			Unit	Note / Test Condition
			Min.	Typ.	Max.		
DC Switching Level	V_{ODC}	CC	100	125	200	mV	$V_{AIN} \geq V_{AREF} + V_{ODC}$
Hysteresis	V_{OHYS}	CC	50	–	V_{ODC}	mV	
Detection Delay of a persistent Overvoltage	t_{ODD}	CC	60	–	450	ns	$V_{AIN} \geq V_{AREF}$ + 200 mV
			45	–	100	ns	$V_{AIN} \geq V_{AREF}$ + 450 mV
Always detected Overvoltage Pulse	t_{OPDD}	CC	440	–	–	ns	$V_{AIN} \geq V_{AREF}$ + 200 mV
			85	–	–	ns	$V_{AIN} \geq V_{AREF}$ + 450 mV
Never detected Overvoltage Pulse	t_{OPDN}	CC	–	–	49	ns	$V_{AIN} \geq V_{AREF}$ + 200 mV
			–	–	25	ns	$V_{AIN} \geq V_{AREF}$ + 450 mV
Release Delay	t_{ORD}	CC	65	–	110	ns	$V_{AIN} \leq V_{AREF}$
Enable Delay	t_{OED}	CC	–	100	200	ns	

1) Always the standard VADC reference, alternate references do not apply to the ORC.

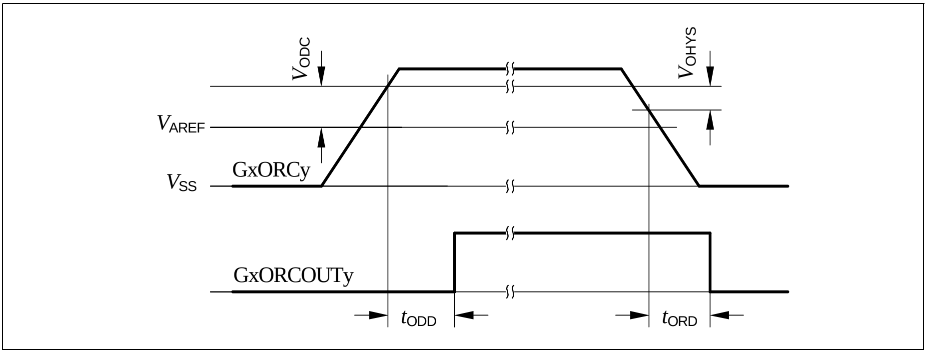


Figure 10 GxORCOUTy Trigger Generation

3.2.5 Die Temperature Sensor

The Die Temperature Sensor (DTS) measures the junction temperature T_J.

Note: These parameters are not subject to production test, but verified by design and/or characterization.

Table 20 Die Temperature Sensor Parameters

Parameter	Symbol		Values			Unit	Note / Test Condition
			Min.	Typ.	Max.		
Temperature sensor range	T_{SR}	SR	-40	–	150	°C	
Linearity Error (to the below defined formula)	ΔT_{LE}	CC	–	–	tbd	°C	
			–	±1	–	°C	0 °C ≤ T_J ≤ 80 °C
Offset Error	ΔT_{OE}	CC	–	tbd	tbd	°C	$\Delta T_{OE} = T_J - T_{DTS}$
Measurement time	t_M	CC	–	–	100	µs	
Start-up time after reset inactive	t_{TSST}	SR	–	–	20	µs	

The following formula calculates the temperature measured by the DTS in [°C] from the RESULT bit field of the DTSSTAT register.

Temperature T_{DTS} = (RESULT - 596) / 2.03 [°C] (*PRELIMINARY*)

This formula and the values defined in **Table 20** apply with the following calibration values:

- DTSCON.BGTRIM = 0_H (*PRELIMINARY*)
- DTSCON.REFTRIM = 4_H (*PRELIMINARY*)

3.2.6 USB OTG Interface DC Characteristics

The Universal Serial Bus (USB) Interface is compliant to the USB Rev. 2.0 Specification and the OTG Specification Rev. 1.3. High-Speed Mode is not supported.

Note: These parameters are not subject to production test, but verified by design and/or characterization.

Table 21 USB OTG VBUS Parameters (Operating Conditions apply)

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
VBUS input voltage range	V_{IN} CC	0.0	–	5.25	V	
A-device VBUS valid threshold	V_{B1} CC	4.4	–	–	V	
A-device session valid threshold	V_{B2} CC	0.8	–	2.0	V	
B-device session valid threshold	V_{B3} CC	0.8	–	4.0	V	
B-device session end threshold	V_{B4} CC	0.2	–	0.8	V	
VBUS input resistance to ground	R_{VBUS_IN} CC	40	–	100	kOhm	
B-device VBUS pull-up resistor	R_{VBUS_PU} CC	281	–	–	Ohm	Pull-up voltage = 3.0 V
B-device VBUS pull-down resistor	R_{VBUS_PD} CC	656	–	–	Ohm	
VBUS input current	I_{VBUS_IN} CC	–	–	150	µA	$0 V \leq V_{IN} \leq 5.25 V$: T_{AVG} = 1 ms

Table 22 USB OTG Data Line (USB_DP, USB_DN) Parameters (Operating Conditions apply)

Parameter	Symbol		Values			Unit	Note / Test Condition
			Min.	Typ.	Max.		
Input low voltage	V_{IL}	SR	–	–	0.8	V	
Input high voltage (driven)	V_{IH}	SR	2.0	–	–	V	
Input high voltage (floating) 1)	V_{IHZ}	SR	2.7	–	3.6	V	
Differential input sensitivity	V_{DIS}	CC	0.2	–	–	V	
Differential common mode range	V_{CM}	CC	0.8	–	2.5	V	
Output low voltage	V_{OL}	CC	0.0	–	0.3	V	1.5 kOhm pull-up to 3.6 V
Output high voltage	V_{OH}	CC	2.8	–	3.6	V	15 kOhm pull-down to 0 V
DP pull-up resistor (idle bus)	R_{PUI}	CC	900	–	1 575	Ohm	
DN pull-up resistor (upstream port receiving)	R_{PUA}	CC	1 425	–	3 090	Ohm	
DP, DN pull-down resistor	R_{PD}	CC	14.25	–	24.8	kOhm	
Input impedance DP, DN	Z_{INP}	CC	300	–	–	kOhm	$0\ V \leq V_{IN} \leq V_{DDP}$
Driver output resistance DP, DN	Z_{DRV}	CC	28	–	44	Ohm	

1) Measured at A-connector with 1.5 kOhm ± 5% to 3.3 V ± 0.3 V connected to USB_DP or USB_DN and at B-connector with 15 kOhm ± 5% to ground connected to USB_DP and USB_DN.

3.2.7 Oscillator Pins

Note: It is strongly recommended to measure the oscillation allowance (negative resistance) in the final target system (layout) to determine the optimal parameters for the oscillator operation. Please refer to the limits specified by the crystal or ceramic resonator supplier.

Table 23 OSC_XTAL Parameters

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Input current at XTAL1	I_{IX1} CC	-25	–	25	µA	0 V < V_{IN} < V_{DDP}
Input frequency	f_{OSC} SR	4	–	40	MHz	Direct Input Mode selected
		4	–	25	MHz	External Crystal Mode selected
Oscillator start-up time[1)]	t_{OSCS} CC	–	–	10	ms	
Input high voltage at XTAL1[2)]	V_{IHX} SR	0.7 × $V_{DDOS C3}$	–	V_{DDP} + 0.2	V	
Input low voltage at XTAL1	V_{ILX} SR	-0.2	–	0.3 × V_{DDP}	V	

1) t_{OSCS} is defined from the moment when V_{DDP} = 3.13 V until the oscillations reach an amplitude at XTAL1 of 0.3 * V_{DDP}. The external oscillator circuitry must be optimized by the customer and checked for negative resistance as recommended and specified by crystal suppliers.

2) When the XTAL1 pin is driven by a crystal, reaching a minimum amplitude (peak-to-peak) of 0.4 * V_{DDP} is necessary.

Table 24 RTC_XTAL Parameters

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Input current at RTC_XTAL1	I_{IX1} CC	tbd	–	tbd	µA	0 V < V_{IN} < V_{DDP}
Input frequency	f_{OSC} SR	–	32.768	–	kHz	
Oscillator start-up time[1)]	t_{OSCS} CC	–	–	5	s	
Input high voltage at RTC_XTAL1[2)]	V_{IHX} SR	0.6	–	V_{BAT} + 0.3	V	
Input low voltage at RTC_XTAL1	V_{ILX} SR	-0.3	–	0.2	V	

1) t_{OSCS} is defined from the moment when V_{BAT} = 3.13 V until the oscillations reach an amplitude at RTC_XTAL1 of 0.3 * V_{BAT}. The external oscillator circuitry must be optimized by the customer and checked for negative resistance as recommended and specified by crystal suppliers.

2) When the RTC_XTAL1 pin is driven by a crystal, reaching a minimum amplitude (peak-to-peak) of 0.4 * V_{BAT} is necessary.

3.2.8 Power Supply Current

The total power supply current defined below consists of a leakage and a switching component.

Application relevant values are typically lower than those given in the following tables, and depend on the customer's system operating conditions (e.g. thermal connection or used application configurations).

If not stated otherwise, the operating conditions for the parameters in the following table are:
V_{DDP} = 3.3 V, T_A = 25 °C

Table 25 Power Supply Parameters

Parameter	Symbol		Values			Unit	Note / Test Condition
			Min.	Typ.	Max.		
Active supply current[1)] Peripherals enabled Frequency: f_{CPU} / f_{PERIPH} / f_{CCU} in MHz	I_{DDPA}	CC	–	120	–	mA	120 / 120 / 120
			–	tbd	–		120 / 60 / 60
			–	tbd	–		60 / 60 / 120
			–	tbd	–		24 / 24 / 24
			–	tbd	–		1 / 1 / 1
Active supply current[2)] Peripherals disabled Frequency: f_{CPU} / f_{PERIPH} / f_{CCU} in MHz	I_{DDPA}	CC	–	tbd	–	mA	120 / 120 / 120
			–	tbd	–		120 / 60 / 60
			–	tbd	–		60 / 60 / 120
			–	tbd	–		24 / 24 / 24
			–	tbd	–		1 / 1 / 1
Sleep supply current[3)] Peripherals enabled Frequency: f_{CPU} / f_{PERIPH} / f_{CCU} in MHz	I_{DDPS}	CC	–	tbd	–	mA	120 / 120 / 120
			–	tbd	–		120 / 60 / 60
			–	tbd	–		60 / 60 / 120
			–	tbd	–		24 / 24 / 24
			–	tbd	–		1 / 1 / 1
f_{CPU} / f_{PERIPH} / f_{CCU} in kHz			–	tbd	–		100 / 100 / 100

Table 25 Power Supply Parameters (cont'd)

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Sleep supply current[4)] Peripherals disabled Frequency: f_{CPU} / f_{PERIPH} / f_{CCU} in MHz	I_{DDPS} CC	–	tbd	–	mA	120 / 120 / 120
		–	tbd	–		120 / 60 / 60
		–	tbd	–		60 / 60 / 120
		–	tbd	–		24 / 24 / 24
		–	tbd	–		1 / 1 / 1
f_{CPU} / f_{PERIPH} / f_{CCU} in kHz		–	tbd	–		100 / 100 / 100
Deep Sleep supply current[5)] Flash in Sleep mode Frequency: f_{CPU} / f_{PERIPH} / f_{CCU} in MHz	I_{DDPD} CC	–	15	–	mA	24 / 24 / 24
		–	tbd	–		4 / 4 / 4
		–	tbd	–		1 / 1 / 1
f_{CPU} / f_{PERIPH} / f_{CCU} in kHz		–	tbd	–		100 / 100 / 100 [6)]
Hibernate supply current RTC on[7)]	I_{DDPH} CC	–	10	–	µA	V_{BAT} = 3.3 V
		–	tbd	–		V_{BAT} = 2.4 V
		–	tbd	–		V_{BAT} = 2.0 V
Hibernate supply current RTC off[8)]	I_{DDPH} CC	–	tbd	–	µA	V_{BAT} = 3.3 V
		–	tbd	–		V_{BAT} = 2.4 V
		–	tbd	–		V_{BAT} = 2.0 V
Hibernate off[9)]	I_{DDPH} CC	–	tbd	–	µA	V_{BAT} = 3.3 V
		–	tbd	–		V_{BAT} = 2.4 V
		–	tbd	–		V_{BAT} = 2.0 V
Worst case active supply current[10)]	I_{DDPA} CC	–	–	tbd[11)]	mA	V_{DDP} = 3.6 V, T_J = 150 °C
V_{DDA} power supply current	I_{DDA} CC	–	–	tbd	mA	V_{DDP} = 3.6 V, T_J = 150 °C
Pad current relevant for thermal calculation, no pad activity	I_{DDP} CC	–	–	tbd	mA	V_{DDP} = 3.6 V, T_J = 150 °C
I_{DDP} current at $\overline{\text{PORST}}$ Low	I_{DDP_PORST} CC	–	–	tbd	mA	V_{DDP} = 3.6 V, T_J = 150 °C

Table 25 Power Supply Parameters (cont'd)

Parameter	Symbol		Values			Unit	Note / Test Condition
			Min.	Typ.	Max.		
Power Dissipation	P_{DISS}	CC	–	–	tbd	W	V_{DDP} = 3.6 V, T_J = 150 °C
Wake-up time from Sleep to Active mode	t_{SSA}	CC	–	tbd	–	cycles	
Wake-up time from Deep Sleep to Active mode			–	–	–	ms	Defined by the wake-up of the Flash module, see **Chapter 3.2.9**
Wake-up time from Hibernate mode			–	–	–	ms	Wake-up via power-on reset event, see **Chapter 3.3.2**

1) CPU executing code from Flash, all peripherals idle.
2) CPU executing code from Flash.
3) CPU in sleep, all peripherals idle, Flash in Active mode.
4) CPU in sleep, Flash in Active mode.
5) CPU in sleep, peripherals disabled, after wake-up code execution from RAM.
6) To wake-up the Flash from its Sleep mode, $f_{CPU} \geq 1$ MHz is required.
7) OSC_ULP operating with external crystal on RTC_XTAL
8) OSC_ULP off, Hibernate domain operating with OSC_SI clock
9) V_{BAT} supplied, but Hibernate domain not started; for example state after factory assembly
10) Test Power Loop: f_{SYS} = 120 MHz, CPU and tbd modules running, all peripherals active. The power consumption of each customer application will most probably be lower than this value, but must be evaluated separately.
11) I_{DDP} decreases typically by tbd mA when f_{SYS} decreases by 50 MHz, at constant T_J

3.2.9 Flash Memory Parameters

Note: These parameters are not subject to production test, but verified by design and/or characterization.

Table 26 Flash Memory Parameters

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Erase Time per 256 Kbyte Sector	t_{ERP} CC	–	–	5	s	
Erase Time per 64 Kbyte Sector	t_{ERP} CC	–	–	1.2	s	
Program time per page[1]	t_{PRP} CC	–	5.5	11	ms	
Erase suspend delay	t_{FL_ErSusp} CC	–	–	15	ms	
Wait time after margin change	$t_{FL\_MarginDel}$ CC	10	–	–	µs	
Wake-up time	t_{WU} CC	–	–	270	µs	
Read access time	t_a CC	22	–	–	ns	For operation with $1 / f_{CPU} < t_a$ wait states must be configured[2]
Data Retention Time, Physical Sector[3)4)]	t_{RET} CC	20	–	–	years	Max. 1000 erase/program cycles
Data Retention Time, Logical Sector[3)4)]	t_{RETL} CC	20	–	–	years	Max. 100 erase/program cycles
Data Retention Time, User Configuration Block (UCB)[3)4)]	t_{RTU} CC	20	–	–	years	Max. 4 erase/program cycles per UCB

1) In case the Program Verify feature detects weak bits, these bits will be programmed once more. The reprogramming takes an additional time of 5.5 ms.

2) The following formula applies to the wait state configuration: FCON.WSPFLASH $\times$ $(1 / f_{CPU}) \geq t_a$.

3) Storage and inactive time included.

4) Values given are valid for an average weighted junction temperature of T_J = 110°C. Further lifetime dependency values are give in the Quality Declarations.

3.3 AC Parameters

3.3.1 Testing Waveforms

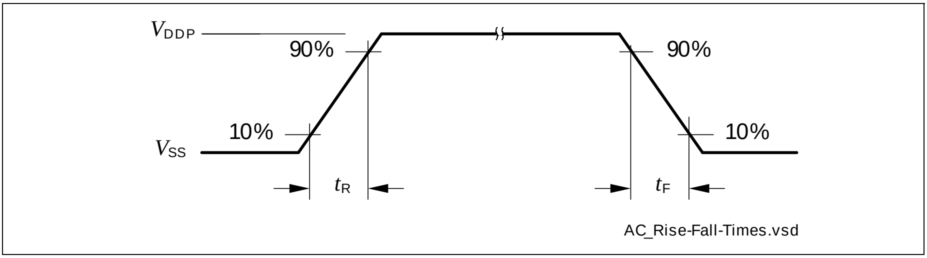


Figure 11 Rise/Fall Time Parameters

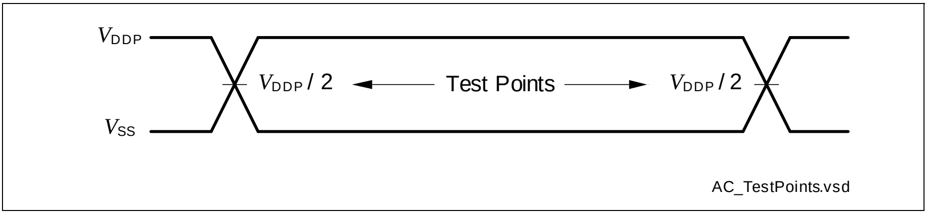


Figure 12 Testing Waveform, Output Delay

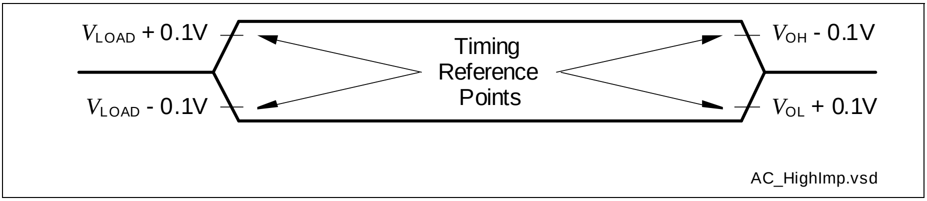


Figure 13 Testing Waveform, Output High Impedance

3.3.2 Power-Up and Supply Monitoring

$\overline{\text{PORST}}$ is always asserted when V_{DDP} and/or V_{DDC} violate the respective thresholds.

Table 27 Supply Monitoring Parameters

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Digital supply voltage reset threshold	V_{POR} CC	2.79[1]	2.95	3.05[2]	V	
Core supply voltage reset threshold	V_{PV} CC	–	–	1.17	V	
V_{DDP} voltage to ensure defined pad states	V_{DDPPA} CC	–	1.0	–	V	
Startup time from power-on reset with code execution from Flash	t_{SSW} CC	–	2.5	3.5	ms	Time to the first user code instruction
V_{DDC} ramp up time	t_{VCR} CC	–	550	–	µs	Ramp up after power-on or after a reset triggered by a violation of V_{POR} or V_{PV}

1) Minimum threshold for reset assertion.

2) Maximum threshold for reset deassertion.

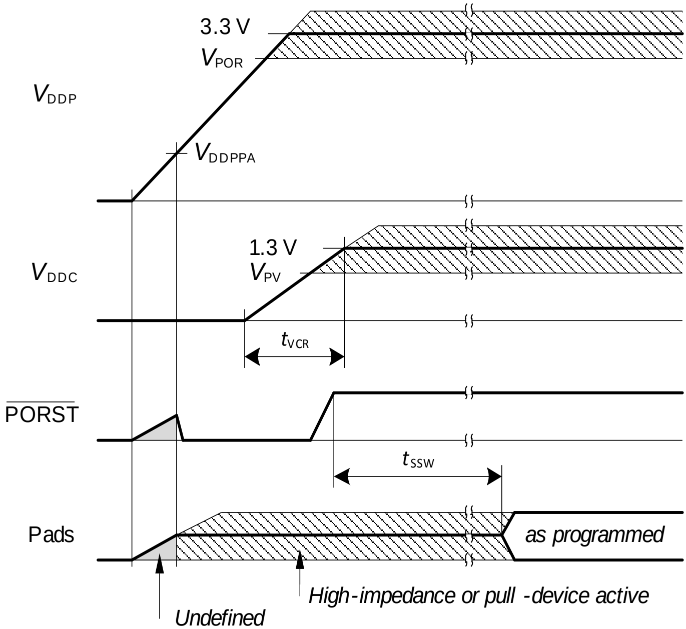


Figure 14 Power-Up Behavior

3.3.3 Power Sequencing

While starting up and shutting down as well as when switching power modes of the system it is important to limit the current load steps. A typical cause for such load steps is changing the CPU frequency f_{CPU}. Load steps exceeding the below defined values may cause a power on reset triggered by the supply monitor.

Note: These parameters are not subject to production test, but verified by design and/or characterization.

Table 28 Power Sequencing Parameters

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Positive Load Step Current	ΔI_{PLS} SR	-	–	50	mA	Load increase on V_{DDP} $\Delta t \leq 10$ ns
Negative Load Step Current	ΔI_{NLS} SR	-	–	150	mA	Load decrease on V_{DDP} $\Delta t \leq 10$ ns
V_{DDC} Voltage Over- / Undershoot from Load Step	ΔV_{LS} CC	-	–	±100	mV	For maximum positive or negative load step
Positive Load Step Settling Time	t_{PLSS} SR	50	–	-	µs	
Negative Load Step Settling Time	t_{NLSS} SR	100	–	-	µs	
External Buffer Capacitor on V_{DDC}	C_{EXT} SR	-	6.8	-	µF	In addition C = 100 nF capacitor on each V_{DDC} pin

Positive Load Step Examples

System assumptions:
$f_{CPU} = f_{SYS}$, target frequency f_{CPU} = 120 MHz, main PLL f_{VCO} = 480 MHz, stepping done py K2 divider, t_{PLSS} between individual steps:

24 MHz - 48 MHz - 68 MHz - 96 MHz - 120 MHz (K2 steps 20 - 10 - 7 - 5 - 4)
24 MHz - 68 MHz - 96 MHz - 120 MHz (K2 steps 20 - 7 - 5 - 4)
24 MHz - 68 MHz - 120 MHz (K2 steps 20 - 7 - 4)

3.3.4 Phase Locked Loop (PLL) Characteristics

Main and USB PLL

Table 29 PLL Parameters

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Accumulated Jitter	D_P CC	–	–	±tbd	ns	accumulated over 300 cycles
Cycle-to-Cycle Jitter	D_C CC	–	–	±tbd	ps	
PLL base frequency	$f_{PLLBASE}$ CC	60	–	140	MHz	
VCO input frequency	f_{REF} CC	4	–	16	MHz	
VCO frequency range	f_{VCO} CC	260	–	520	MHz	
PLL lock-in time	t_L CC	–	–	400	µs	

3.3.5 Internal Clock Source Characteristics

Fast Internal Clock Source

Table 30 Fast Internal Clock Parameters

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Nominal frequency	f_{OFINC} CC	–	32.5	–	MHz	not calibrated
		–	24	–	MHz	calibrated
Accuracy	Δf_{OFI} CC	–	–	±30	%	no calibration
		–	–	±1	%	automatic calibration
Accumulated Jitter	D_P CC	–	–	±tbd	ns	
Start-up time	t_{OFIS} CC	–	50	–	µs	

Slow Internal Clock Source

Table 31 Slow Internal Clock Parameters

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Nominal frequency	f_{OSI} CC	–	32.768	–	kHz	
Accuracy	Δf_{OSI} CC	–	–	±1.5	%	V_{BAT} = const.
		–	–	±3	%	1.8 V < V_{BAT} < 3.6 V
Start-up time	t_{OSIS} CC	–	50	–	µs	

3.3.6 JTAG Interface Timing

The following parameters are applicable for communication through the JTAG debug interface. The JTAG module is fully compliant with IEEE1149.1-2000.

Note: These parameters are not subject to production test, but verified by design and/or characterization.

Note: Operating conditions apply.

Table 32 JTAG Interface Timing Parameters

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
TCK clock period	t_1 SR	25	–	–	ns	
TCK high time	t_2 SR	10	–	–	ns	
TCK low time	t_3 SR	10	–	–	ns	
TCK clock rise time	t_4 SR	–	–	4	ns	
TCK clock fall time	t_5 SR	–	–	4	ns	
TDI/TMS setup to TCK rising edge	t_6 SR	6	–	–	ns	
TDI/TMS hold after TCK rising edge	t_7 SR	6	–	–	ns	
TDO valid after TCK falling edge[1] (propagation delay)	t_8 CC	–	–	13	ns	C_L = 50 pF
	t_8 CC	3	–	–	ns	C_L = 20 pF
TDO hold after TCK falling edge[1]	t_{18} CC	2	–	–	ns	
TDO high imped. to valid from TCK falling edge[1)2)]	t_9 CC	–	–	14	ns	C_L = 50 pF
TDO valid to high imped. from TCK falling edge[1]	t_{10} CC	–	–	13.5	ns	C_L = 50 pF

1) The falling edge on TCK is used to generate the TDO timing.

2) The setup time for TDO is given implicitly by the TCK cycle time.

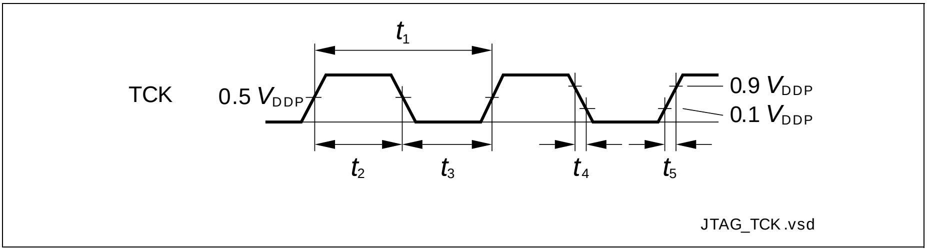


Figure 15 Test Clock Timing (TCK)

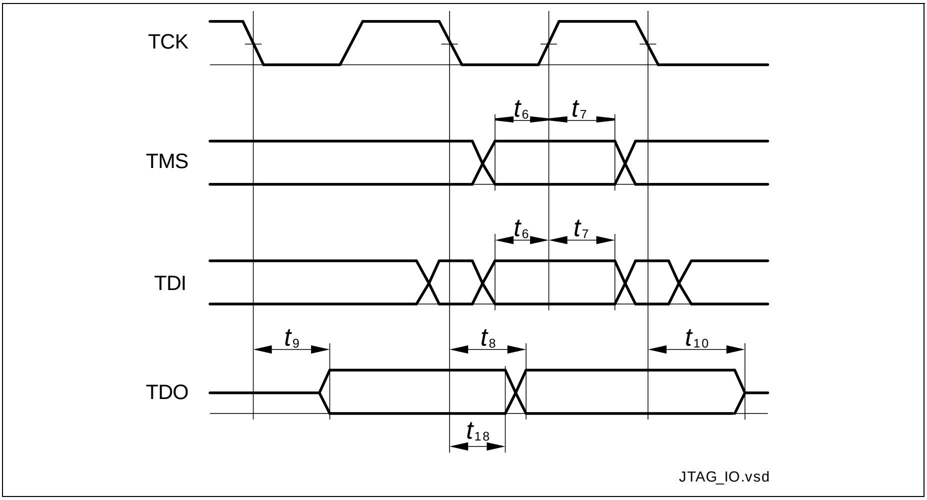


Figure 16 JTAG Timing

3.3.7 Serial Wire Debug Port (SW-DP) Timing

The following parameters are applicable for communication through the SW-DP interface.

Note: These parameters are not subject to production test, but verified by design and/or characterization.

Note: Operating conditions apply.

Table 33 SWD Interface Timing Parameters(Operating Conditions apply)

Parameter	Symbol		Values			Unit	Note / Test Condition
			Min.	Typ.	Max.		
SWDCLK clock period	t_{SC}	SR	25	–	–	ns	
SWDCLK high time	t_1	SR	10	–	500000	ns	
SWDCLK low time	t_2	SR	10	–	500000	ns	
SWDIO input setup to SWDCLK rising edge	t_3	SR	4	–	–	ns	
SWDIO input hold after SWDCLK rising edge	t_4	SR	1	–	–	ns	
SWDIO output skew after SWDCLK falling edge[1)] (propagation delay)	t_5	CC	-5	–	5	ns	

1) The falling edge on SWDCLK is used to generate the SWDIO output timing.

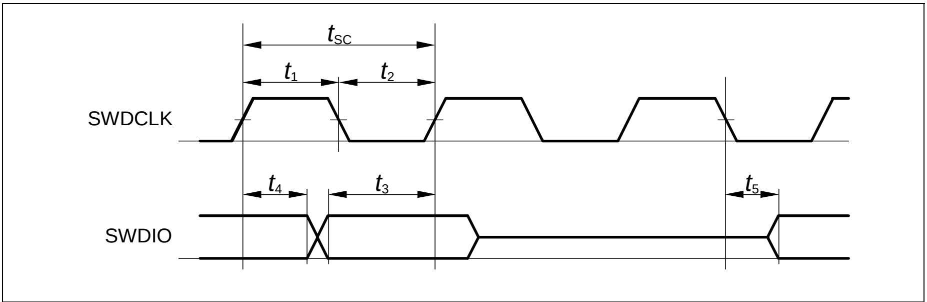


Figure 17 SWD Timing

3.3.8 Embedded Trace Macro Cell (ETM) Timing

The Data timings are to the active clock edge, in half-rate clocking mode that is the rising and falling clock edge.

Note: These parameters are not subject to production test, but verified by design and/or characterization.

Note: Operating conditions apply, with $C_L \leq 15$ pF.

Table 34 ETM Interface Timing Parameters

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
TRACECLK period	t_1 CC	16.7	–	–	ns	–
TRACECLK high time	t_2 CC	2	–	–	ns	–
TRACECLK low time	t_3 CC	2	–	–	ns	–
TRACECLK and TRACEDATA rise time	t_4 CC	–	–	3	ns	–
TRACECLK and TRACEDATA fall time	t_5 CC	–	–	3	ns	–
TRACEDATA output setup time	t_6 CC	3	–	–	ns	–
TRACEDATA output hold time	t_7 CC	2	–	–	ns	–

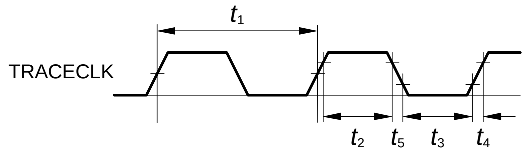


Figure 18 ETM Clock Timing

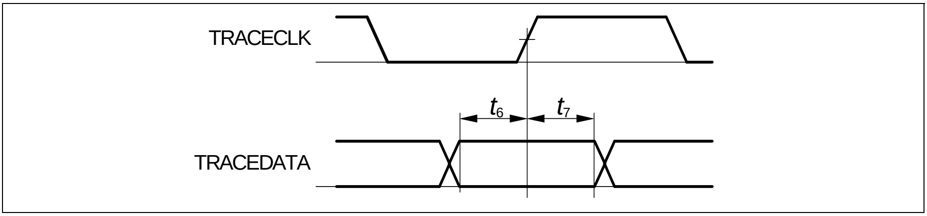


Figure 19 ETM Data Timing

3.3.9 Peripheral Timings

Note: These parameters are not subject to production test, but verified by design and/or characterization.

Note: Operating conditions apply.

3.3.9.1 Delta-Sigma Demodulator Digital Interface Timing

The following parameters are applicable for the digital interface of the Delta-Sigma Demodulator (DSD).
Data timings are to the active clock edge. Depending on the operation mode of the connected modulator that can be the rising and falling clock edge.

Note: These parameters are not subject to production test, but verified by design and/or characterization.

Table 35 DSD Interface Timing Parameters

Parameter	Symbol		Values			Unit	Note / Test Condition
			Min.	Typ.	Max.		
MCLK period in master mode	t_1	CC	tbd	–	–	ns	
MCLK high time in master mode	t_2	CC	tbd	–	–	ns	
MCLK low time in master mode	t_3	CC	tbd	–	–	ns	
MCLK period in slave mode	t_1	SR	tbd	–	–	ns	$t_1 \geq 2 \times 1 / f_{PERIPH}$
MCLK high time in slave mode	t_2	SR	tbd	–	–	ns	
MCLK low time in slave mode	t_3	SR	tbd	–	–	ns	
DIN input setup time to the active clock edge	t_4	SR	tbd	–	–	ns	
DIN input hold time to the active clock edge	t_5	SR	tbd	–	–	ns	

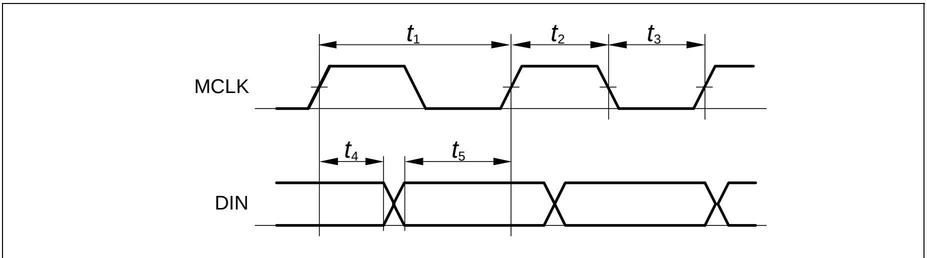


Figure 20 DSD Data Timing

3.3.9.2 Synchronous Serial Interface (USIC SSC) Timing

The following parameters are applicable for a USIC channel operated in SSC mode.

Note: Operating Conditions apply.

Table 36 USIC SSC Master Mode Timing

Parameter	Symbol		Values			Unit	Note / Test Condition
			Min.	Typ.	Max.		
SCLKOUT master clock period	t_{CLK}	CC	33.3	–	–	ns	
Slave select output SELO active to first SCLKOUT transmit edge	t_1	CC	t_{SYS} - 6.5[1]	–	–	ns	
Slave select output SELO inactive after last SCLKOUT receive edge	t_2	CC	t_{SYS} - 8.5[1]	–	–	ns	
Data output DOUT[3:0] valid time	t_3	CC	-6	–	8	ns	
Receive data input DX0/DX[5:3] setup time to SCLKOUT receive edge	t_4	SR	23	–	–	ns	
Data input DX0/DX[5:3] hold time from SCLKOUT receive edge	t_5	SR	1	–	–	ns	

1) $t_{SYS} = 1 / f_{PB}$

Table 37 USIC SSC Slave Mode Timing

Parameter	Symbol		Values			Unit	Note / Test Condition
			Min.	Typ.	Max.		
DX1 slave clock period	t_{CLK}	SR	66.6	–	–	ns	
Select input DX2 setup to first clock input DX1 transmit edge[1]	t_{10}	SR	3	–	–	ns	
Select input DX2 hold after last clock input DX1 receive edge[1]	t_{11}	SR	4	–	–	ns	
Receive data input DX0/DX[5:3] setup time to shift clock receive edge[1]	t_{12}	SR	6	–	–	ns	
Data input DX0/DX[5:3] hold time from clock input DX1 receive edge[1]	t_{13}	SR	4	–	–	ns	
Data output DOUT[3:0] valid time	t_{14}	CC	0	–	24	ns	

1) These input timings are valid for asynchronous input signal handling of slave select input, shift clock input, and receive data input (bits DXnCR.DSEN = 0).

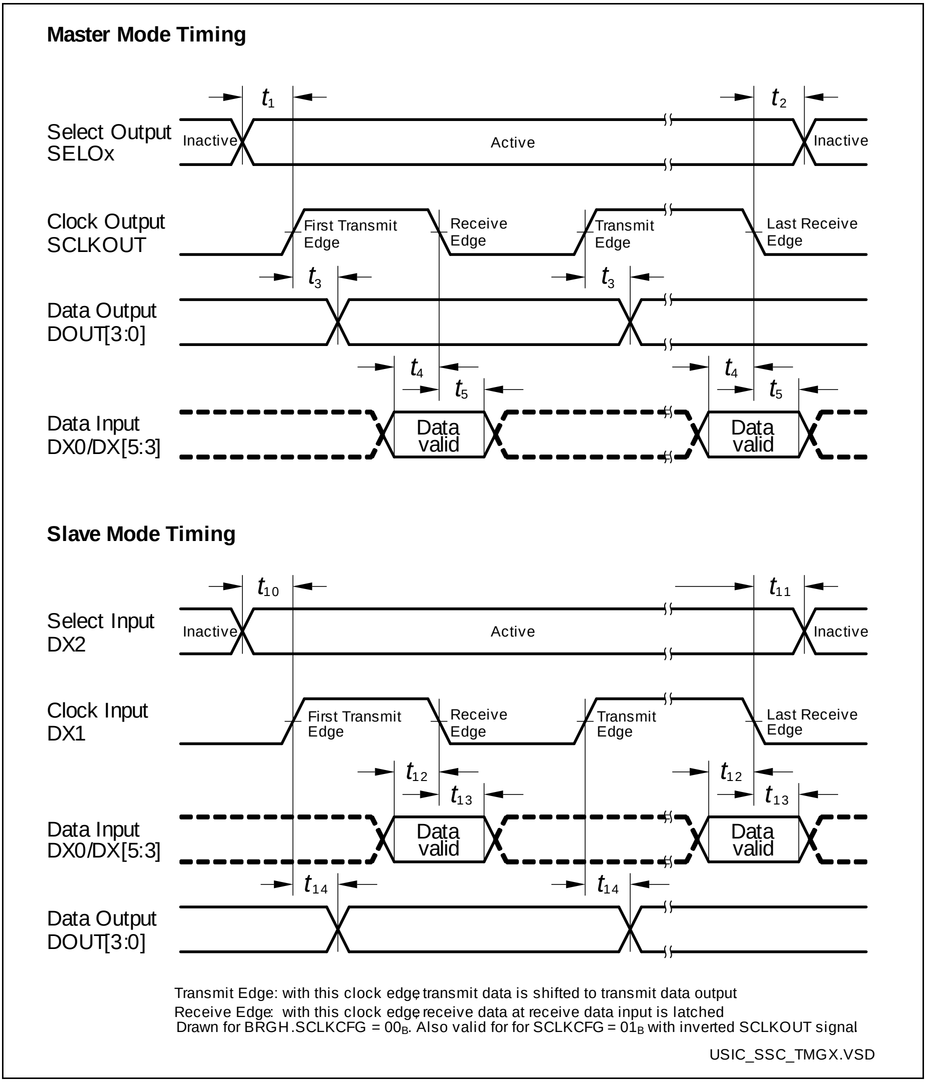


Figure 21 USIC - SSC Master/Slave Mode Timing

Note: This timing diagram shows a standard configuration, for which the slave select signal is low-active, and the serial clock signal is not shifted and not inverted.

3.3.9.3 Inter-IC (IIC) Interface Timing

The following parameters are applicable for a USIC channel operated in IIC mode.

Note: Operating Conditions apply.

Table 38 USIC IIC Standard Mode Timing[1)]

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Fall time of both SDA and SCL	t_1 CC/SR	-	-	300	ns	
Rise time of both SDA and SCL	t_2 CC/SR	-	-	1000	ns	
Data hold time	t_3 CC/SR	0	-	-	µs	
Data set-up time	t_4 CC/SR	250	-	-	ns	
LOW period of SCL clock	t_5 CC/SR	4.7	-	-	µs	
HIGH period of SCL clock	t_6 CC/SR	4.0	-	-	µs	
Hold time for (repeated) START condition	t_7 CC/SR	4.0	-	-	µs	
Set-up time for repeated START condition	t_8 CC/SR	4.7	-	-	µs	
Set-up time for STOP condition	t_9 CC/SR	4.0	-	-	µs	
Bus free time between a STOP and START condition	t_{10} CC/SR	4.7	-	-	µs	
Capacitive load for each bus line	C_b SR	-	-	400	pF	

1) All parameters are measured with a pull-up resistor of 4.7 kOhms at each of the SCL and SDA line.

Table 39 USIC IIC Fast Mode Timing[1)]

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Fall time of both SDA and SCL	t_1 CC/SR	20 + 0.1*C_b [2)]	-	300	ns	
Rise time of both SDA and SCL	t_2 CC/SR	20 + 0.1*C_b [2)]	-	300	ns	
Data hold time	t_3 CC/SR	0	-	-	µs	
Data set-up time	t_4 CC/SR	100	-	-	ns	
LOW period of SCL clock	t_5 CC/SR	1.3	-	-	µs	
HIGH period of SCL clock	t_6 CC/SR	0.6	-	-	µs	
Hold time for (repeated) START condition	t_7 CC/SR	0.6	-	-	µs	
Set-up time for repeated START condition	t_8 CC/SR	0.6	-	-	µs	
Set-up time for STOP condition	t_9 CC/SR	0.6	-	-	µs	
Bus free time between a STOP and START condition	t_{10} CC/SR	1.3	-	-	µs	
Capacitive load for each bus line	C_b SR	-	-	400	pF	

1) All parameters are measured with a pull-up resistor of 4.7 kOhms at each of the SCL and SDA line.

2) C_b refers to the total capacitance of one bus line in pF.

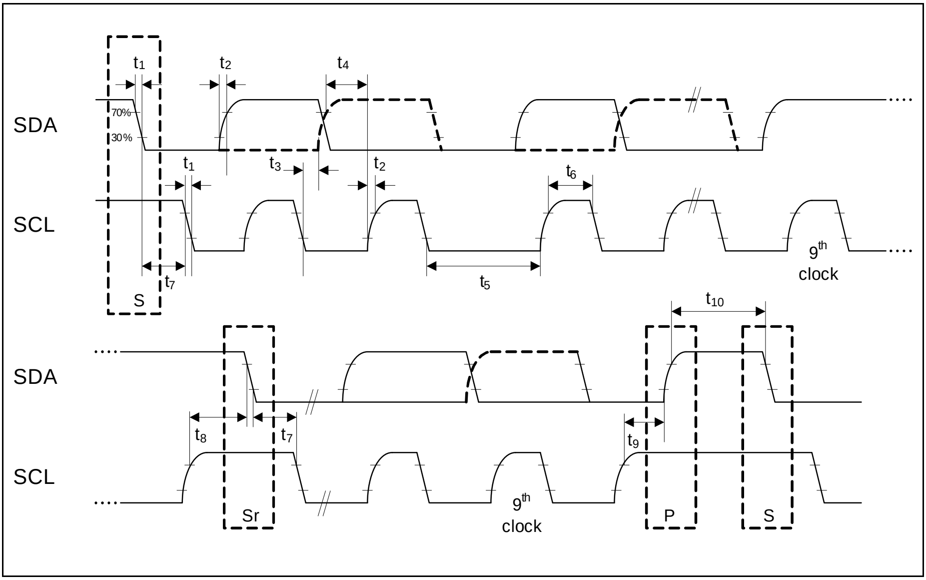


Figure 22 USIC IIC Stand and Fast Mode Timing

3.3.9.4 Inter-IC Sound (IIS) Interface Timing

The following parameters are applicable for a USIC channel operated in IIS mode.

Note: Operating Conditions apply.

Table 40 USIC IIS Master Transmitter Timing

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Clock period	t_1 CC	33.3	–	–	ns	
Clock HIGH	t_2 CC	0.35 x t_{1min}	–	–	ns	
Clock Low	t_3 CC	0.35 x t_{1min}	–	–	ns	
Hold time	t_4 CC	0	–	–	ns	
Clock rise time	t_5 CC	–	–	0.15 x t_{1min}	ns	

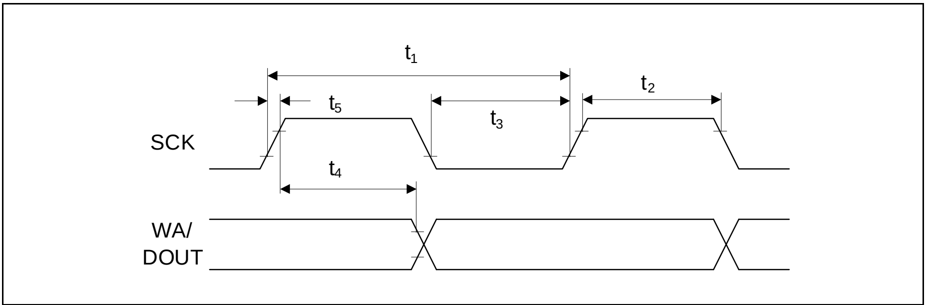


Figure 23 USIC IIS Master Transmitter Timing

Table 41 USIC IIS Slave Receiver Timing

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Clock period	t_6 SR	66.6	–	–	ns	
Clock HIGH	t_7 SR	0.35 x t_{6min}	–	–	ns	
Clock Low	t_8 SR	0.35 x t_{6min}	–	–	ns	
Set-up time	t_9 SR	0.2 x t_{6min}	–	–	ns	
Hold time	t_{10} SR	0	–	–	ns	

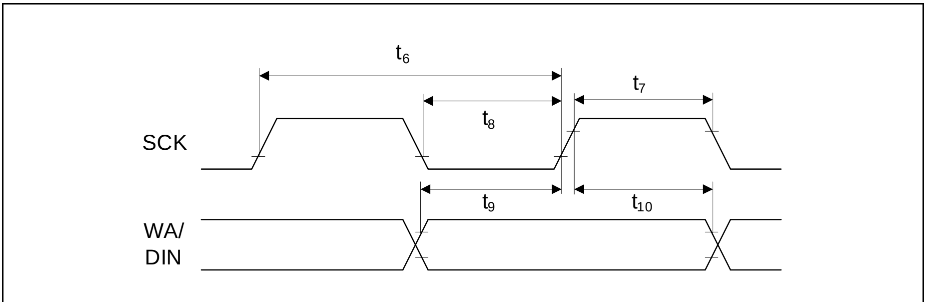


Figure 24 USIC IIS Slave Receiver Timing

3.3.9.5 SDMMC Interface Timing

Note: Operating Conditions apply, total external capacitive load C_L = 40 pF.

AC Timing Specifications (Full-Speed Mode)

Table 42 SDMMC Timing for Full-Speed Mode

Parameter	Symbol		Values		Unit	Note/ Test Condition
			Min.	Max.		
Clock frequency in full speed transfer mode ($1/t_{pp}$)	f_{pp}	CC	0	24	MHz	
Clock cycle in full speed transfer mode	t_{pp}	CC	40	–	ns	
Clock low time	t_{WL}	CC	10	–	ns	
Clock high time	t_{WH}	CC	10	–	ns	
Clock rise time	t_{TLH}	CC	–	10	ns	
Clock fall time	t_{THL}	CC	–	10	ns	
Inputs setup to clock rising edge	t_{ISU_F}	SR	2	–	ns	
Inputs hold after clock rising edge	t_{IH_F}	SR	2	–	ns	
Outputs valid time in full speed mode	t_{ODLY_F}	CC	–	10	ns	
Outputs hold time in full speed mode	t_{OH_F}	CC	0	–	ns	

Table 43 SD Card Bus Timing for Full-Speed Mode[1)]

Parameter	Symbol	Values		Unit	Note/ Test Condition
		Min.	Max.		
SD card input setup time	t_{ISU}	5	–	ns	
SD card input hold time	t_{IH}	5	–	ns	
SD card output valid time	t_{ODLY}	–	14	ns	
SD card output hold time	t_{OH}	0	–	ns	

1) Reference card timing values for calculation examples. Not subject to production test and not characterized.

Full-Speed Output Path (Write)

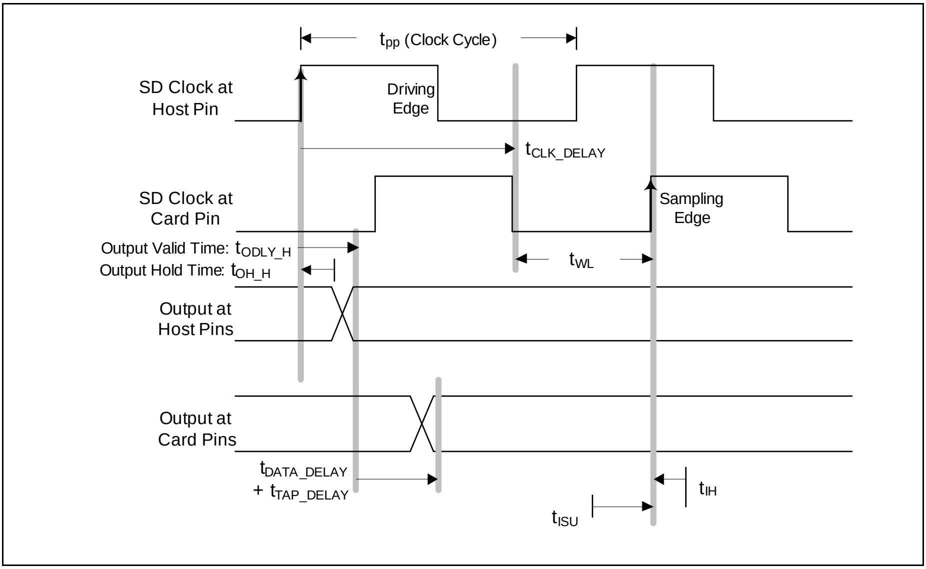


Figure 25 Full-Speed Output Path

Full-Speed Write Meeting Setup (Maximum Delay)

The following equations show how to calculate the allowed skew range between the SD_CLK and SD_DAT/CMD signals on the PCB.

No clock delay:

(1)

$$t_{ODLY\_F} + t_{DATA\_DELAY} + t_{TAP\_DELAY} + t_{ISU} < t_{WL}$$

With clock delay:

(2)

$$t_{ODLY\_F} + t_{DATA\_DELAY} + t_{TAP\_DELAY} + t_{ISU} < t_{WL} + t_{CLK\_DELAY}$$

(3)

$$t_{DATA\_DELAY} + t_{TAP\_DELAY} + t_{WL} < t_{PP} + t_{CLK\_DELAY} - t_{ISU} - t_{ODLY\_F}$$

$$t_{DATA\_DELAY} + t_{TAP\_DELAY} + 20 < 40 + t_{CLK\_DELAY} - 5 - 10$$

$$t_{DATA\_DELAY} < 5 + t_{CLK\_DELAY} - t_{TAP\_DELAY}$$

The data can be delayed versus clock up to 5 ns in ideal case of t_{WL}= 20 ns.

Full-Speed Write Meeting Hold (Minimum Delay)

The following equations show how to calculate the allowed skew range between the SD_CLK and SD_DAT/CMD signals on the PCB.

(4)

$$t_{CLK\_DELAY} < t_{WL} + t_{OH\_F} + t_{DATA\_DELAY} + t_{TAP\_DELAY} - t_{IH}$$

$$t_{CLK\_DELAY} < 20 + t_{DATA\_DELAY} + t_{TAP\_DELAY} - 5$$

$$t_{DATA\_DELAY} < 15 + t_{CLK\_DELAY} + t_{TAP\_DELAY}$$

The clock can be delayed versus data up to 18.2 ns (external delay line) in ideal case of t_{WL}= 20 ns, with maximum t_{TAP_DELAY} = 3.2 ns programmed.

Full-Speed Input Path (Read)

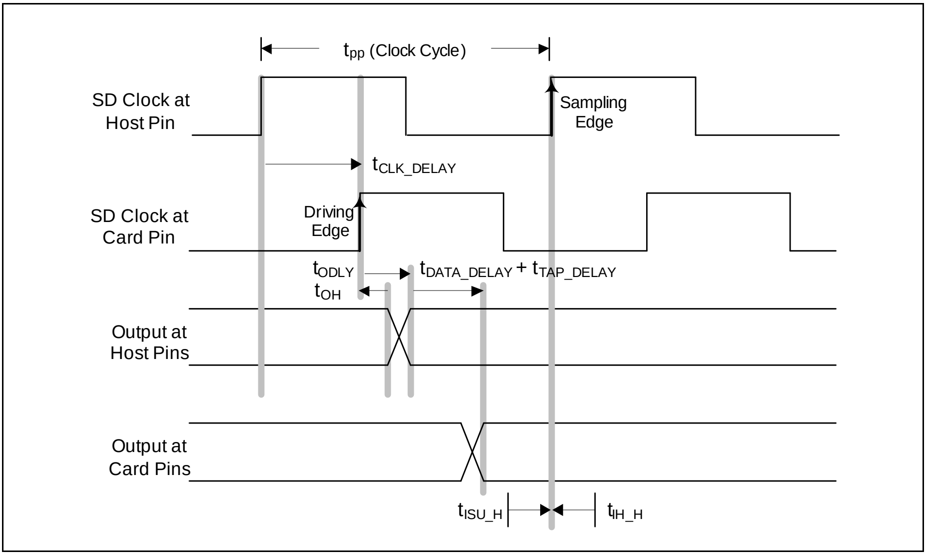


Figure 26 Full-Speed Input Path

Full-Speed Read Meeting Setup (Maximum Delay)

The following equations show how to calculate the allowed combined propagation delay range of the SD_CLK and SD_DAT/CMD signals on the PCB.

(5)

$$t_{CLK\_DELAY} + t_{DATA\_DELAY} + t_{TAP\_DELAY} + t_{ODLY} + t_{ISU\_F} < 0{,}5 \times t_{pp}$$

$$t_{CLK\_DELAY} + t_{DATA\_DELAY} < 0{,}5 \times t_{pp} - t_{ODLY} - t_{ISU\_F} - t_{TAP\_DELAY}$$

$$t_{CLK\_DELAY} + t_{DATA\_DELAY} < 20 - 14 - 2 - t_{TAP\_DELAY}$$

$$t_{CLK\_DELAY} + t_{DATA\_DELAY} < 4 - t_{TAP\_DELAY}$$

The data + clock delay can be up to 4 ns for a 40 ns clock cycle.

Full-Speed Read Meeting Hold (Minimum Delay)

The following equations show how to calculate the allowed combined propagation delay range of the SD_CLK and SD_DAT/CMD signals on the PCB.

(6)

$$t_{CLK\_DELAY} + t_{OH} + t_{DATA\_DELAY} + t_{TAP\_DELAY} > t_{IH\_F}$$

$$t_{CLK\_DELAY} + t_{DATA\_DELAY} > t_{IH\_F} - t_{OH} - t_{TAP\_DELAY}$$

$$t_{CLK\_DELAY} + t_{DATA\_DELAY} > 2 - t_{TAP\_DELAY}$$

The data + clock delay must be greater than 2 ns if t_{TAP_DELAY} is not used.

If the t_{TAP_DELAY} is programmed to at least 2 ns, the data + clock delay must be greater than 0 ns (or less). This is always fulfilled.

AC Timing Specifications (High-Speed Mode)

Table 44 SDMMC Timing for High-Speed Mode

Parameter	Symbol		Values		Unit	Note/ Test Condition
			Min.	Max.		
Clock frequency in high speed transfer mode ($1/t_{pp}$)	f_{pp}	CC	0	48	MHz	
Clock cycle in high speed transfer mode	t_{pp}	CC	20	–	ns	
Clock low time	t_{WL}	CC	7	–	ns	
Clock high time	t_{WH}	CC	7	–	ns	
Clock rise time	t_{TLH}	CC	–	3	ns	
Clock fall time	t_{THL}	CC	–	3	ns	
Inputs setup to clock rising edge	t_{ISU_H}	SR	2	–	ns	
Inputs hold after clock rising edge	t_{IH_H}	SR	2	–	ns	
Outputs valid time in high speed mode	t_{ODLY_H}	CC	–	14	ns	
Outputs hold time in high speed mode	t_{OH_H}	CC	2	–	ns	

Table 45 SD Card Bus Timing for High-Speed Mode[1)]

Parameter	Symbol	Values		Unit	Note/ Test Condition
		Min.	Max.		
SD card input setup time	t_{ISU}	6	–	ns	
SD card input hold time	t_{IH}	2	–	ns	
SD card output valid time	t_{ODLY}	–	14	ns	
SD card output hold time	t_{OH}	2.5	–	ns	

1) Reference card timing values for calculation examples. Not subject to production test and not characterized.

High-Speed Output Path (Write)

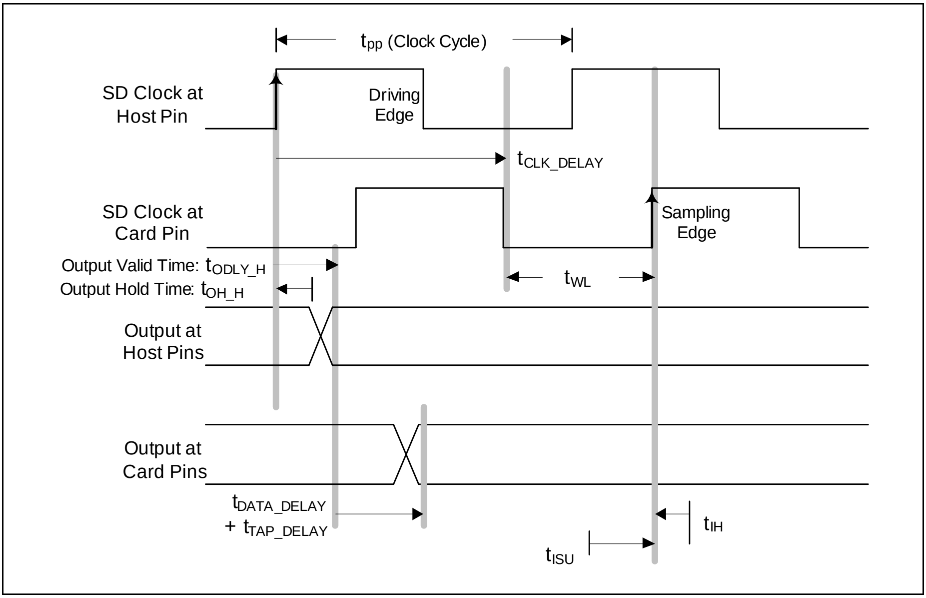


Figure 27 High-Speed Output Path

High-Speed Write Meeting Setup (Maximum Delay)

The following equations show how to calculate the allowed skew range between the SD_CLK and SD_DAT/CMD signals on the PCB.

No clock delay:

$$t_{ODLY\_H} + t_{DATA\_DELAY} + t_{TAP\_DELAY} + t_{ISU} < t_{WL} \tag{7}$$

With clock delay:

$$t_{ODLY\_H} + t_{DATA\_DELAY} + t_{TAP\_DELAY} + t_{ISU} < t_{WL} + t_{CLK\_DELAY} \tag{8}$$

(9)

$$t_{DATA\_DELAY} + t_{TAP\_DELAY} - t_{CLK\_DELAY} < t_{WL} - t_{ISU} - t_{ODLY\_H}$$

$$t_{DATA\_DELAY} - t_{CLK\_DELAY} < t_{WL} - t_{ISU} - t_{ODLY\_H} - t_{TAP\_DELAY}$$

$$t_{DATA\_DELAY} - t_{CLK\_DELAY} < 10 - 6 - 14 - t_{TAP\_DELAY}$$

$$t_{DATA\_DELAY} - t_{CLK\_DELAY} < -10 - t_{TAP\_DELAY}$$

The data delay is less than the clock delay by at least 10 ns in the ideal case where t_{WL}= 10 ns.

High-Speed Write Meeting Hold (Minimum Delay)

The following equations show how to calculate the allowed skew range between the SD_CLK and SD_DAT/CMD signals on the PCB.

(10)

$$t_{CLK\_DELAY} < t_{WL} + t_{OH\_H} + t_{DATA\_DELAY} + t_{TAP\_DELAY} - t_{IH}$$

$$t_{CLK\_DELAY} - t_{DATA\_DELAY} < t_{WL} + t_{OH\_H} + t_{TAP\_DELAY} - t_{IH}$$

$$t_{CLK\_DELAY} - t_{DATA\_DELAY} < 10 + 2 + t_{TAP\_DELAY} - 2$$

$$t_{CLK\_DELAY} - t_{DATA\_DELAY} < 10 + t_{TAP\_DELAY}$$

The clock can be delayed versus data up to 13.2 ns (external delay line) in ideal case of t_{WL}= 10 ns, with maximum t_{TAP_DELAY} = 3.2 ns programmed.

High-Speed Input Path (Read)

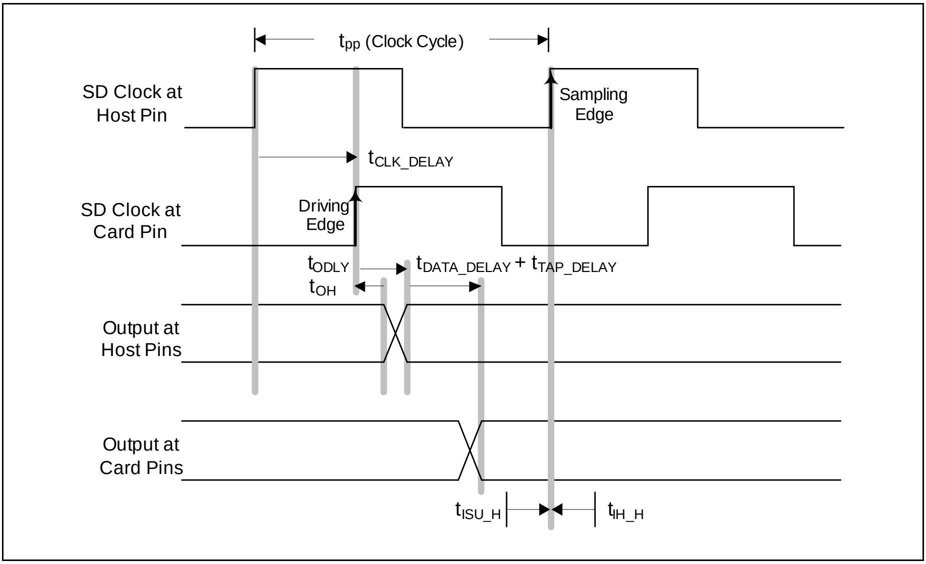


Figure 28 High-Speed Input Path

High-Speed Read Meeting Setup (Maximum Delay)

The following equations show how to calculate the allowed combined propagation delay range of the SD_CLK and SD_DAT/CMD signals on the PCB.

(11)

$$t_{CLK\_DELAY} + t_{DATA\_DELAY} + t_{TAP\_DELAY} + t_{ODLY} + t_{ISU\_H} < t_{pp}$$

$$t_{CLK\_DELAY} + t_{DATA\_DELAY} < t_{pp} - t_{ODLY} - t_{ISU\_H} - t_{TAP\_DELAY}$$

$$t_{CLK\_DELAY} + t_{DATA\_DELAY} < 20 - 14 - 2 - t_{TAP\_DELAY}$$

$$t_{CLK\_DELAY} + t_{DATA\_DELAY} < 4 - t_{TAP\_DELAY}$$

The data + clock delay can be up to 4 ns for a 20 ns clock cycle.

High-Speed Read Meeting Hold (Minimum Delay)

The following equations show how to calculate the allowed combined propagation delay range of the SD_CLK and SD_DAT/CMD signals on the PCB.

(12)

$$t_{CLK\_DELAY} + t_{OH} + t_{DATA\_DELAY} + t_{TAP\_DELAY} > t_{IH\_H}$$

$$t_{CLK\_DELAY} + t_{DATA\_DELAY} > t_{IH\_H} - t_{OH} - t_{TAP\_DELAY}$$

$$t_{CLK\_DELAY} + t_{DATA\_DELAY} > 2 - 2{,}5 - t_{TAP\_DELAY}$$

$$t_{CLK\_DELAY} + t_{DATA\_DELAY} > -0{,}5 - t_{TAP\_DELAY}$$

The data + clock delay must be greater than -0.5 ns for a 20 ns clock cycle. This is always fulfilled.

3.3.10 EBU Timings

Note: These parameters are not subject to production test, but verified by design and/or characterization.

Note: Operating Conditions apply, with Class A2 pins and C_L = 16 pF.

3.3.10.1 EBU Asynchronous Timings

Note: For each timing, the accumulated PLL jitter of the programmed duration in number of clock periods must be added separately.

Table 46 Common Timing Parameters for all Asynchronous Timings

Parameter			Symbol	Limit Values		Unit	Edge Setting
				Min.	Max.		
Pulse width deviation from the ideal programmed width due to the A2 pad asymmetry, strong driver mode, rise delay - fall delay. C_L = 16 pF.		CC	t_a	-1	1.5	ns	sharp
				-2	1		medium
AD(24:16) output delay	to $\overline{\text{ADV}}$ rising edge, multiplexed read / write	CC	t_{13}	-5.5	2		–
AD(24:16) output delay		CC	t_{14}	-5.5	2		–

Read Timings

Table 47 Asynchronous Read Timings, Multiplexed and Demultiplexed

Parameter			Symbol	Limit Values		Unit
				Min.	Max.	
A(24:16) output delay	to $\overline{RD}$ rising edge, deviation from the ideal programmed value.	CC	t_0	-2.5	2.5	ns
A(24:16) output delay		CC	t_1	-2.5	2.5	
$\overline{CS}$ rising edge		CC	t_2	-2	2.5	
$\overline{ADV}$ rising edge		CC	t_3	-1.5	4.5	
$\overline{BC}$ rising edge		CC	t_4	-2.5	2.5	
$\overline{WAIT}$ input setup		SR	t_5	12	–	
$\overline{WAIT}$ input hold		SR	t_6	0	–	
Data input setup		SR	t_7	12	–	
Data input hold		SR	t_8	0	–	
RD / $\overline{WR}$ output delay		CC	t_9	-2.5	1.5	

Multiplexed Read Timing

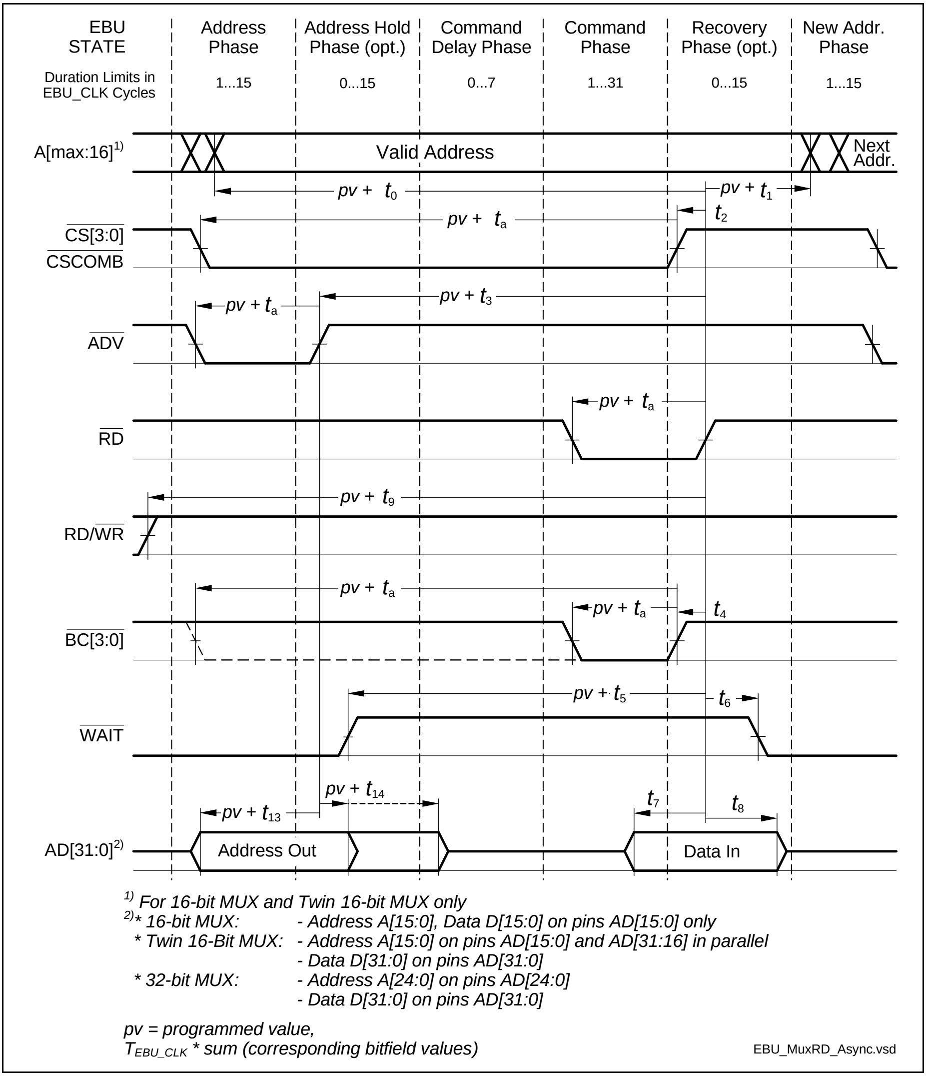


Figure 29 Multiplexed Read Access

Demultiplexed Read Timing

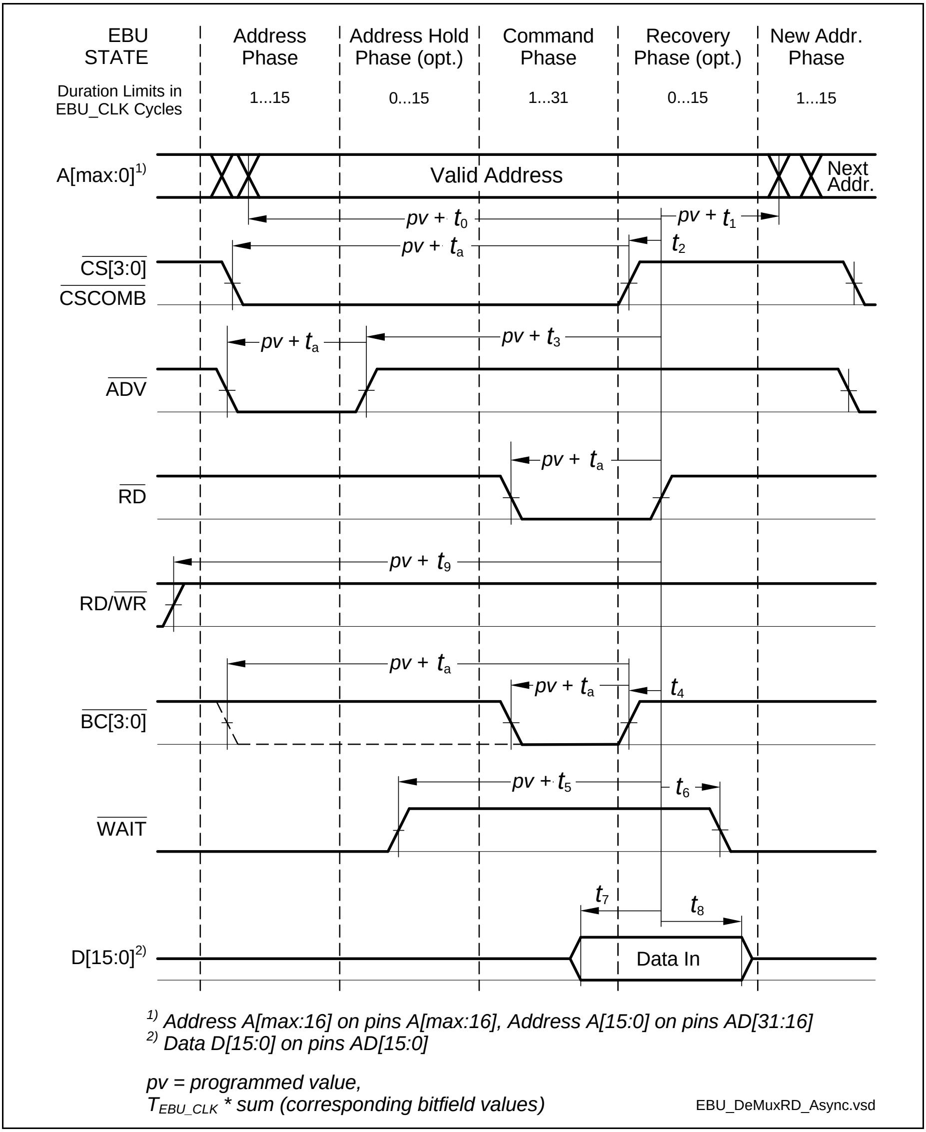


Figure 30 Demultiplexed Read Access

Write Timings

Table 48 Asynchronous Write Timings, Multiplexed and Demultiplexed

Parameter			Symbol	Limit Values		Unit
				Min.	Max.	
A(24:0) output delay	to RD/$\overline{WR}$ rising edge, deviation from the ideal programmed value.	CC	t_{30}	-2.5	2.5	ns
A(24:0) output delay		CC	t_{31}	-2.5	2.5	
$\overline{CS}$ rising edge		CC	t_{32}	-2	2	
$\overline{ADV}$ rising edge		CC	t_{33}	-2	4.5	
$\overline{BC}$ rising edge		CC	t_{34}	-2.5	2	
$\overline{WAIT}$ input setup		SR	t_{35}	12	–	
$\overline{WAIT}$ input hold		SR	t_{36}	0	–	
Data output delay		CC	t_{37}	-5.5	2	
Data output delay		CC	t_{38}	-5.5	2	
RD / $\overline{WR}$ output delay		CC	t_{39}	-2.5	1.5	

Multiplexed Write Timing

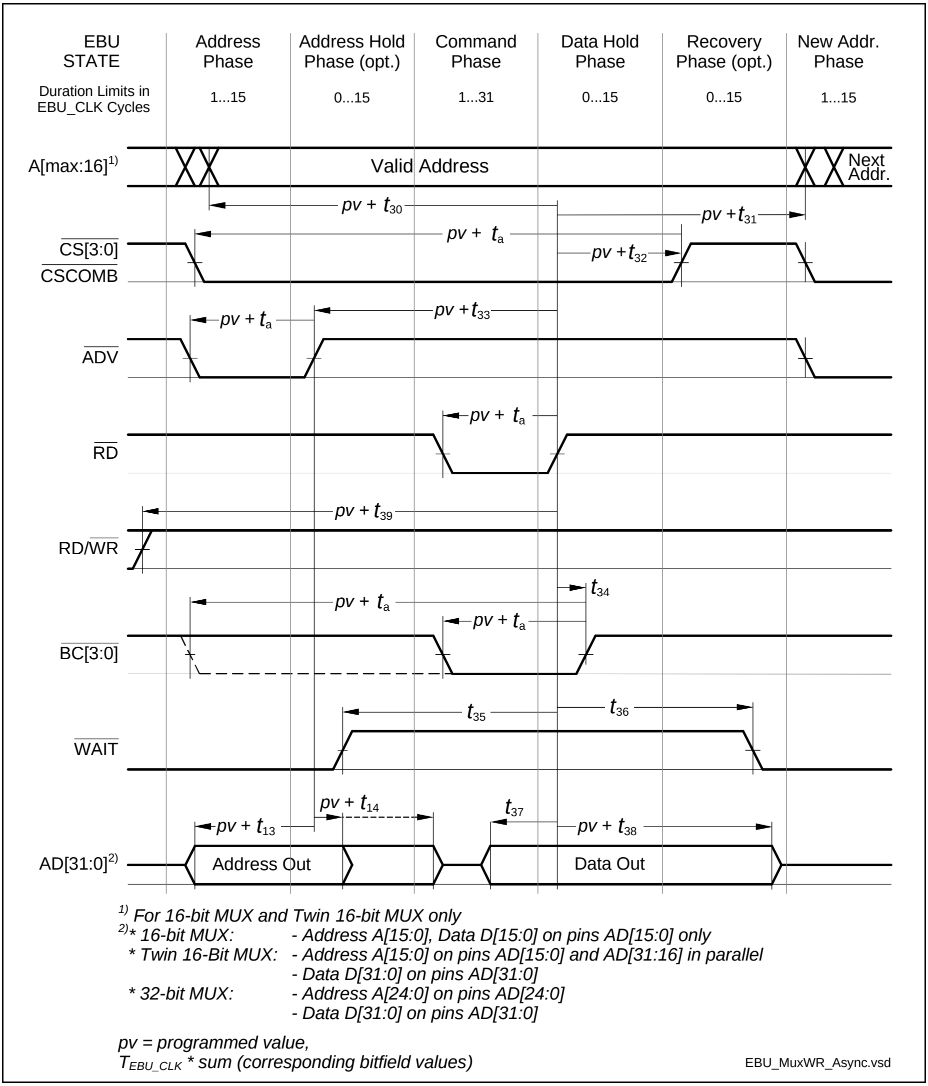


Figure 31 Multiplexed Write Access

Demultiplexed Write Timing

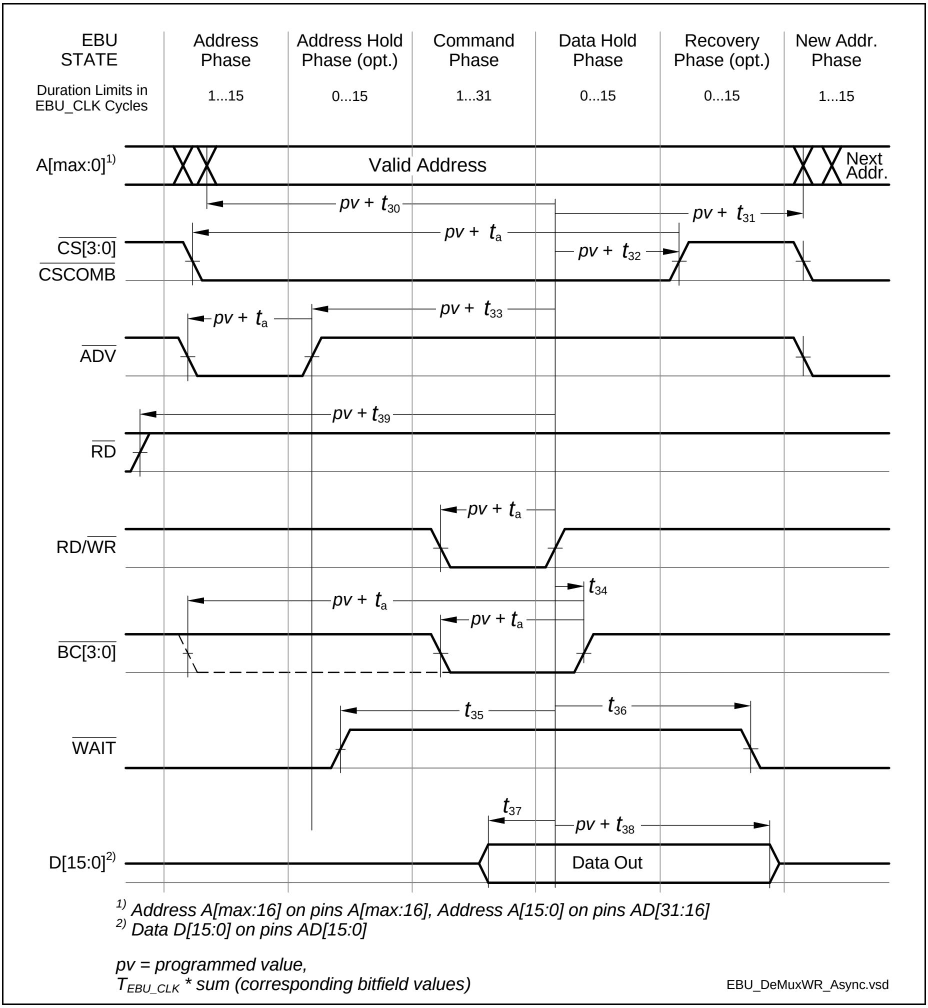


Figure 32 Demultiplexed Write Access

3.3.10.2 EBU Burst Mode Access Timing

Note: These parameters are not subject to production test, but verified by design and/or characterization.

Note: Operating Conditions apply, with Class A2 pins and C_L = 16 pF.

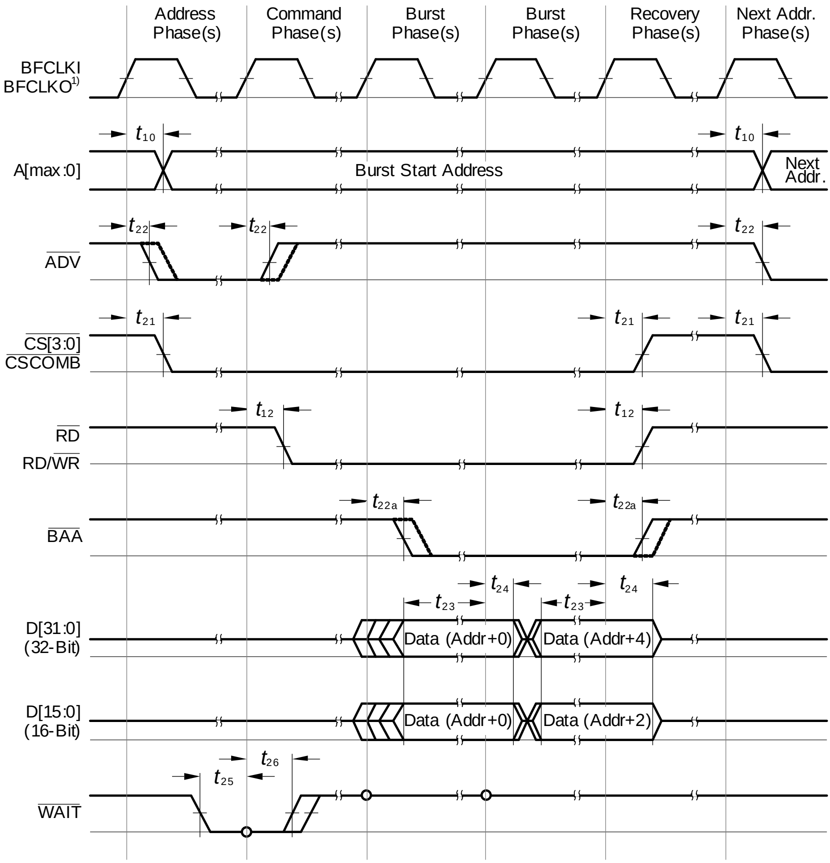
Table 49 EBU Burst Mode Read / Write Access Timing Parameters

Parameter	Symbol		Values			Unit	Note / Test Condition
			Min.	Typ.	Max.		
Output delay from BFCLKO rising edge	t_{10}	CC	-2	–	2	ns	–
$\overline{\text{RD}}$ and RD/$\overline{\text{WR}}$ active/inactive after BFCLKO active edge[1]	t_{12}	CC	-2	–	2	ns	–
$\overline{\text{CS}}$x output delay from BFCLKO active edge[1]	t_{21}	CC	-2.5	–	1.5	ns	–
$\overline{\text{ADV}}$ active/inactive after BFCLKO active edge[2]	t_{22}	CC	-2	–	2	ns	–
$\overline{\text{BAA}}$ active/inactive after BFCLKO active edge[2]	t_{22a}	CC	-2.5	–	1.5	ns	–
Data setup to BFCLKI rising edge[3]	t_{23}	SR	3	–	–	ns	–
Data hold from BFCLKI rising edge[3]	t_{24}	SR	0	–	–	ns	–
$\overline{\text{WAIT}}$ setup (low or high) to BFCLKI rising edge[3]	t_{25}	SR	3	–	–	ns	–
$\overline{\text{WAIT}}$ hold (low or high) from BFCLKI rising edge[3]	t_{26}	SR	0	–	–	ns	–

1) An active edge can be a rising or falling edge, depending on the settings of bits BFCON.EBSE / ECSE and the clock divider ratio.
Negative minimum values for these parameters mean that the last data read during a burst may be corrupted. However, with clock feedback enabled, this value is an oversampling not required for the internal bus transaction, and will be discarded.

2) This parameter is valid for BUSCONx.EBSE = 1 and BUSAPx.EXTCLK = 00_B.
For BUSCONx.EBSE = 1 and other values of BUSAPx.EXTCLK, ADV and BAA will be delayed by 1/2 of the internal bus clock period $T_{CPU} = 1 / f_{CPU}$.
For BUSCONx. EBSE = 0 and BUSAPx.EXTCLK = 11_B, add 2 internal bus clock periods.
For BUSCONx. EBSE = 0 and other values of BUSAPx.EXTCLK, add 1 internal bus clock period.

3) If the clock feedback is not enabled, the input signals are latched using the internal clock in the same way as for asynchronous access. Thus, t_5, t_6, t_7 and t_8 from the asynchronous timings apply.



1) Output delays are always referenced to BCLKO . The reference clock for input characteristics depends on bit EBU _BFCON.FDBKEN.
EBU_BFCON.FDBKEN= 0: BFCLKO is the input reference clock .
EBU_BFCON.FDBKEN= 1: BFCLKI is the input reference clock (EBU clock feedback enabled).

EBU_BurstRDWR.vsd

Figure 33 EBU Burst Mode Read / Write Access Timing

3.3.10.3 EBU Arbitration Signal Timing

Note: These parameters are not subject to production test, but verified by design and/or characterization.

Note: Operating Conditions apply.

Table 50 EBU Arbitration Signal Timing Parameters

Parameter	Symbol		Values			Unit	Note / Test Condition
			Min.	Typ.	Max.		
Output delay from BFCLKO rising edge	t_1	CC	–	–	16	ns	C_L = 50 pF
Data setup to BFCLKO falling edge	t_2	SR	11	–	–	ns	–
Data hold from BFCLKO falling edge	t_3	SR	2	–	–	ns	–

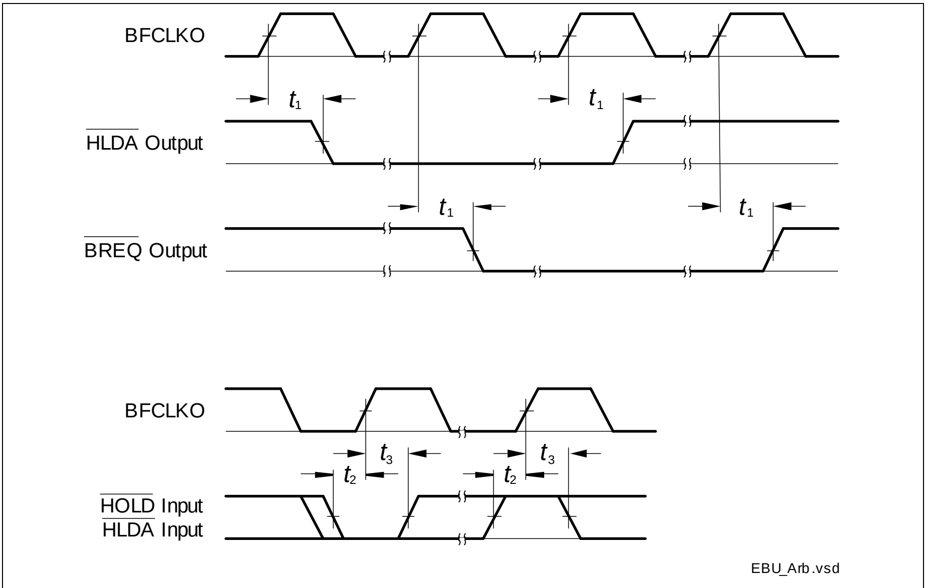


Figure 34 EBU Arbitration Signal Timing

3.3.10.4 EBU SDRAM Access Timing

Note: These parameters are not subject to production test, but verified by design and/or characterization.

Note: Operating Conditions apply, with Class A2 pins and C_L = 16 pF.

Table 51 EBU SDRAM Access SDCLKO Signal Timing Parameters

Parameter	Symbol		Values			Unit	Note / Test Con dition
			Min.	Typ.	Max.		
SDCLKO period	t_1	CC	12.5	–	–	ns	–
SDCLKO high time	t_2	SR	5.5	–	–	ns	–
SDCLKO low time	t_3	SR	3.75	–	–	ns	–
SDCLKO rise time	t_4	SR	–	–	3.0	ns	–
SDCLKO fall time	t_5	SR	–	–	3.0	ns	–

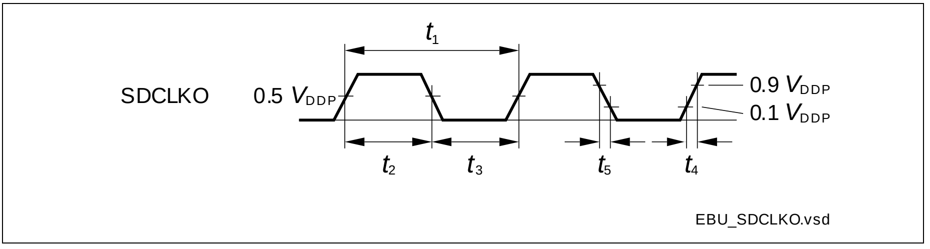


Figure 35 EBU SDRAM Access CLKOUT Timing

Table 52 EBU SDRAM Access Signal Timing Parameters

Parameter		Symbol		Limit Values		Unit
				Min.	Max.	
A(15:0) output valid	from SDCLKO low-to-high transition	CC	t_6	–	9	ns
A(15:0) output hold		CC	t_7	3	–	
$\overline{\text{CS}}$(3:0) low		CC	t_8	–	9	
$\overline{\text{CS}}$(3:0) high		CC	t_9	3	–	
$\overline{\text{RAS}}$ low		CC	t_{10}	–	9	
$\overline{\text{RAS}}$ high		SR	t_{11}	3	–	
$\overline{\text{CAS}}$ low		SR	t_{12}	–	9	
$\overline{\text{CAS}}$ high		CC	t_{13}	3	–	
RD/$\overline{\text{WR}}$ low		CC	t_{14}	–	9	
RD/$\overline{\text{WR}}$ high		CC	t_{15}	3	–	
$\overline{\text{BC}}$(3:0) low		CC	t_{16}	–	9	
$\overline{\text{BC}}$(3:0) high		CC	t_{17}	3	–	
D(15:0) output valid		CC	t_{18}	–	9	
D(15:0) output hold		CC	t_{19}	3	–	
CKE output valid[1)]		CC	t_{22}	–	7	
CKE output hold[1)]		CC	t_{23}	2	–	
D(15:0) input hold		SR	t_{21}	3	–	
D(15:0) input setup to SDCLKO low-to-high transition		SR	t_{20}	4	–	

1) Not depicted in the read and write access timing figures below.

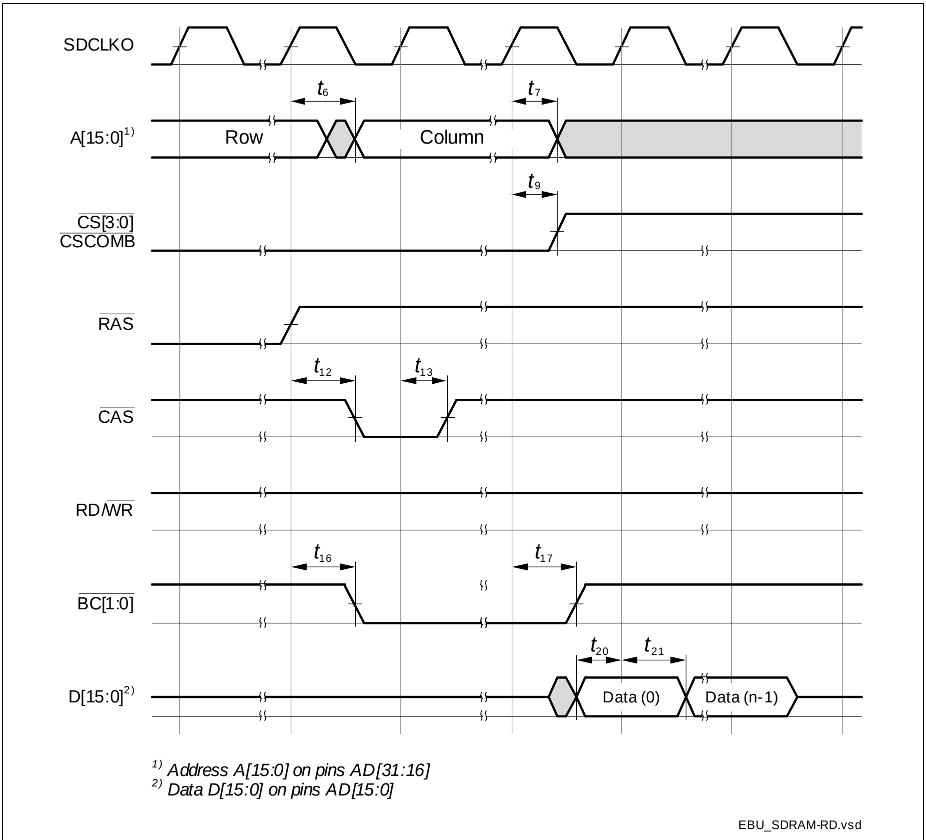


Figure 36 EBU SDRAM Read Access Timing

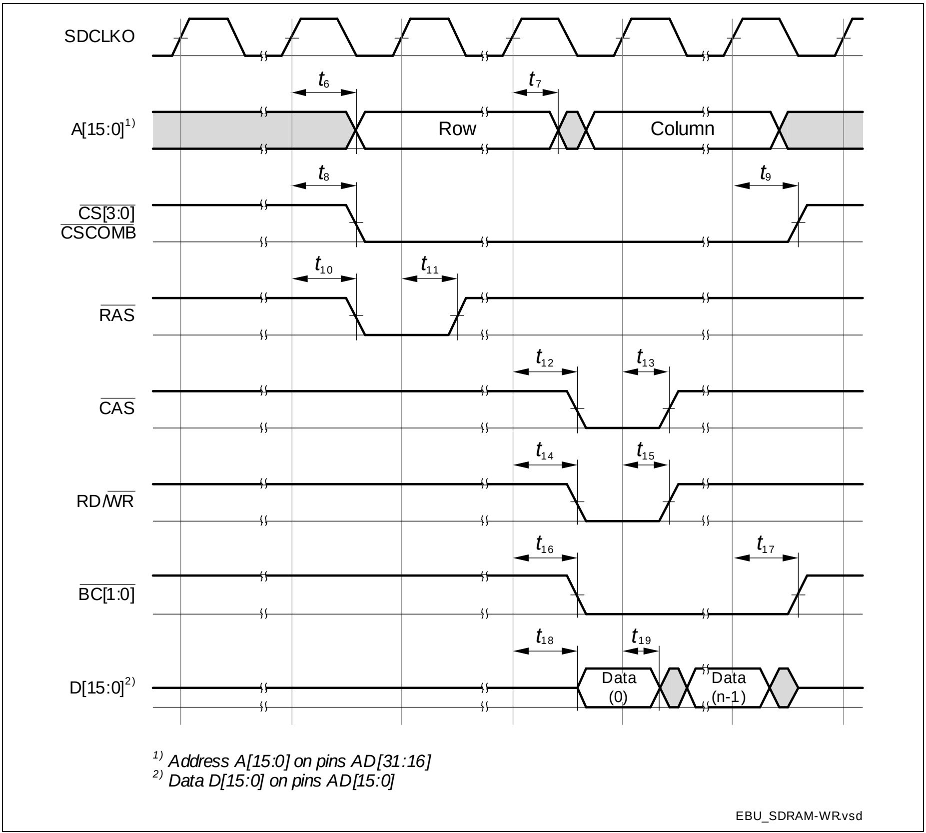


Figure 37 EBU SDRAM Write Access Timing

3.3.11 USB Interface Characteristics

The Universal Serial Bus (USB) Interface is compliant to the USB Rev. 2.0 Specification and the OTG Specification Rev. 1.3. High-Speed Mode is not supported.

Note: These parameters are not subject to production test, but verified by design and/or characterization.

Table 53 USB Timing Parameters (operating conditions apply)

Parameter	Symbol		Values			Unit	Note / Test Condition
			Min.	Typ.	Max.		
Rise time	t_R	CC	4	–	20	ns	C_L = 50 pF
Fall time	t_F	CC	4	–	20	ns	C_L = 50 pF
Rise/Fall time matching	t_R/t_F	CC	90	–	111.11	%	C_L = 50 pF
Crossover voltage	V_{CRS}	CC	1.3	–	2.0	V	C_L = 50 pF

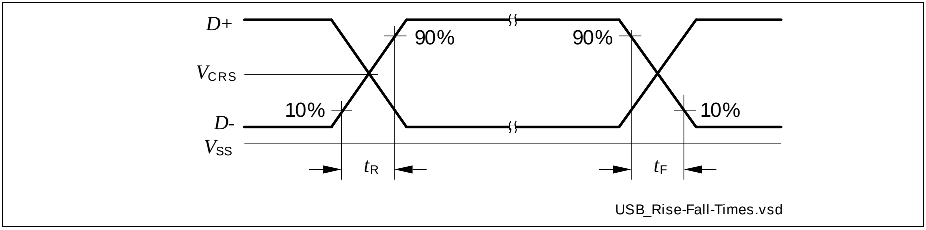


Figure 38 USB Signal Timing

3.3.12 Ethernet Interface (ETH) Characteristics

For proper operation of the Ethernet Interface it is required that $f_{SYS} \geq 100$ MHz.

Note: These parameters are not subject to production test, but verified by design and/or characterization.

3.3.12.1 ETH Measurement Reference Points

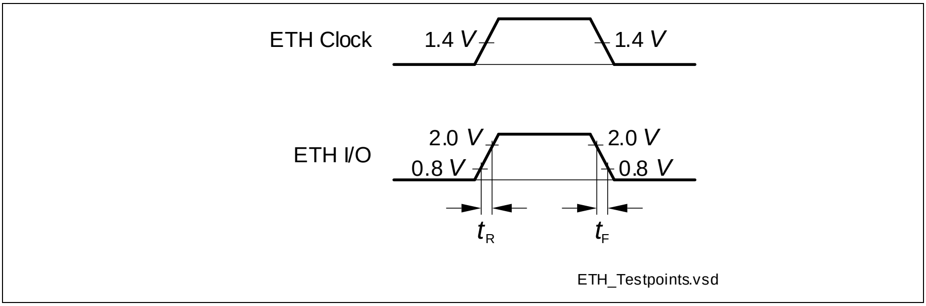


Figure 39 ETH Measurement Reference Points

3.3.12.2 ETH Management Signal Parameters (ETH_MDC, ETH_MDIO)

Table 54 ETH Management Signal Timing Parameters

Parameter	Symbol		Values			Unit	Note / Test Condition
			Min.	Typ.	Max.		
ETH_MDC period	t_1	CC	400	–	–	ns	C_L = 25 pF
ETH_MDC high time	t_2	CC	160	–	–	ns	
ETH_MDC low time	t_3	CC	160	–	–	ns	
ETH_MDIO setup time (output)	t_4	CC	10	–	–	ns	
ETH_MDIO hold time (output)	t_5	CC	10	–	–	ns	
ETH_MDIO data valid (input)	t_6	SR	0	–	300	ns	

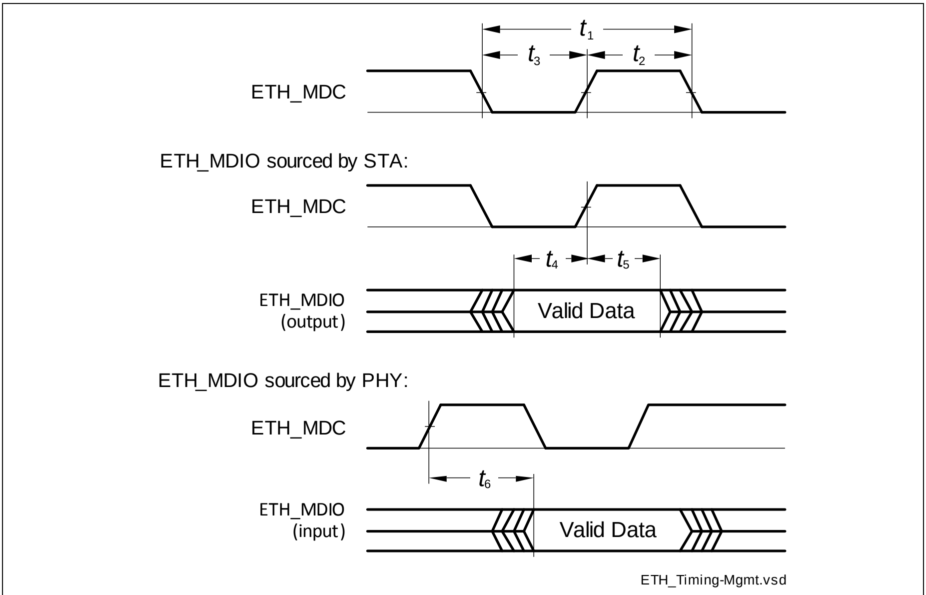


Figure 40 ETH Management Signal Timing

3.3.12.3 ETH MII Parameters

In the following, the parameters of the MII (Media Independent Interface) are described.

Table 55 ETH MII Signal Timing Parameters

Parameter	Symbol		Values			Unit	Note / Test Condition
			Min.	Typ.	Max.		
Clock period, 10 Mbps	t_7	SR	400	–	–	ns	C_L = 25 pF
Clock high time, 10 Mbps	t_8	SR	140	–	260	ns	
Clock low time, 10 Mbps	t_9	SR	140	–	260	ns	
Clock period, 100 Mbps	t_7	SR	40	–	–	ns	
Clock high time, 100 Mbps	t_8	SR	14	–	26	ns	
Clock low time, 100 Mbps	t_9	SR	14	–	26	ns	
Input setup time	t_{10}	SR	10	–	–	ns	
Input hold time	t_{11}	SR	10	–	–	ns	
Output valid time	t_{12}	CC	0	–	25	ns	

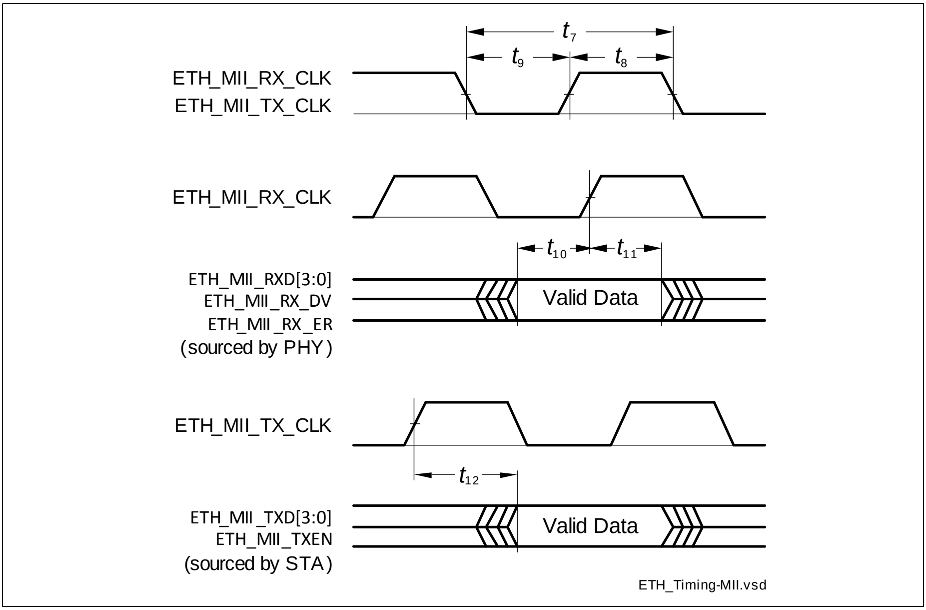


Figure 41 ETH MII Signal Timing

3.3.12.4 ETH RMII Parameters

In the following, the parameters of the RMII (Reduced Media Independent Interface) are described.

Table 56 ETH RMII Signal Timing Parameters

Parameter	Symbol		Values			Unit	Note / Test Condition
			Min.	Typ.	Max.		
ETH_RMII_REF_CL clock period	t_{13}	SR	20	–	–	ns	C_L = 25 pF; 50 ppm
ETH_RMII_REF_CL clock high time	t_{14}	SR	7	–	13	ns	C_L = 25 pF
ETH_RMII_REF_CL clock low time	t_{15}	SR	7	–	13	ns	
ETH_RMII_RXD[1:0], ETH_RMII_CRS setup time	t_{16}	SR	4	–	–	ns	
ETH_RMII_RXD[1:0], ETH_RMII_CRS hold time	t_{17}	SR	2	–	–	ns	
ETH_RMII_TXD[1:0], ETH_RMII_TXEN data valid	t_{18}	CC	–	–	15	ns	

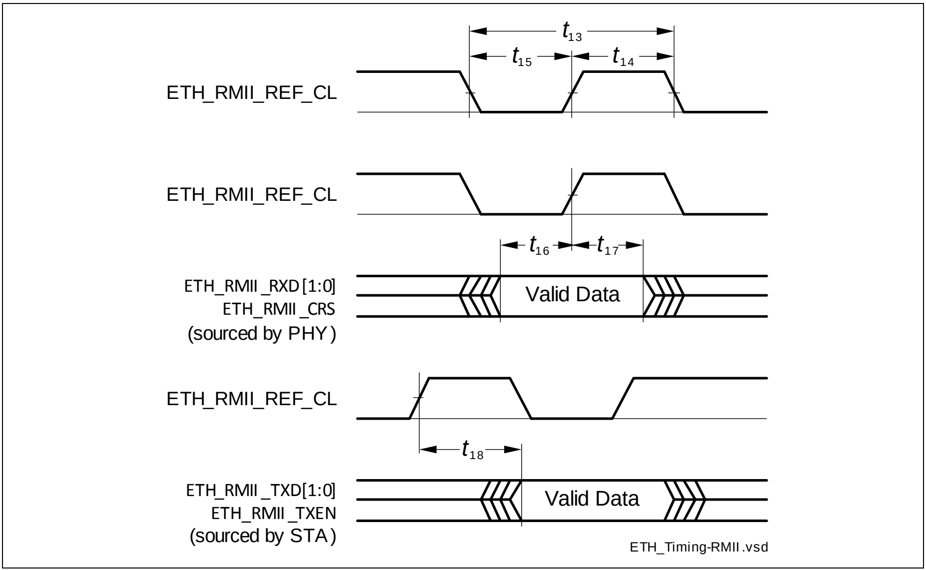


Figure 42 ETH RMII Signal Timing

4 Package and Reliability

The XMC4500 is a member of the XMC4000 Derivatives of microcontrollers. It is also compatible to a certain extent with members of similar families or subfamilies.

Each package is optimized for the device it houses. Therefore, there may be slight differences between packages of the same pin-count but for different device types. In particular, the size of the Exposed Die Pad may vary.

If different device types are considered or planned for an application, it must be ensured that the board layout fits all packages under consideration.

4.1 Package Parameters

Table 57 provides the thermal characteristics of the packages used in XMC4500.

Table 57 Thermal Characteristics of the Packages

Parameter	Symbol	Limit Values		Unit	Package Types
		Min.	Max.		
Exposed Die Pad Dimensions	Ex × Ey CC	-	6.5 × 6.5	mm	PG-LQFP-144-18
		-	7.0 × 7.0	mm	PG-LQFP-100-11
Thermal resistance Junction-Ambient	$R_{\Theta JA}$ CC	-	tbd	K/W	PG-LFBGA-144-4
		-	22.4	K/W	PG-LQFP-144-18[1)]
		-	23.0	K/W	PG-LQFP-100-11[1)]

1) Device mounted on a 4-layer JEDEC board (JESD 51-7) with thermal vias; exposed pad soldered.

Note: For electrical reasons, it is required to connect the exposed pad to the board ground V_{SS}, independent of EMC and thermal requirements.

4.1.1 Thermal Considerations

When operating the XMC4500 in a system, the total heat generated in the chip must be dissipated to the ambient environment to prevent overheating and the resulting thermal damage.

The maximum heat that can be dissipated depends on the package and its integration into the target board. The “Thermal resistance $R_{\Theta JA}$” quantifies these parameters. The power dissipation must be limited so that the average junction temperature does not exceed 150 °C.

The difference between junction temperature and ambient temperature is determined by $\Delta T = (P_{INT} + P_{IOSTAT} + P_{IODYN}) \times R_{\Theta JA}$

The internal power consumption is defined as
$P_{INT} = V_{DDP} \times I_{DDP}$ (switching current and leakage current).

The static external power consumption caused by the output drivers is defined as
$P_{IOSTAT} = \Sigma((V_{DDP}-V_{OH}) \times I_{OH}) + \Sigma(V_{OL} \times I_{OL})$

The dynamic external power consumption caused by the output drivers (P_{IODYN}) depends on the capacitive load connected to the respective pins and their switching frequencies.

If the total power dissipation for a given system configuration exceeds the defined limit, countermeasures must be taken to ensure proper system operation:

- Reduce V_{DDP}, if possible in the system
- Reduce the system frequency
- Reduce the number of output pins
- Reduce the load on active output drivers

4.2 Package Outlines

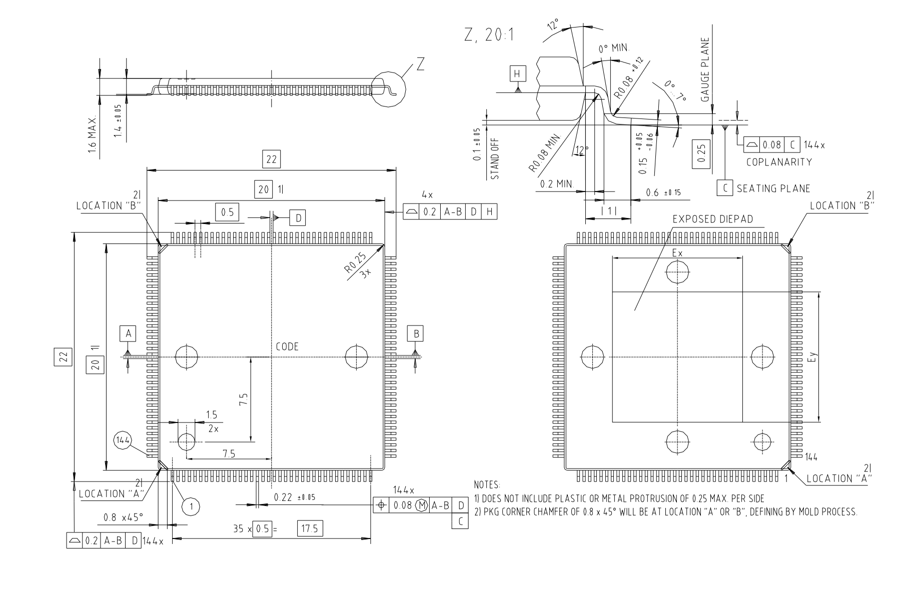


Figure 43 PG-LQFP-144-18 (Plastic Green Low Profile Quad Flat Package)

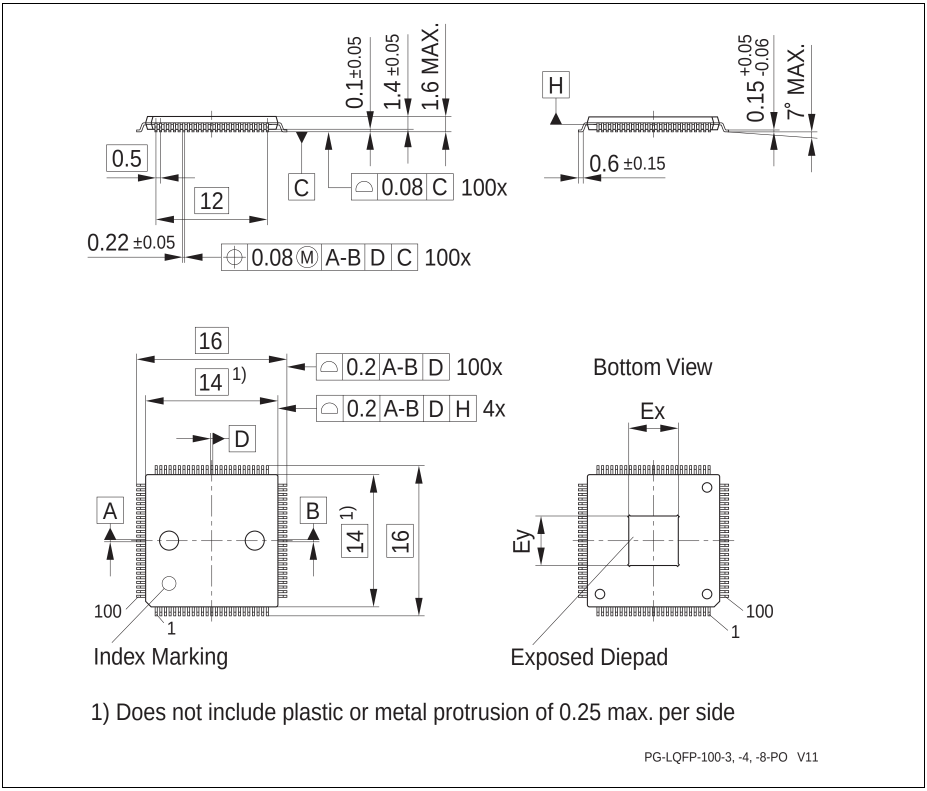


Figure 44 **PG-LQFP-100-11** (Plastic Green Low Profile Quad Flat Package)

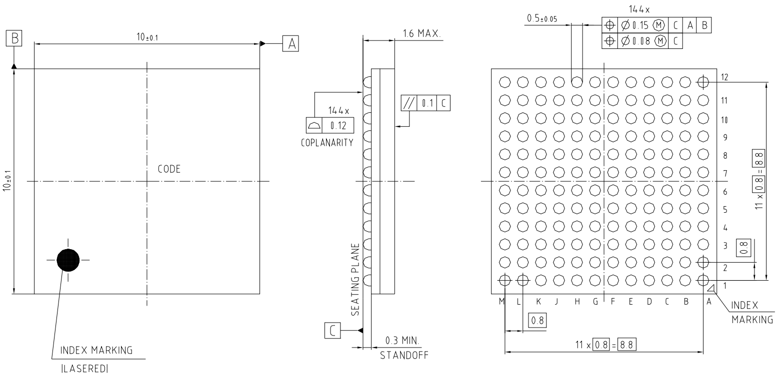


Figure 45 **PG-LFBGA-144-9** (Plastic Green Low Profile Fine Pitch Ball Grid Array)

All dimensions in mm.

You can find complete information about Infineon packages, packing and marking in our Infineon Internet Page "Packages": **http://www.infineon.com/packages**

4.3 Quality Declarations

The operation lifetime of the XMC4500 depends on the operating temperature. The life time decreases with increasing temperature as shown in **Table 59**.

Table 58 Quality Parameters

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Operation lifetime	t_{OP} CC	–	–	20	a	See **Table 59**
ESD susceptibility according to Human Body Model (HBM)	V_{HBM} SR	–	–	2 000	V	EIA/JESD22-A114-B
ESD susceptibility according to Charged Device Model (CDM)	V_{CDM} SR	–	–	500	V	Conforming to JESD22-C101-C
Moisture sensitivity level	MSL CC	–	–	3	–	JEDEC J-STD-020C

Table 59 Lifetime dependency from Temperature

Operating Time	Operating Temperature
20 a	$T_J \leq 110°C$
10 a	$T_J = 118°C$
5 a	$T_J = 130°C$
1 a	$T_J = 150°C$

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