EFM32®

... the world's most energy friendly microcontrollers

EFM32G290 DATASHEET

F128/F64/F32

- **ARM Cortex-M3 CPU platform**
  - High Performance 32-bit processor @ up to 32 MHz
  - Memory Protection Unit
  - Wake-up Interrupt Controller
- **Flexible Energy Management System**
  - 20 nA @ 3 V Shutoff Mode
  - 0.6 µA @ 3 V Stop Mode, including Power-on Reset, Brown-out Detector, RAM and CPU retention
  - 0.9 µA @ 3 V Deep Sleep Mode, including RTC with 32.768 kHz oscillator, Power-on Reset, Brown-out Detector, RAM and CPU retention
  - 45 µA/MHz @ 3 V Sleep Mode
  - 180 µA/MHz @ 3 V Run Mode, with code executed from flash
- **128/64/32 KB Flash**
- **16/16/8 KB RAM**
- **90 General Purpose I/O pins**
  - Configurable Push-pull, Open-drain, pull-up/down, input filter, drive strength
  - Configurable peripheral I/O locations
  - 16 asynchronous external interrupts
- **8 Channel DMA Controller**
- **8 Channel Peripheral Reflex System (PRS) for autonomous inter-peripheral signaling**
- **Hardware AES with 128/256-bit keys in 54/75 cycles**
- **Timers/Counters**
  - 3× 16-bit Timer/Counter
    - 3×3 Compare/Capture/PWM channels
    - Dead-Time Insertion on TIMER0
  - 16-bit Low Energy Timer
  - 24-bit Real-Time Counter
  - 3× 8-bit Pulse Counter
  - Watchdog Timer with dedicated RC oscillator @ 50 nA
- **External Bus Interface for up to 4×64 MB of external memory mapped space**
- **Communication interfaces**
  - 3× Universal Synchronous/Asynchronous Receiver/Transmitter
    - UART/SPI/SmartCard (ISO 7816)/IrDA
    - Triple buffered full/half-duplex operation
  - Universal Asynchronous Receiver/Transmitter
  - 2× Low Energy UART
    - Autonomous operation with DMA in Deep Sleep Mode
  - I^2C Interface with SMBus support
    - Address recognition in Stop Mode
- **Ultra low power precision analog peripherals**
  - 12-bit 1 Msamples/s Analog to Digital Converter
    - 8 single ended channels/4 differential channels
    - On-chip temperature sensor
    - Conversion tailgating for predictable latency
  - 12-bit 500 ksamples/s Digital to Analog Converter
    - 2 single ended channels/1 differential channel
  - 2× Analog Comparator
    - Capacitive sensing with up to 16 inputs
  - Supply Voltage Comparator
- **Ultra efficient Power-on Reset and Brown-Out Detector**
- **Pre-Programmed Serial Bootloader**
- **Temperature range -40 to 85 ºC**
- **Single power supply 1.85 to 3.8 V**
- **BGA112 package**

32-bit ARM Cortex-M0, Cortex-M3 and Cortex-M4F microcontrollers for:

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1 Ordering Information

Table 1.1 (p. 2) shows the available EFM32G290 devices.

Table 1.1. Ordering Information

Ordering Code	Flash (KB)	RAM (KB)	Max Speed (MHz)	Supply Voltage (V)	Temperature	Package
EFM32G290F32-BGA112	32	8	32	1.85 - 3.8	-40 - 85 ºC	BGA112
EFM32G290F64-BGA112	64	16	32	1.85 - 3.8	-40 - 85 ºC	BGA112
EFM32G290F128-BGA112	128	16	32	1.85 - 3.8	-40 - 85 ºC	BGA112

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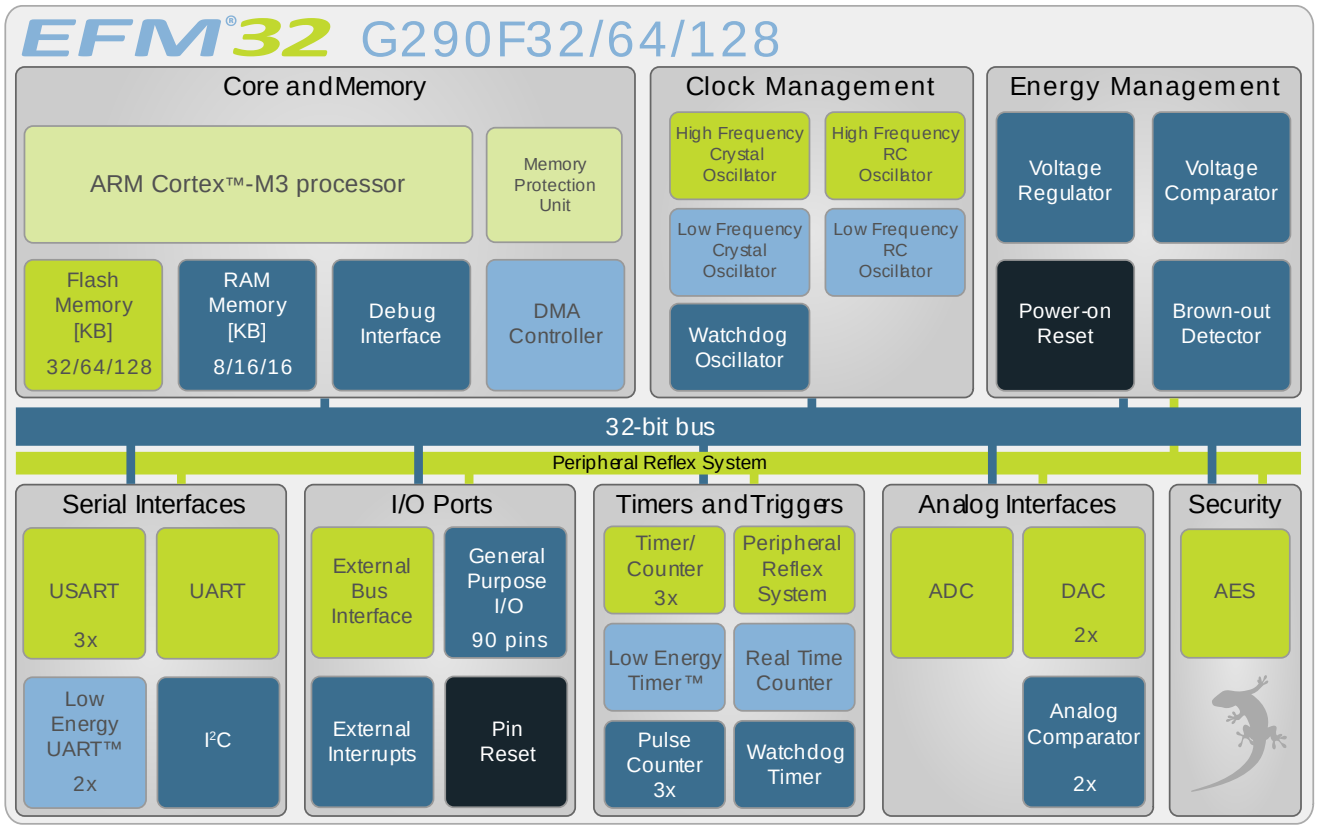
2 System Summary

2.1 System Introduction

The EFM32 MCUs are the world's most energy friendly microcontrollers. With a unique combination of the powerful 32-bit ARM Cortex-M3, innovative low energy techniques, short wake-up time from energy saving modes, and a wide selection of peripherals, the EFM32G microcontroller is well suited for any battery operated application as well as other systems requiring high performance and low-energy consumption. This section gives a short introduction to each of the modules in general terms and also and shows a summary of the configuration for the EFM32G290 devices. For a complete feature set and in-depth information on the modules, the reader is referred to the *EFM32G Reference Manual*.

A block diagram of the EFM32G290 is shown in Figure 2.1 (p. 3) .

Figure 2.1. Block Diagram



2.1.1 ARM Cortex-M3 Core

The ARM Cortex-M3 includes a 32-bit RISC processor which can achieve as much as 1.25 Dhrystone MIPS/MHz. A Memory Protection Unit with support for up to 8 memory segments is included, as well as a Wake-up Interrupt Controller handling interrupts triggered while the CPU is asleep. The EFM32 implementation of the Cortex-M3 is described in detail in *EFM32G Cortex-M3 Reference Manual*.

2.1.2 Debug Interface (DBG)

This device includes hardware debug support through a 2-pin serial-wire debug interface . In addition there is also a 1-wire Serial Wire Viewer pin which can be used to output profiling information, data trace and software-generated messages.

2.1.3 Memory System Controller (MSC)

The Memory System Controller (MSC) is the program memory unit of the EFM32G microcontroller. The flash memory is readable and writable from both the Cortex-M3 and DMA. The flash memory is divided

into two blocks; the main block and the information block. Program code is normally written to the main block. Additionally, the information block is available for special user data and flash lock bits. There is also a read-only page in the information block containing system and device calibration data. Read and write operations are supported in the energy modes EM0 and EM1.

2.1.4 Direct Memory Access Controller (DMA)

The Direct Memory Access (DMA) controller performs memory operations independently of the CPU. This has the benefit of reducing the energy consumption and the workload of the CPU, and enables the system to stay in low energy modes when moving for instance data from the USART to RAM or from the External Bus Interface to a PWM-generating timer. The DMA controller uses the PL230 µDMA controller licensed from ARM.

2.1.5 Reset Management Unit (RMU)

The RMU is responsible for handling the reset functionality of the EFM32G.

2.1.6 Energy Management Unit (EMU)

The Energy Management Unit (EMU) manage all the low energy modes (EM) in EFM32G microcontrollers. Each energy mode manages if the CPU and the various peripherals are available. The EMU can also be used to turn off the power to unused SRAM blocks.

2.1.7 Clock Management Unit (CMU)

The Clock Management Unit (CMU) is responsible for controlling the oscillators and clocks on-board the EFM32G. The CMU provides the capability to turn on and off the clock on an individual basis to all peripheral modules in addition to enable/disable and configure the available oscillators. The high degree of flexibility enables software to minimize energy consumption in any specific application by not wasting power on peripherals and oscillators that are inactive.

2.1.8 Watchdog (WDOG)

The purpose of the watchdog timer is to generate a reset in case of a system failure, to increase application reliability. The failure may e.g. be caused by an external event, such as an ESD pulse, or by a software failure.

2.1.9 Peripheral Reflex System (PRS)

The Peripheral Reflex System (PRS) system is a network which lets the different peripheral module communicate directly with each other without involving the CPU. Peripheral modules which send out Reflex signals are called producers. The PRS routes these reflex signals to consumer peripherals which apply actions depending on the data received. The format for the Reflex signals is not given, but edge triggers and other functionality can be applied by the PRS.

2.1.10 External Bus Interface (EBI)

The External Bus Interface provides access to external parallel interface devices such as SRAM, FLASH, ADCs and LCDs. The interface is memory mapped into the address bus of the Cortex-M3. This enables seamless access from software without manually manipulating the IO settings each time a read or write is performed. The data and address lines are multiplexed in order to reduce the number of pins required to interface the external devices. The timing is adjustable to meet specifications of the external devices. The interface is limited to asynchronous devices.

2.1.11 Inter-Integrated Circuit Interface (I2C)

The I^2C module provides an interface between the MCU and a serial I^2C-bus. It is capable of acting as both a master and a slave, and supports multi-master buses. Both standard-mode, fast-mode and fast-mode plus speeds are supported, allowing transmission rates all the way from 10 kbit/s up to 1 Mbit/s.

Slave arbitration and timeouts are also provided to allow implementation of an SMBus compliant system. The interface provided to software by the I^2C module, allows both fine-grained control of the transmission process and close to automatic transfers. Automatic recognition of slave addresses is provided in all energy modes.

2.1.12 Universal Synchronous/Asynchronous Receiver/Transmitter (USART)

The Universal Synchronous Asynchronous serial Receiver and Transmitter (USART) is a very flexible serial I/O module. It supports full duplex asynchronous UART communication as well as RS-485, SPI, MicroWire and 3-wire. It can also interface with ISO7816 SmartCards and IrDA devices.

2.1.13 Pre-Programmed Serial Bootloader

The bootloader presented in application note AN0003 is pre-programmed in the device at factory. Auto-baud and destructive write are supported. The autobaud feature, interface and commands are described further in the application note.

2.1.14 Universal Asynchronous Receiver/Transmitter (UART)

The Universal Asynchronous serial Receiver and Transmitter (UART) is a very flexible serial I/O module. It supports full- and half-duplex asynchronous UART communication.

2.1.15 Low Energy Universal Asynchronous Receiver/Transmitter (LEUART)

The unique LEUART™, the Low Energy UART, is a UART that allows two-way UART communication on a strict power budget. Only a 32.768 kHz clock is needed to allow UART communication up to 9600 baud/s. The LEUART includes all necessary hardware support to make asynchronous serial communication possible with minimum of software intervention and energy consumption.

2.1.16 Timer/Counter (TIMER)

The 16-bit general purpose Timer has 3 compare/capture channels for input capture and compare/Pulse-Width Modulation (PWM) output. TIMER0 also includes a Dead-Time Insertion module suitable for motor control applications.

2.1.17 Real Time Counter (RTC)

The Real Time Counter (RTC) contains a 24-bit counter and is clocked either by a 32.768 kHz crystal oscillator, or a 32 kHz RC oscillator. In addition to energy modes EM0 and EM1, the RTC is also available in EM2. This makes it ideal for keeping track of time since the RTC is enabled in EM2 where most of the device is powered down.

2.1.18 Low Energy Timer (LETIMER)

The unique LETIMER™, the Low Energy Timer, is a 16-bit timer that is available in energy mode EM2 in addition to EM1 and EM0. Because of this, it can be used for timing and output generation when most of the device is powered down, allowing simple tasks to be performed while the power consumption of the system is kept at an absolute minimum. The LETIMER can be used to output a variety of waveforms with minimal software intervention. It is also connected to the Real Time Counter (RTC), and can be configured to start counting on compare matches from the RTC.

2.1.19 Pulse Counter (PCNT)

The Pulse Counter (PCNT) can be used for counting pulses on a single input or to decode quadrature encoded inputs. It runs off either the internal LFACLK or the PCNTn_S0IN pin as external clock source. The module may operate in energy mode EM0 – EM3.

2.1.20 Analog Comparator (ACMP)

The Analog Comparator is used to compare the voltage of two analog inputs, with a digital output indicating which input voltage is higher. Inputs can either be one of the selectable internal references or from external pins. Response time and thereby also the current consumption can be configured by altering the current supply to the comparator.

2.1.21 Voltage Comparator (VCMP)

The Voltage Supply Comparator is used to monitor the supply voltage from software. An interrupt can be generated when the supply falls below or rises above a programmable threshold. Response time and thereby also the current consumption can be configured by altering the current supply to the comparator.

2.1.22 Analog to Digital Converter (ADC)

The ADC is a Successive Approximation Register (SAR) architecture, with a resolution of up to 12 bits at up to one million samples per second. The integrated input mux can select inputs from 8 external pins and 6 internal signals.

2.1.23 Digital to Analog Converter (DAC)

The Digital to Analog Converter (DAC) can convert a digital value to an analog output voltage. The DAC is fully differential rail-to-rail, with 12-bit resolution. It has two single ended output buffers which can be combined into one differential output. The DAC may be used for a number of different applications such as sensor interfaces or sound output.

2.1.24 Advanced Encryption Standard Accelerator (AES)

The AES accelerator performs AES encryption and decryption with 128-bit or 256-bit keys. Encrypting or decrypting one 128-bit data block takes 52 HFCORECLK cycles with 128-bit keys and 75 HFCORECLK cycles with 256-bit keys. The AES module is an AHB slave which enables efficient access to the data and key registers. All write accesses to the AES module must be 32-bit operations, i.e. 8- or 16-bit operations are not supported.

2.1.25 General Purpose Input/Output (GPIO)

In the EFM32G290, there are 90 General Purpose Input/Output (GPIO) pins, which are divided into ports with up to 16 pins each. These pins can individually be configured as either an output or input. More advances configurations like open-drain, filtering and drive strength can also be configured individually for the pins. The GPIO pins can also be overridden by peripheral pin connections, like Timer PWM outputs or USART communication, which can be routed to several locations on the device. The GPIO supports up to 16 asynchronous external pin interrupts, which enables interrupts from any pin on the device. Also, the input value of a pin can be routed through the Peripheral Reflex System to other peripherals.

2.2 Configuration Summary

The features of the EFM32G290 is a subset of the feature set described in the EFM32G Reference Manual. Table 2.1 (p. 6) describes device specific implementation of the features.

Table 2.1. Configuration Summary

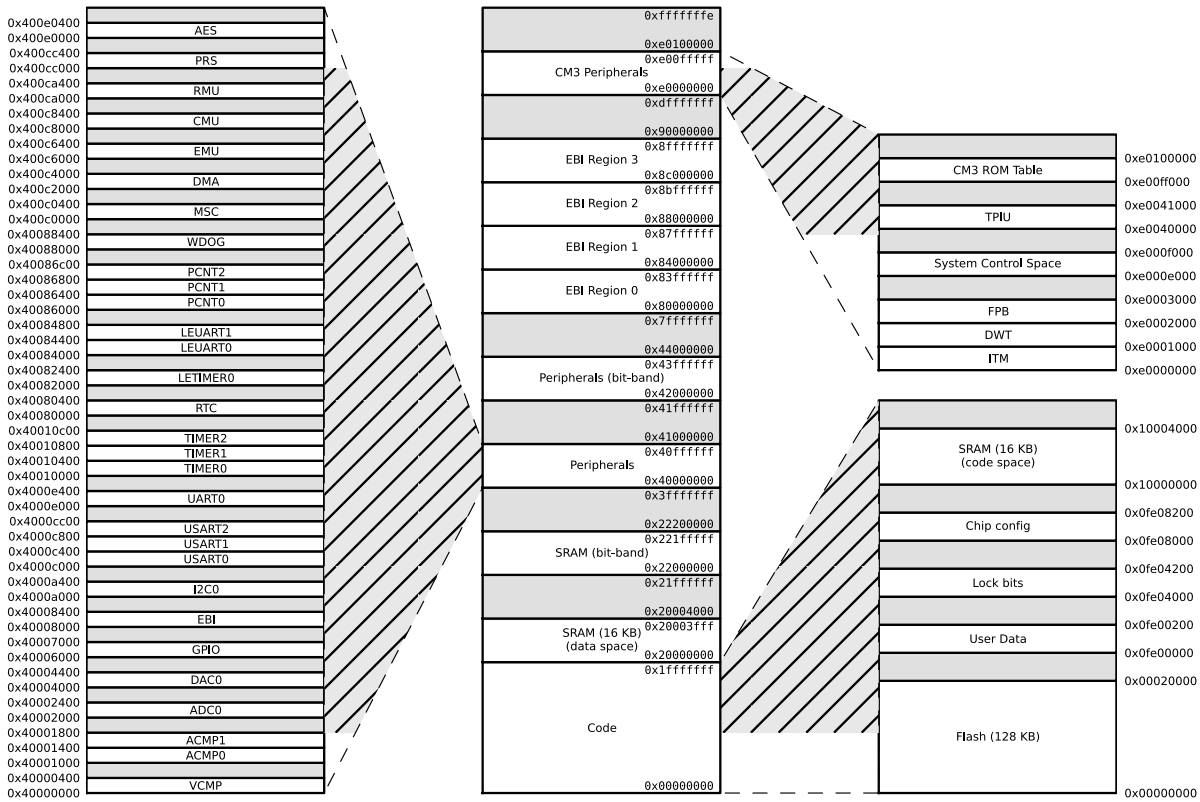
Module	Configuration	Pin Connections
Cortex-M3	Full configuration	NA

Module	Configuration	Pin Connections
DBG	Full configuration	DBG_SWCLK, DBG_SWDIO, DBG_SWO
MSC	Full configuration	NA
DMA	Full configuration	NA
RMU	Full configuration	NA
EMU	Full configuration	NA
CMU	Full configuration	CMU_OUT0, CMU_OUT1
WDOG	Full configuration	NA
PRS	Full configuration	NA
EBI	Full configuration	
I2C0	Full configuration	I2C0_SDA, I2C0_SCL
USART0	IrDA	US0_TX, US0_RX. US0_CLK, US0_CS
USART1		US1_TX, US1_RX, US1_CLK, US1_CS
USART2		US2_TX, US2_RX, US2_CLK, US2_CS
UART0	Full configuration	U0_TX, U0_RX
LEUART0	Full configuration	LEU0_TX, LEU0_RX
LEUART1	Full configuration	LEU1_TX, LEU1_RX
TIMER0	Full configuration with DTI.	TIM0_CC[2:0], TIM0_CDTI[2:0]
TIMER1	Full configuration	TIM1_CC[2:0]
TIMER2	Full configuration	TIM2_CC[2:0]
RTC	Full configuration	NA
LETIMER0	Full configuration	LET0_O[1:0]
PCNT0	8-bit count register	PCNT0_S[1:0]
PCNT1	8-bit count register	PCNT1_S[1:0]
PCNT2	8-bit count register	PCNT2_S[1:0]
ACMP0	Full configuration	ACMP0_CH[7:0], ACMP0_O
ACMP1	Full configuration	ACMP1_CH[7:0], ACMP1_O
VCMP	Full configuration	NA
ADC0	Full configuration	ADC0_CH[7:0]
DAC0	Full configuration	DAC0_OUT[1:0]
AES	Full configuration	NA
GPIO	90 pins	Available pins are shown in Table 4.3 (p. 54)

2.3 Memory Map

The *EFM32G290* memory map is shown in Figure 2.2 (p. 8), with RAM and Flash sizes for the largest memory configuration.

Figure 2.2. EFM32G290 Memory Map with largest RAM and Flash sizes



3 Electrical Characteristics

3.1 Test Conditions

3.1.1 Typical Values

The typical data are based on T_{AMB}=25°C and V_{DD}=3.0 V, as defined in Table 3.2 (p. 9), by simulation and/or technology characterisation unless otherwise specified.

3.1.2 Minimum and Maximum Values

The minimum and maximum values represent the worst conditions of ambient temperature, supply voltage and frequencies, as defined in Table 3.2 (p. 9), by simulation and/or technology characterisation unless otherwise specified.

3.2 Absolute Maximum Ratings

The absolute maximum ratings are stress ratings, and functional operation under such conditions are not guaranteed. Stress beyond the limits specified in Table 3.1 (p. 9) may affect the device reliability or cause permanent damage to the device. Functional operating conditions are given in Table 3.2 (p. 9) .

Table 3.1. Absolute Maximum Ratings

Symbol	Parameter	Condition	Min	Typ	Max	Unit
T_{STG}	Storage temperature range		-40		150[1]	°C
T_S	Maximum soldering temperature	Latest IPC/JEDEC J-STD-020 Standard			260	°C
V_{DDMAX}	External main supply voltage		0		3.8	V
V_{IOPIN}	Voltage on any I/O pin		-0.3		V_{DD}+0.3	V

[1]Based on programmed devices tested for 10000 hours at 150°C. Storage temperature affects retention of preprogrammed calibration values stored in flash. Please refer to the Flash section in the Electrical Characteristics for information on flash data retention for different temperatures.

3.3 General Operating Conditions

3.3.1 General Operating Conditions

Table 3.2. General Operating Conditions

Symbol	Parameter	Min	Typ	Max	Unit
T_{AMB}	Ambient temperature range	-40		85	°C
V_{DDOP}	Operating supply voltage	1.85		3.8	V
f_{APB}	Internal APB clock frequency			32	MHz
f_{AHB}	Internal AHB clock frequency			32	MHz

3.3.2 Environmental

Table 3.3. Environmental

Symbol	Parameter	Condition	Min	Typ	Max	Unit
V_{ESDHBM}	ESD (Human Body Model HBM)	T_{AMB}=25°C			2	kV
V_{ESDCDM}	ESD (Charged Device Model, CDM)	T_{AMB}=25°C			1	kV

Latch-up sensitivity test passed level A according to JEDEC JESD 78B method Class II, 85°C.

3.4 Current Consumption

Table 3.4. Current Consumption

Symbol	Parameter	Condition	Min	Typ	Max	Unit
I_{EM0}	EM0 current. No prescaling. Running prime number calculation code from Flash.	32 MHz HFXO, all peripheral clocks disabled, V_{DD}= 3.0 V		180		µA/MHz
		28 MHz HFRCO, all peripheral clocks disabled, V_{DD}= 3.0 V		181	235	µA/MHz
		21 MHz HFRCO, all peripheral clocks disabled, V_{DD}= 3.0 V		183	237	µA/MHz
		14 MHz HFRCO, all peripheral clocks disabled, V_{DD}= 3.0 V		185	243	µA/MHz
		11 MHz HFRCO, all peripheral clocks disabled, V_{DD}= 3.0 V		186	246	µA/MHz
		7 MHz HFRCO, all peripheral clocks disabled, V_{DD}= 3.0 V		191	257	µA/MHz
		1 MHz HFRCO, all peripheral clocks disabled, V_{DD}= 3.0 V		220		µA/MHz
I_{EM1}	EM1 current	32 MHz HFXO, all peripheral clocks disabled, V_{DD}= 3.0 V		45		µA/MHz
		28 MHz HFRCO, all peripheral clocks disabled, V_{DD}= 3.0 V		47	62	µA/MHz
		21 MHz HFRCO, all peripheral clocks disabled, V_{DD}= 3.0 V		48	64	µA/MHz
		14 MHz HFRCO, all peripheral clocks disabled, V_{DD}= 3.0 V		50	69	µA/MHz
		11 MHz HFRCO, all peripheral clocks disabled, V_{DD}= 3.0 V		51	72	µA/MHz
		7 MHz HFRCO, all peripheral clocks disabled, V_{DD}= 3.0 V		56	83	µA/MHz
		1 MHz HFRCO. all peripheral clocks disabled, V_{DD}= 3.0 V		103		µA/MHz
I_{EM2}	EM2 current	EM2 current with RTC at 1 Hz, RTC prescaled to 1kHz, 32 kHz LFRCO, V_{DD}= 3.0 V, T_{AMB}=25°C		0.9		µA
		EM2 current with RTC at 1 Hz, RTC prescaled to 1kHz, 32 kHz LFRCO, V_{DD}= 3.0 V, T_{AMB}=85°C		3.0	6.0	µA
I_{EM3}	EM3 current	V_{DD}= 3.0 V, T_{AMB}=25°C		0.59		µA
		V_{DD}= 3.0 V, T_{AMB}=85°C		2.75	5.8	µA
I_{EM4}	EM4 current	V_{DD}= 3.0 V, T_{AMB}=25°C		0.02		µA
		V_{DD}= 3.0 V, T_{AMB}=85°C		0.25	0.7	µA

Figure 3.1. EM0 Current consumption while executing prime number calculation code from flash with HFRCO running at 28MHz

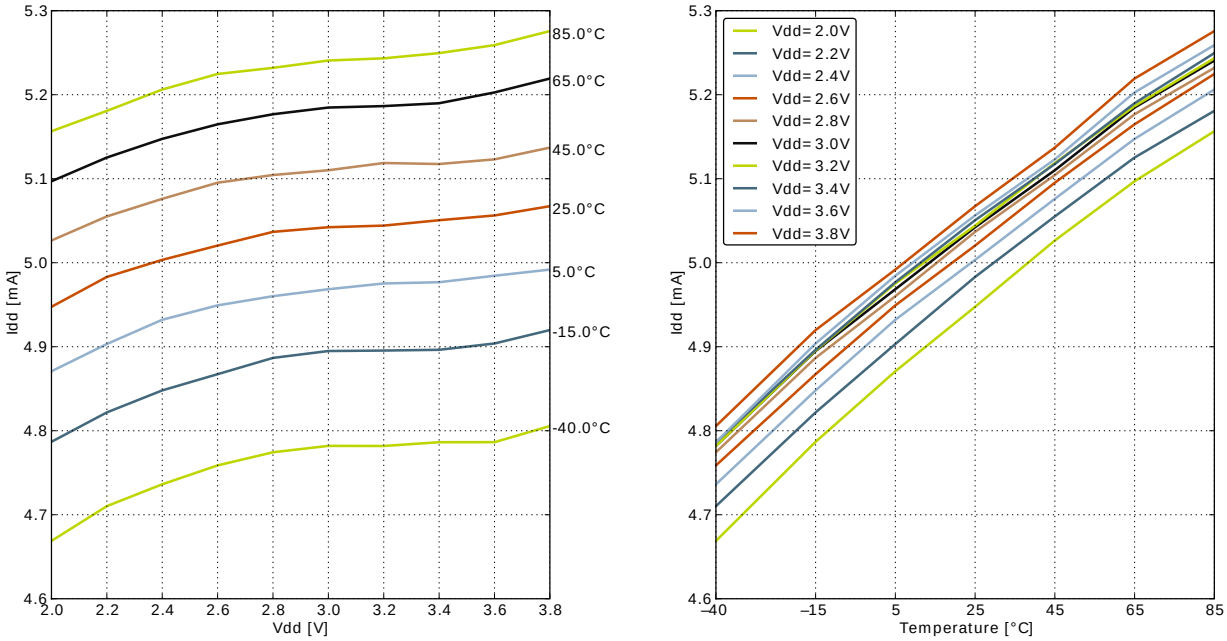


Figure 3.2. EM0 Current consumption while executing prime number calculation code from flash with HFRCO running at 21MHz

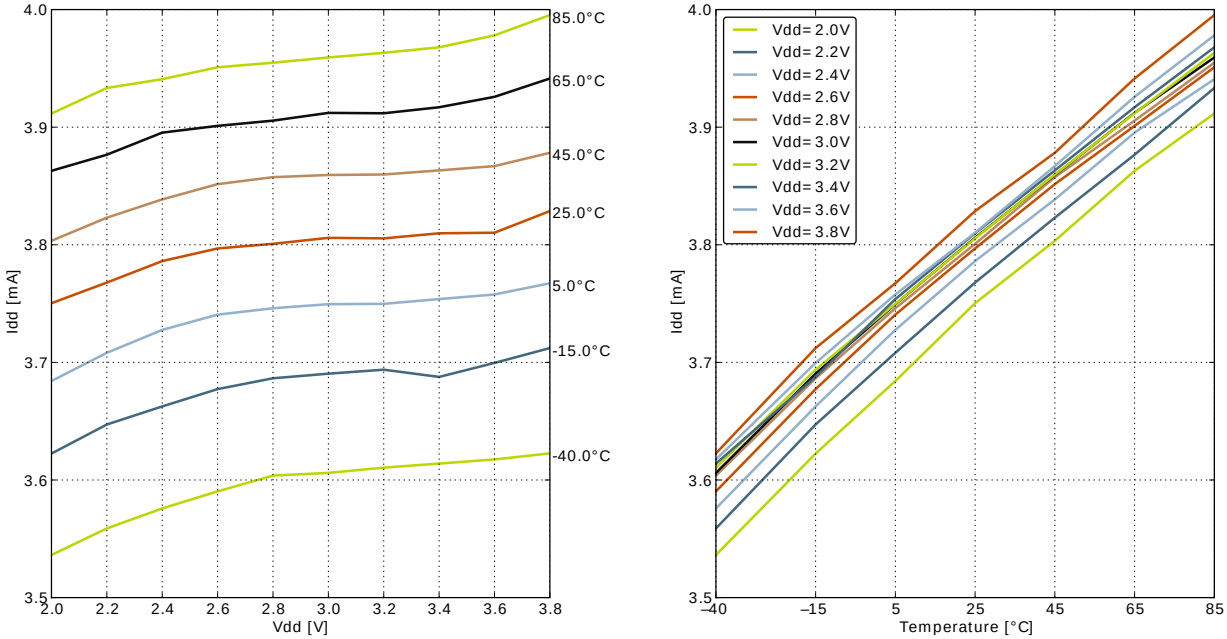


Figure 3.3. EM0 Current consumption while executing prime number calculation code from flash with HFRCO running at 14MHz

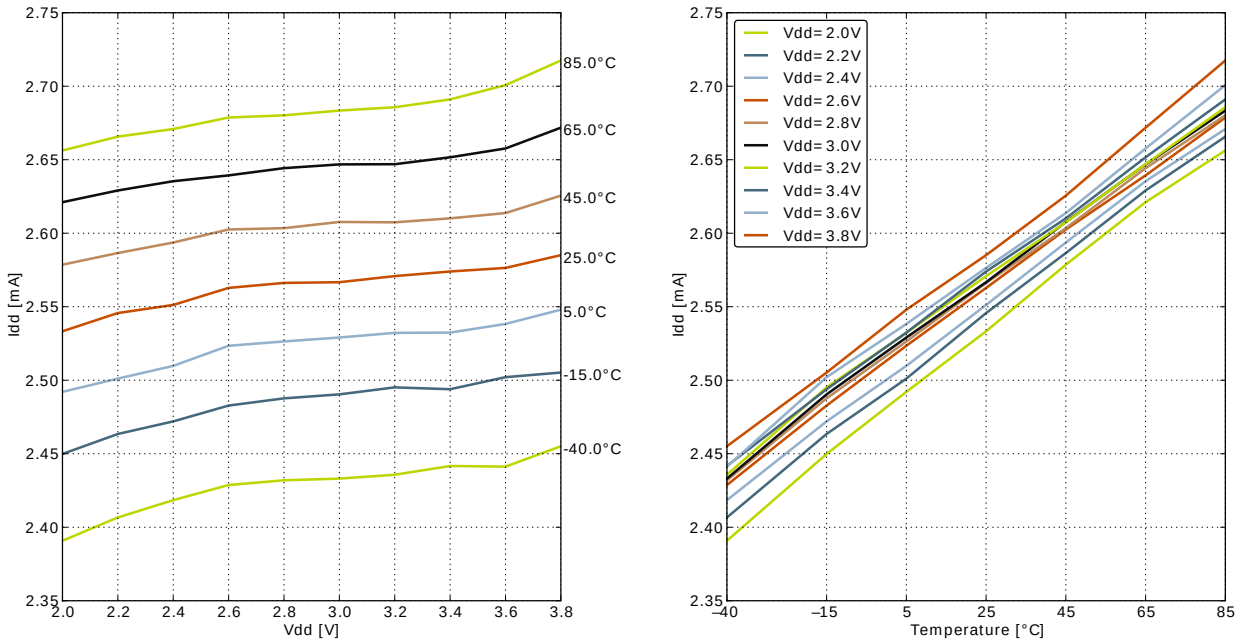


Figure 3.4. EM0 Current consumption while executing prime number calculation code from flash with HFRCO running at 11MHz

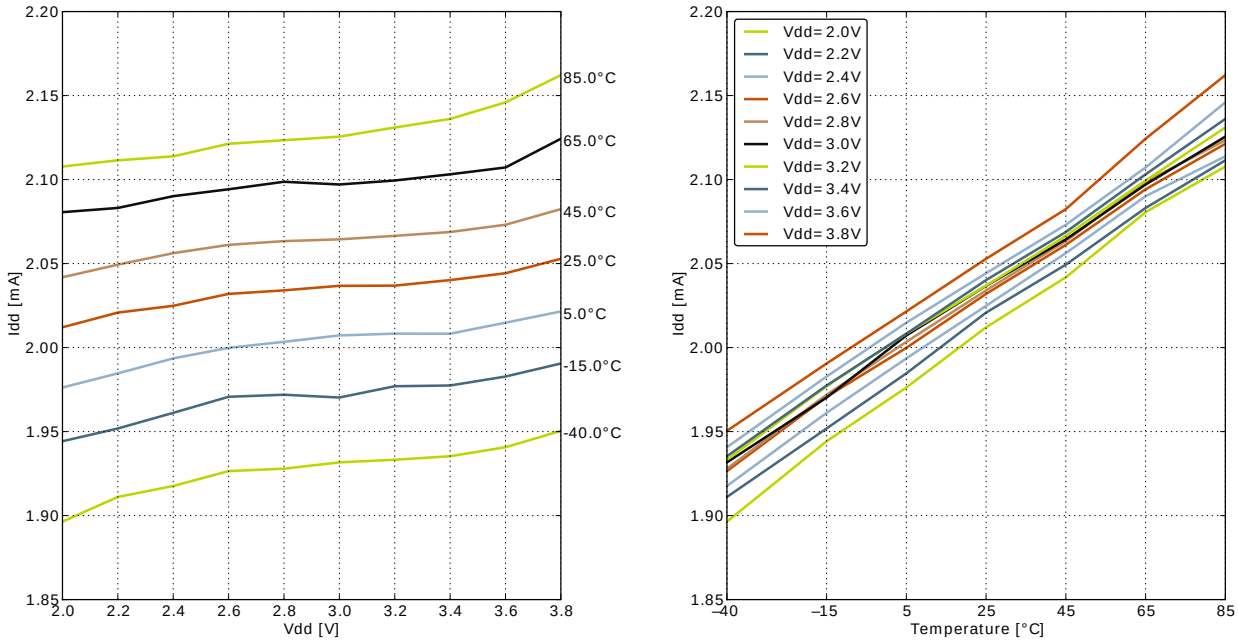


Figure 3.5. EM0 Current consumption while executing prime number calculation code from flash with HFRCO running at 7MHz

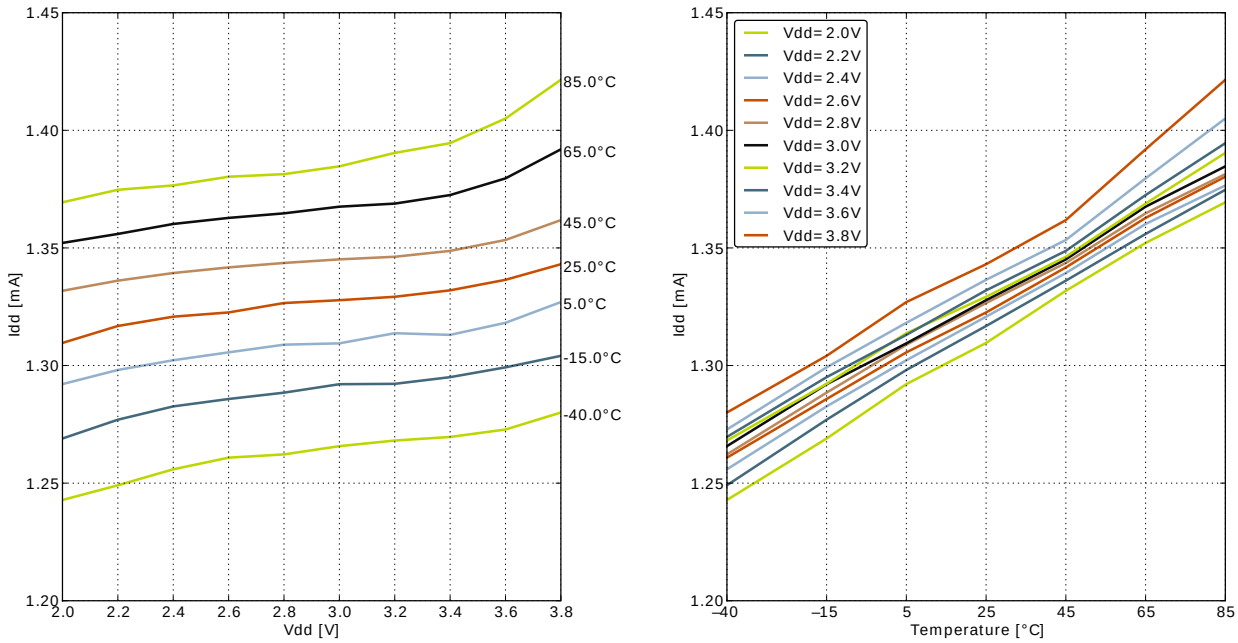


Figure 3.6. EM1 Current consumption with all peripheral clocks disabled and HFRCO running at 28MHz

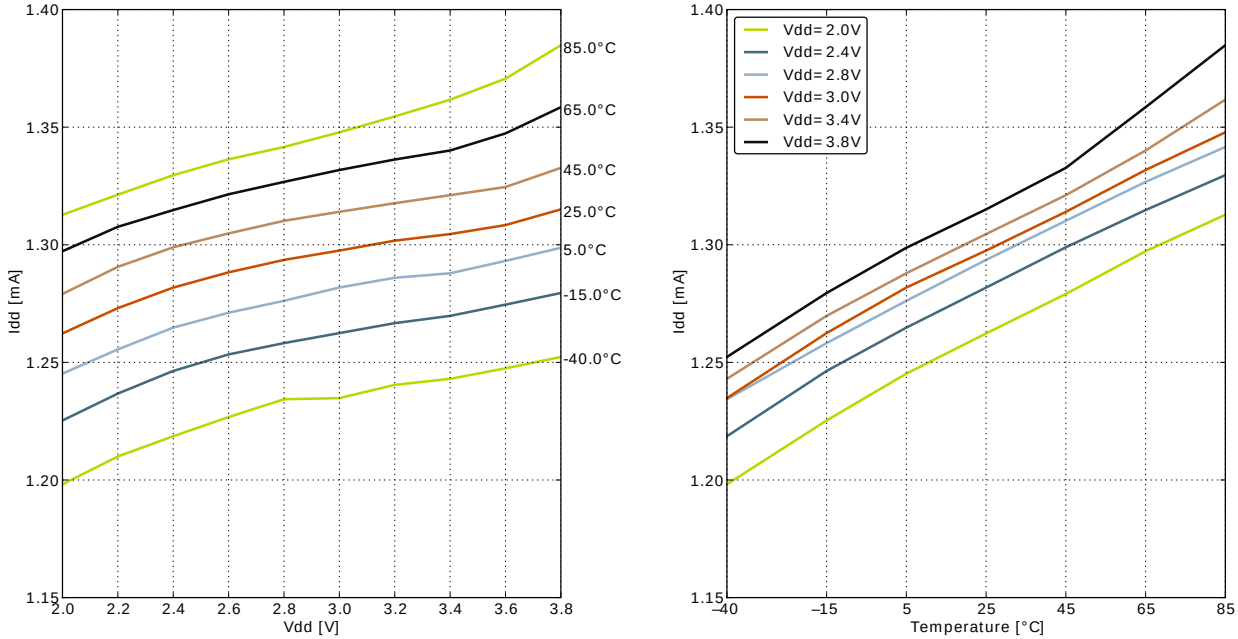


Figure 3.7. EM1 Current consumption with all peripheral clocks disabled and HFRCO running at 21MHz

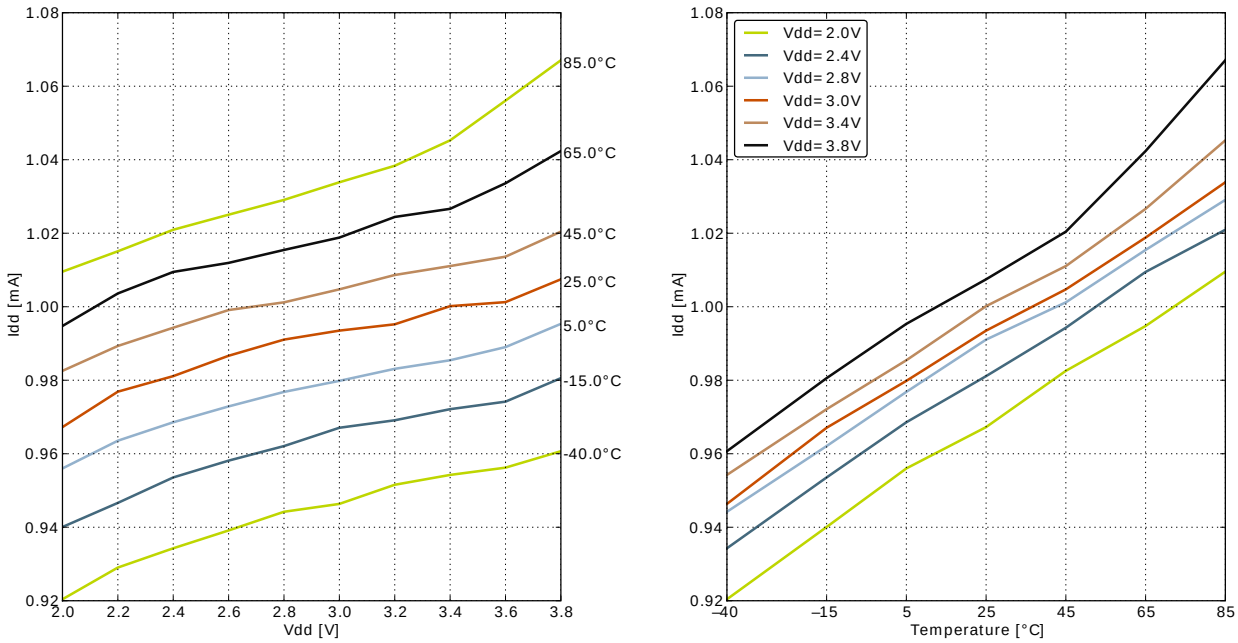


Figure 3.8. EM1 Current consumption with all peripheral clocks disabled and HFRCO running at 14MHz

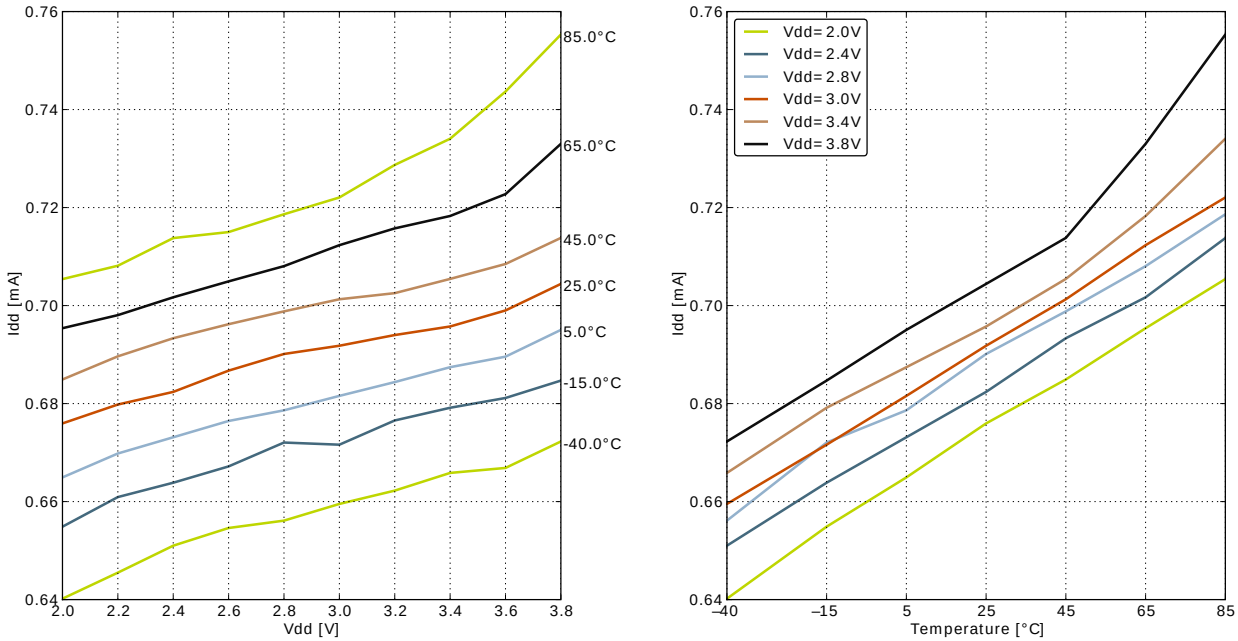


Figure 3.9. EM1 Current consumption with all peripheral clocks disabled and HFRCO running at 11MHz

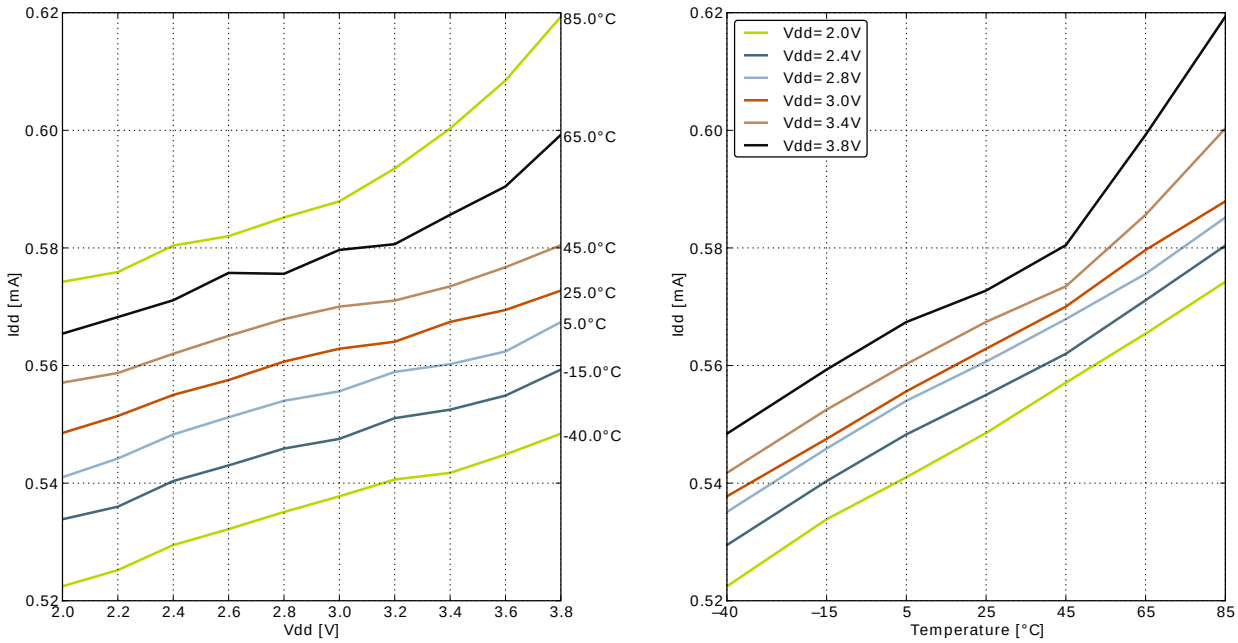


Figure 3.10. EM1 Current consumption with all peripheral clocks disabled and HFRCO running at 7MHz

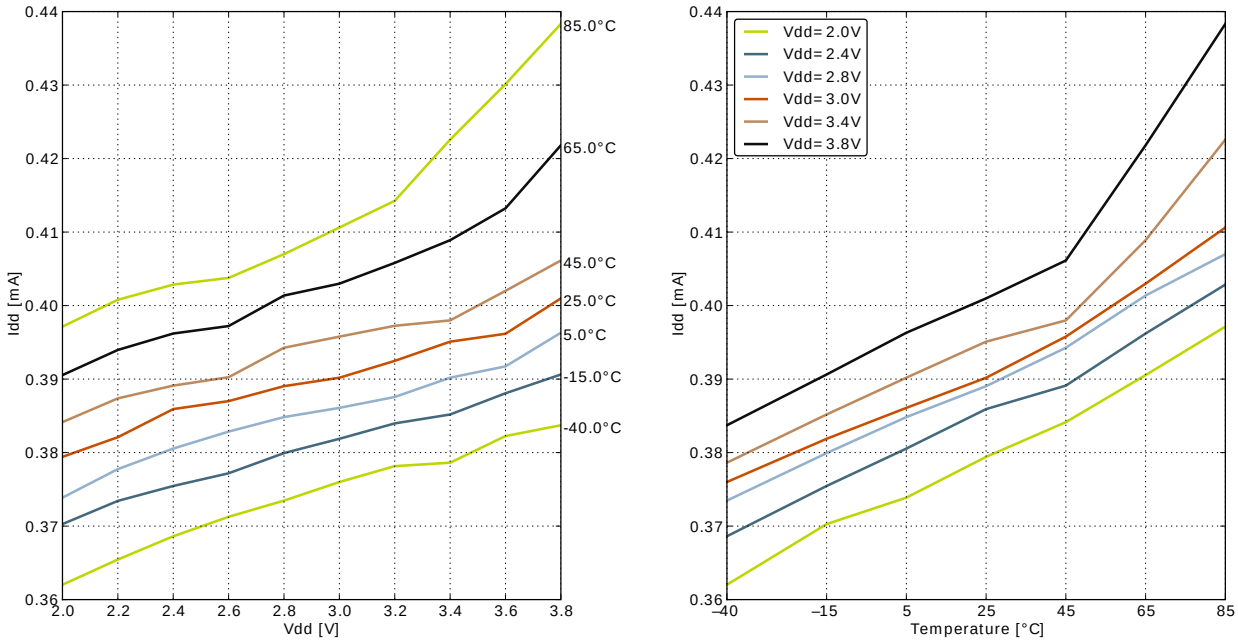


Figure 3.11. EM2 current consumption. RTC prescaled to 1kHz, 32 kHz LFRCO.

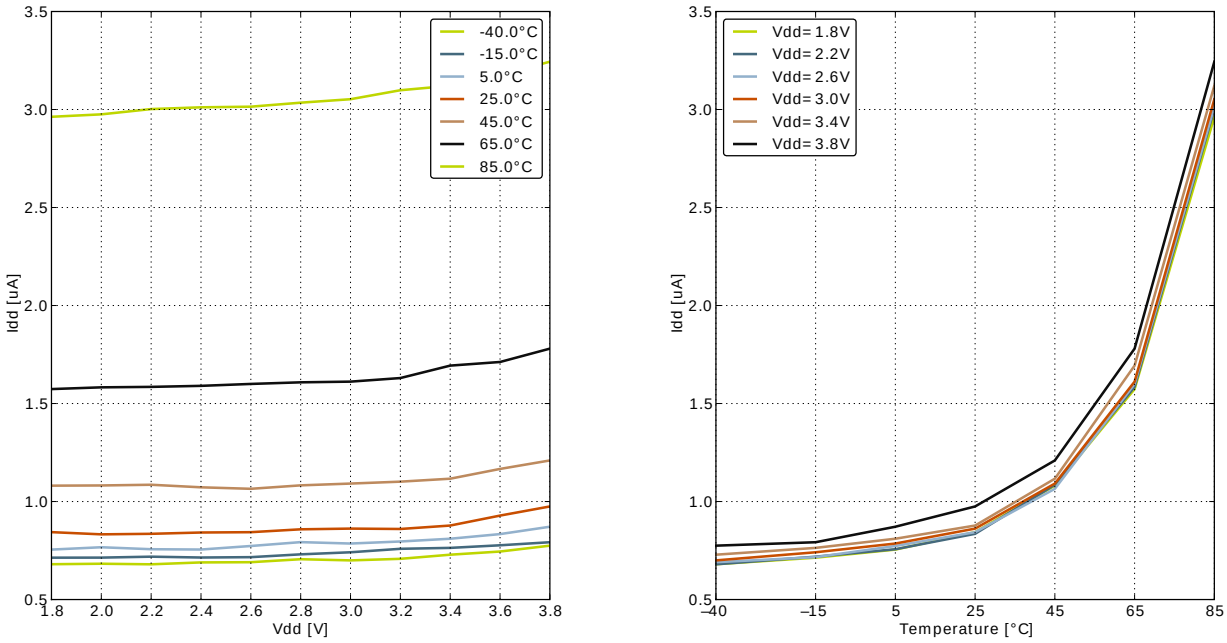


Figure 3.12. EM3 current consumption.

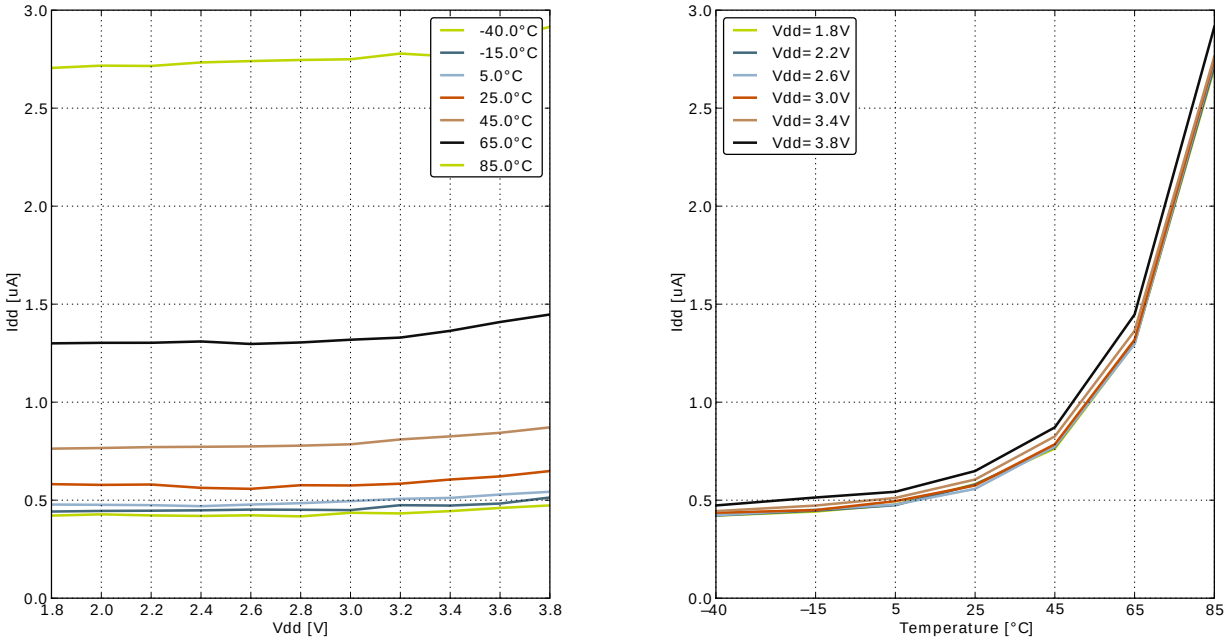
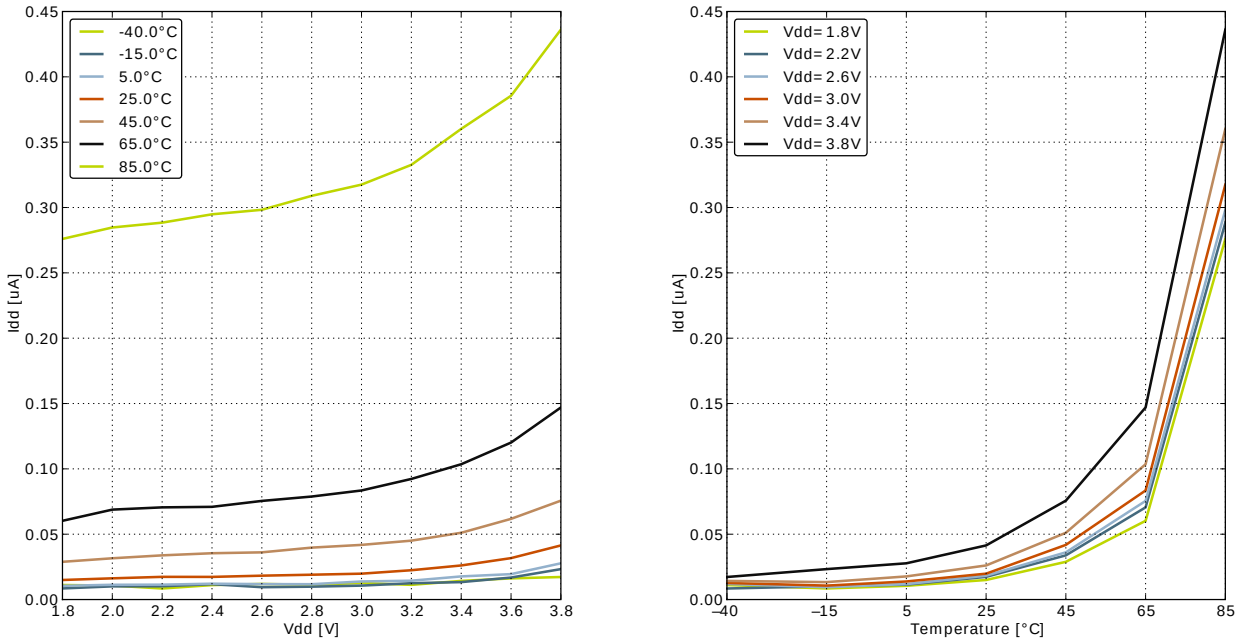


Figure 3.13. EM4 current consumption.



3.5 Transition between Energy Modes

Table 3.5. Energy Modes Transitions

Symbol	Parameter	Min	Typ	Max	Unit
t_{EM10}	Transition time from EM1 to EM0		0[1]		HF core CLK cycles
t_{EM20}	Transition time from EM2 to EM0		2		µs
t_{EM30}	Transition time from EM3 to EM0		2		µs
t_{EM40}	Transition time from EM4 to EM0		163		µs

[1]Core wakeup time only.

3.6 Power Management

This EFM32G device requires the power to be applied to the AVDD_x pins before or at the same time as power is applied to the VDD_DREG and IOVDD_x pins. In addition, it is also a requirement that all the power pins are powered with the same voltage level. For practical schematic recommendations to fulfil this requirement, please see the application note, "AN0002 EFM32 Hardware Design Considerations".

Table 3.6. Power Management

Symbol	Parameter	Condition	Min	Typ	Max	Unit
$V_{BODextthr-}$	BOD threshold on falling external supply voltage		1.82		1.85	V
$V_{BODintthr-}$	BOD threshold on falling internally regulated supply voltage		1.62		1.68	V
$V_{BODextthr+}$	BOD threshold on rising external supply voltage			1.85		V
$V_{PORthr+}$	Power-on Reset (POR) threshold on rising external supply voltage				1.98	V
$t_{RESETdly}$	Delay from reset is released until program execution starts	Applies to Power-on Reset, Brown-out Reset and pin reset.		163		µs
t_{RESET}	negative pulse length to ensure complete reset of device		50			ns
$C_{DECOUPLE}$	Voltage regulator decoupling capacitor.	X5R capacitor recommended. Apply between DECOUPLE pin and GROUND		1		µF

3.7 Flash

Table 3.7. Flash

Symbol	Parameter	Condition	Min	Typ	Max	Unit
EC_{FLASH}	Flash erase cycles before failure		20000			cycles
RET_{FLASH}	Flash data retention	T_{AMB}<150°C	10000			h
		T_{AMB}<85°C	10			years
		T_{AMB}<70°C	20			years
t_{W_PROG}	Word (32-bit) programming time		20			µs
t_{P_ERASE}	Page erase time		20	20.4	20.8	ms
t_{D_ERASE}	Device erase time		40	40.8	41.6	ms
I_{ERASE}	Erase current				7[1]	mA
I_{WRITE}	Write current				7[2]	mA
V_{FLASH}	Supply voltage during flash erase and write		1.8		3.8	V

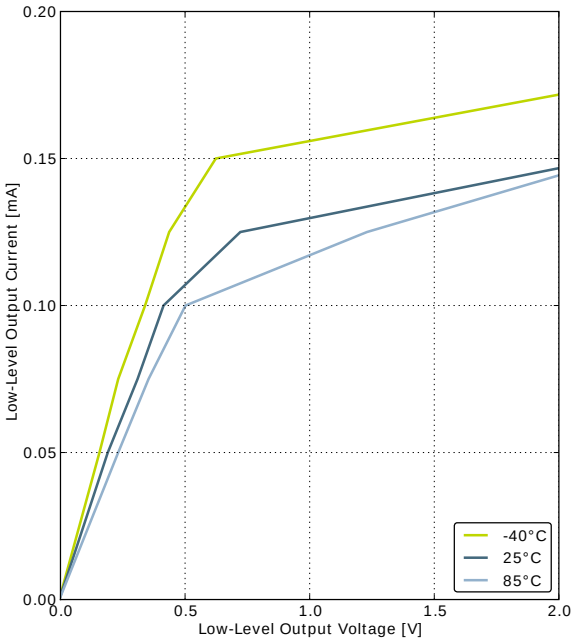
[1]Measured at 25°C
[2]Measured at 25°C

3.8 General Purpose Input Output

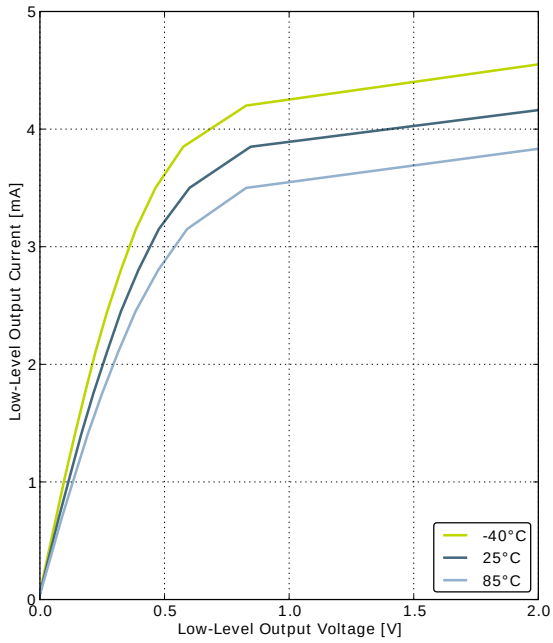
Table 3.8. GPIO

Symbol	Parameter	Condition	Min	Typ	Max	Unit
V_{IOIL}	Input low voltage				0.3V_{DD}	V
V_{IOIH}	Input high voltage		0.7V_{DD}			V
V_{IOOH}	Output high voltage	Sourcing 6 mA, V_{DD}=1.8V, GPIO_Px_CTRL DRIVEMODE = STANDARD	0.75V_{DD}			V
		Sourcing 6 mA, V_{DD}=3.0V, GPIO_Px_CTRL DRIVEMODE = STANDARD	0.95V_{DD}			V
		Sourcing 20 mA, V_{DD}=1.8V, GPIO_Px_CTRL DRIVEMODE = HIGH	0.7V_{DD}			V
		Sourcing 20 mA, V_{DD}=3.0V, GPIO_Px_CTRL DRIVEMODE = HIGH	0.9V_{DD}			V
V_{IOOL}	Output low voltage	Sinking 6 mA, V_{DD}=1.8V, GPIO_Px_CTRL DRIVEMODE = STANDARD			0.25V_{DD}	V
		Sinking 6 mA, V_{DD}=3.0V, GPIO_Px_CTRL DRIVEMODE = STANDARD			0.05V_{DD}	V
		Sinking 20 mA, V_{DD}=1.8V, GPIO_Px_CTRL DRIVEMODE = HIGH			0.3V_{DD}	V
		Sinking 20 mA, V_{DD}=3.0V, GPIO_Px_CTRL DRIVEMODE = HIGH			0.1V_{DD}	V
I_{IOLEAK}	Input leakage current	High Impedance IO connected to GROUND or V_{DD}			+/-25	nA
R_{PU}	I/O pin pull-up resistor			40		kOhm
R_{PD}	I/O pin pull-down resistor			40		kOhm
R_{IOESD}	Internal ESD series resistor			200		Ohm
$t_{IOGLITCH}$	Pulse width of pulses to be removed by the glitch suppression filter		10		50	ns
t_{IOOF}	Output fall time	0.5 mA drive strength and load capacitance C_L=12.5-25pF.	20+0.1C_L		250	ns
		2mA drive strength and load capacitance C_L=350-600pF	20+0.1C_L		250	ns
V_{IOHYST}	I/O pin hysteresis (V_{IOTHR+} - V_{IOTHR-})	V_{DD} = 1.8 - 3.8 V	0.1V_{DD}			V

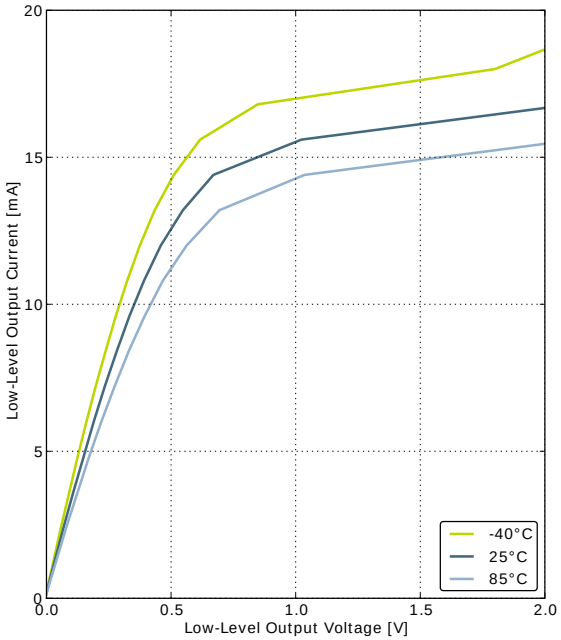
Figure 3.14. Typical Low-Level Output Current, 2V Supply Voltage



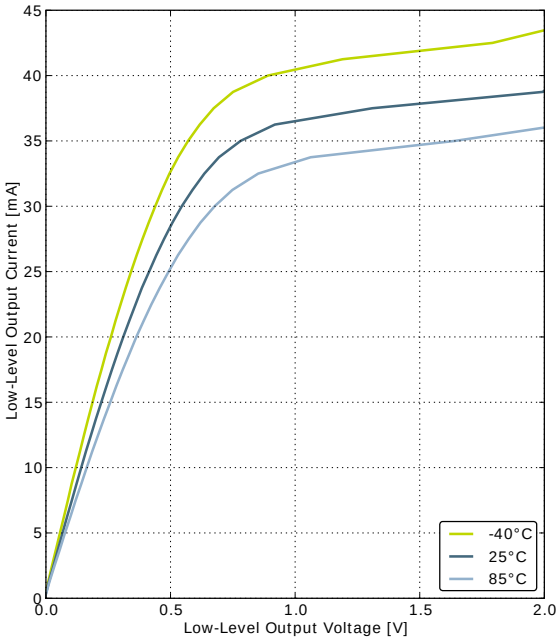
GPIO_Px_CTRL DRIVEMODE = LOWEST



GPIO_Px_CTRL DRIVEMODE = LOW

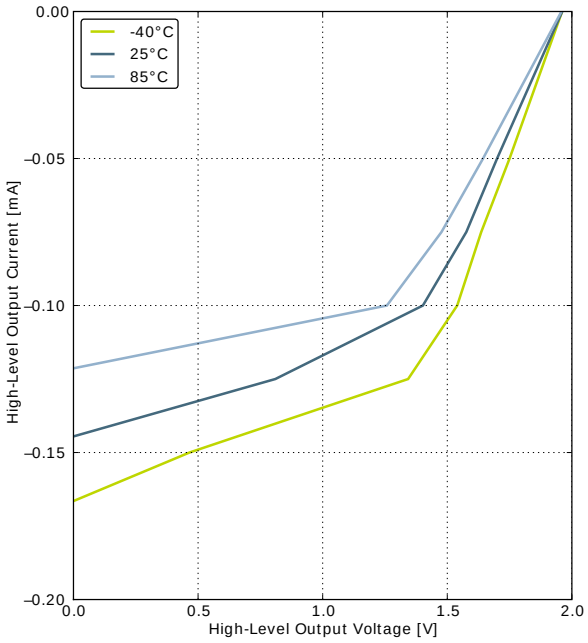


GPIO_Px_CTRL DRIVEMODE = STANDARD

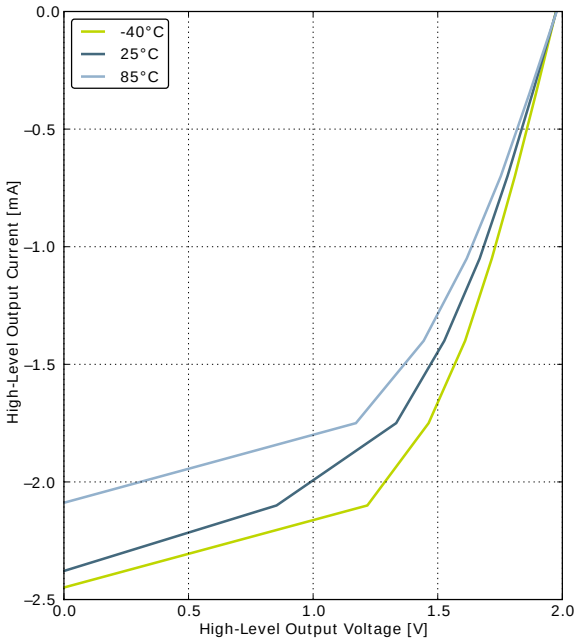


GPIO_Px_CTRL DRIVEMODE = HIGH

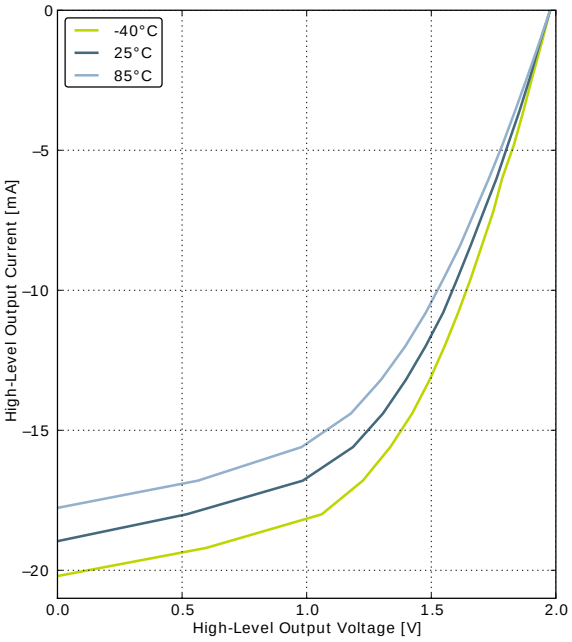
Figure 3.15. Typical High-Level Output Current, 2V Supply Voltage



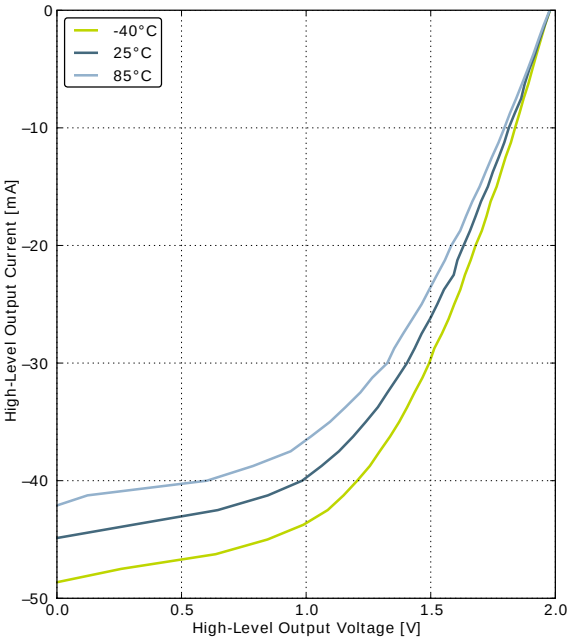
GPIO_Px_CTRL DRIVEMODE = LOWEST



GPIO_Px_CTRL DRIVEMODE = LOW

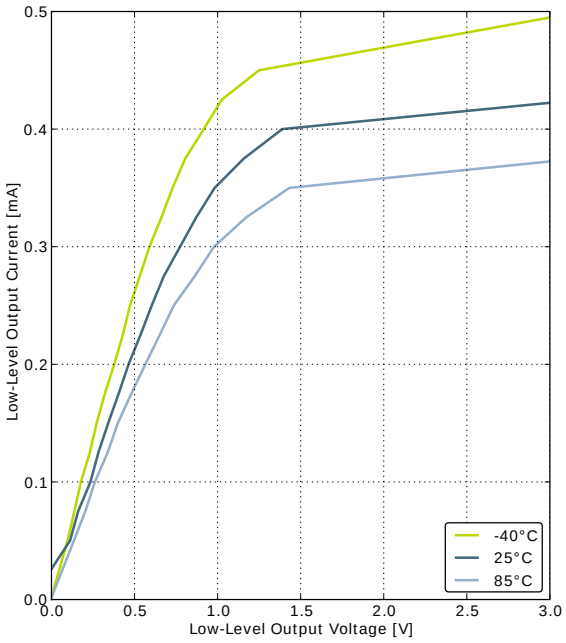


GPIO_Px_CTRL DRIVEMODE = STANDARD

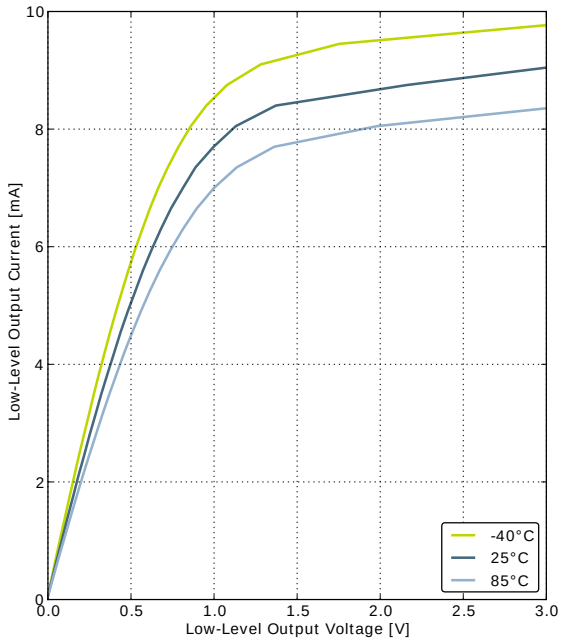


GPIO_Px_CTRL DRIVEMODE = HIGH

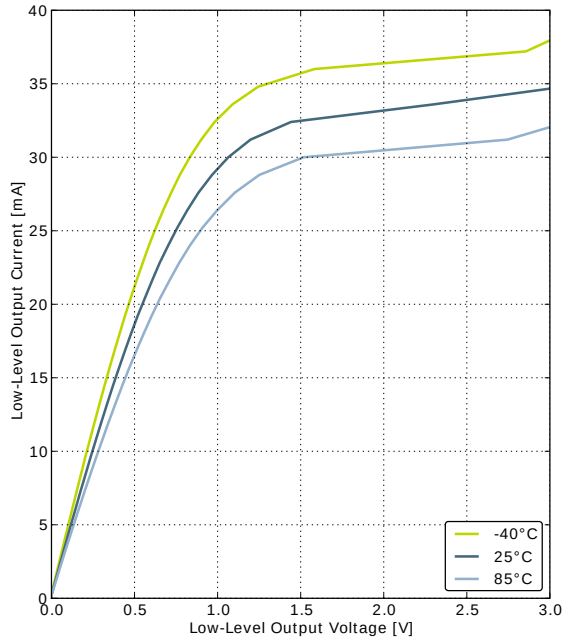
Figure 3.16. Typical Low-Level Output Current, 3V Supply Voltage



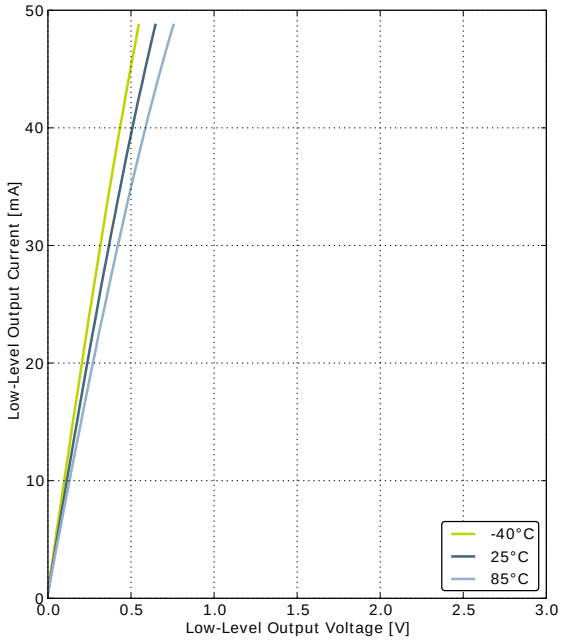
GPIO_Px_CTRL DRIVEMODE = LOWEST



GPIO_Px_CTRL DRIVEMODE = LOW

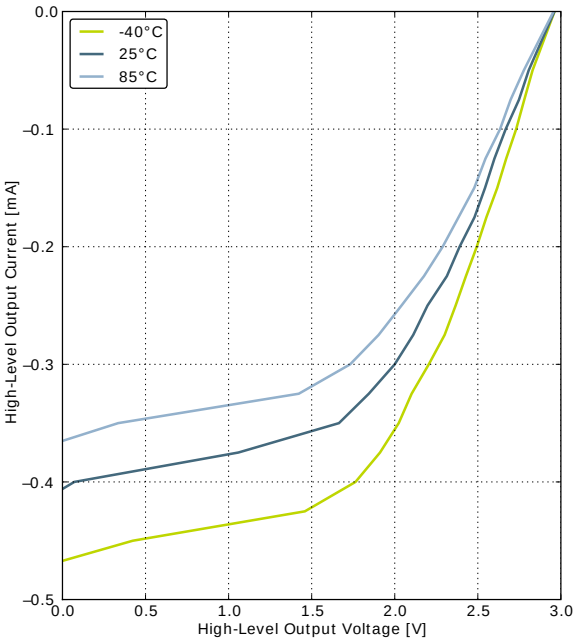


GPIO_Px_CTRL DRIVEMODE = STANDARD

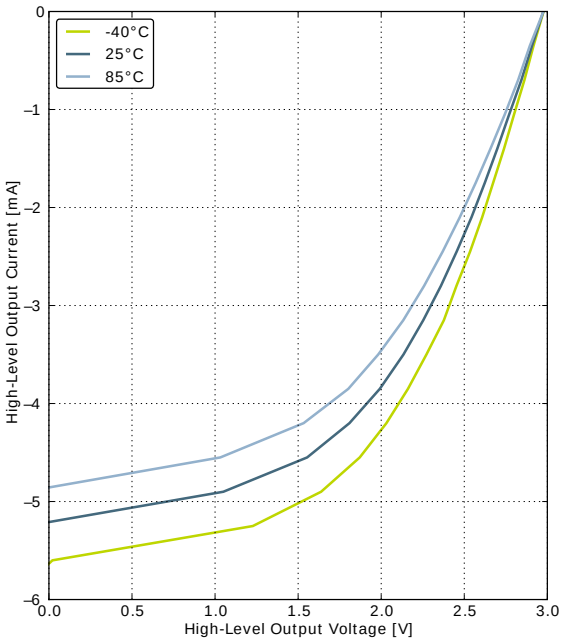


GPIO_Px_CTRL DRIVEMODE = HIGH

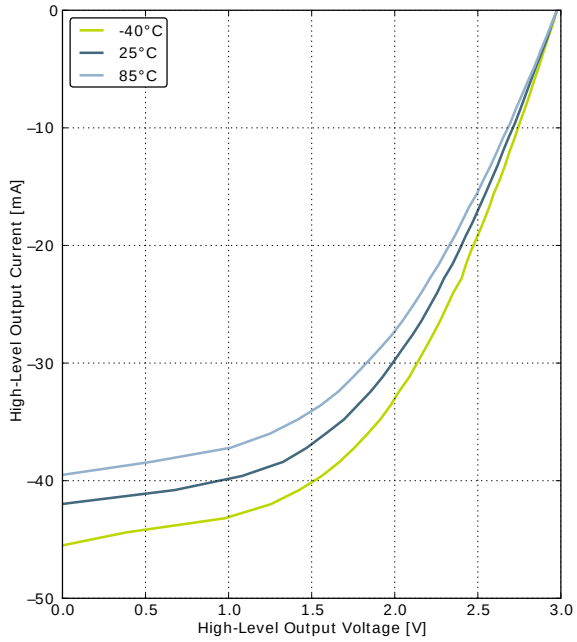
Figure 3.17. Typical High-Level Output Current, 3V Supply Voltage



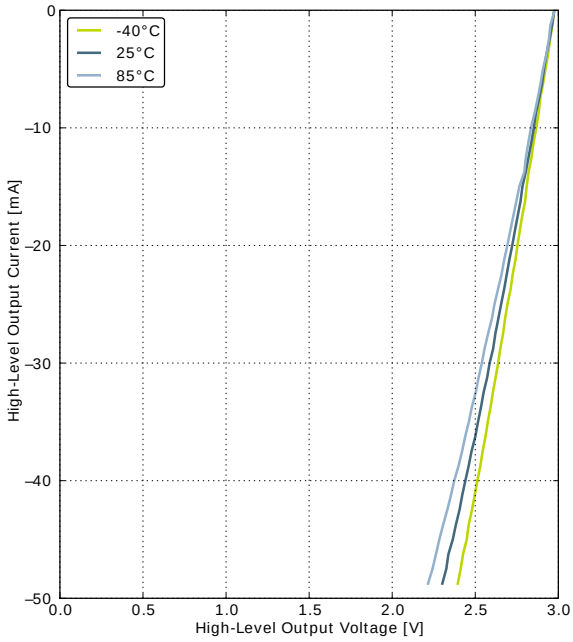
GPIO_Px_CTRL DRIVEMODE = LOWEST



GPIO_Px_CTRL DRIVEMODE = LOW

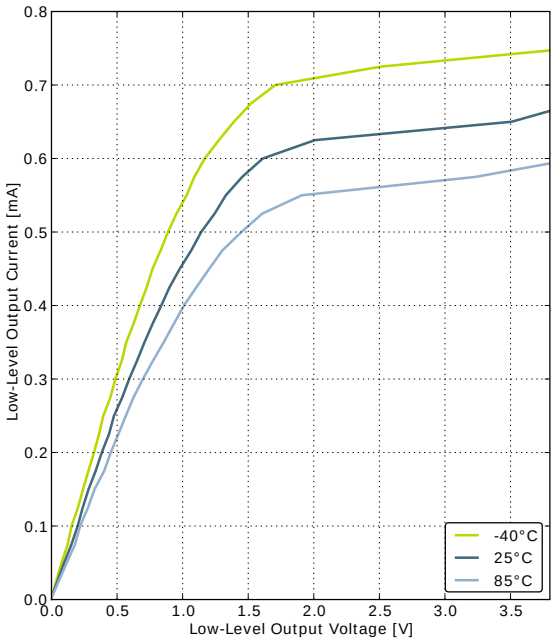


GPIO_Px_CTRL DRIVEMODE = STANDARD

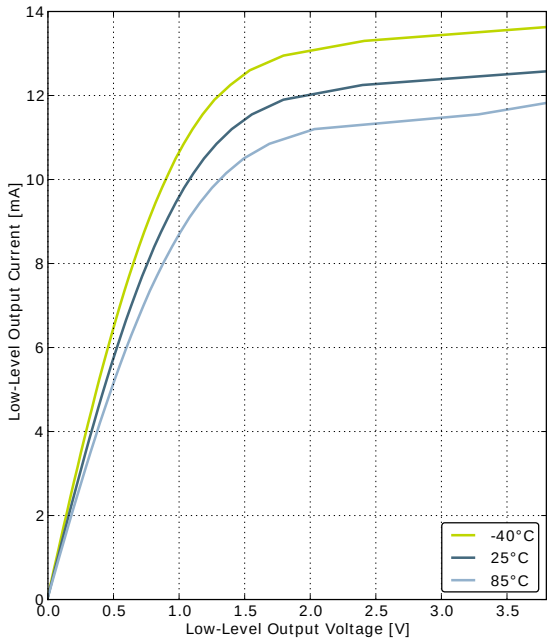


GPIO_Px_CTRL DRIVEMODE = HIGH

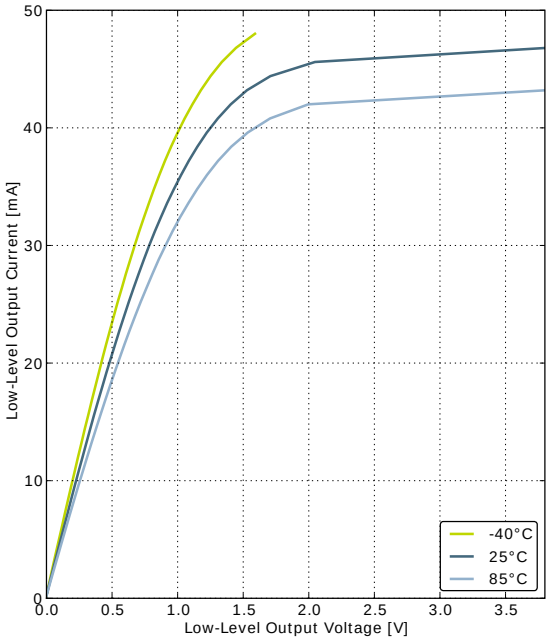
Figure 3.18. Typical Low-Level Output Current, 3.8V Supply Voltage



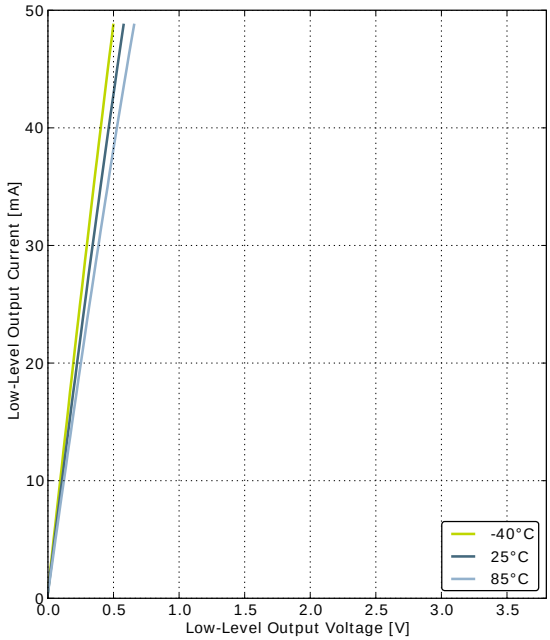
GPIO_Px_CTRL DRIVEMODE = LOWEST



GPIO_Px_CTRL DRIVEMODE = LOW

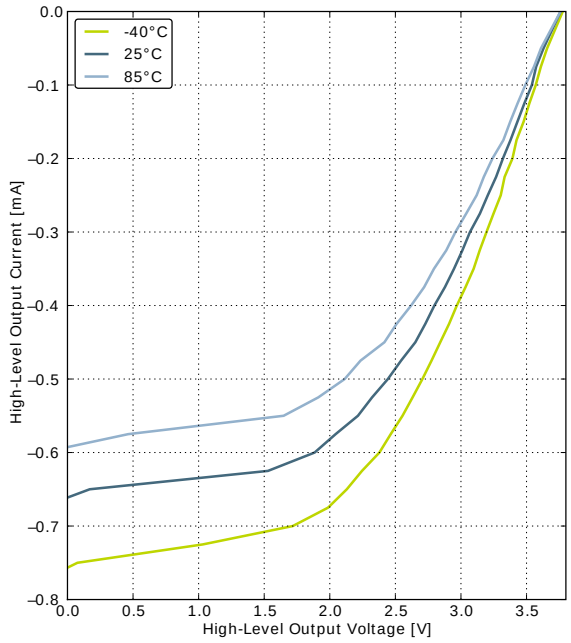


GPIO_Px_CTRL DRIVEMODE = STANDARD

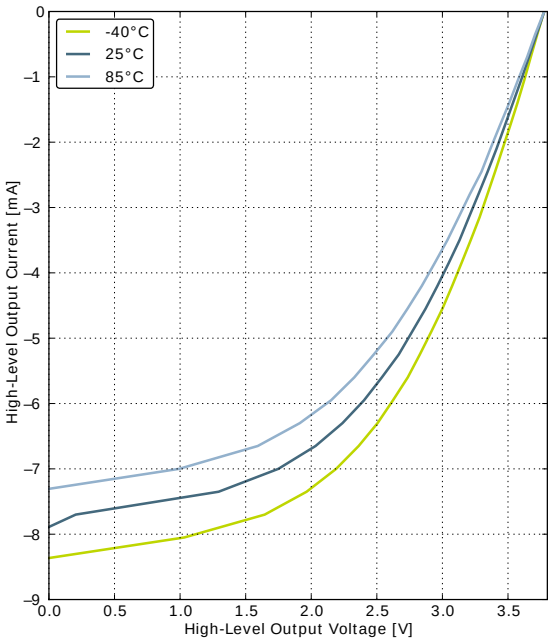


GPIO_Px_CTRL DRIVEMODE = HIGH

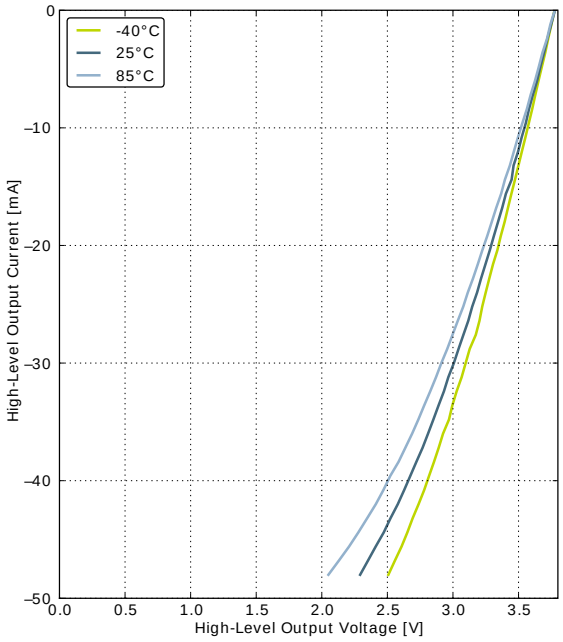
Figure 3.19. Typical High-Level Output Current, 3.8V Supply Voltage



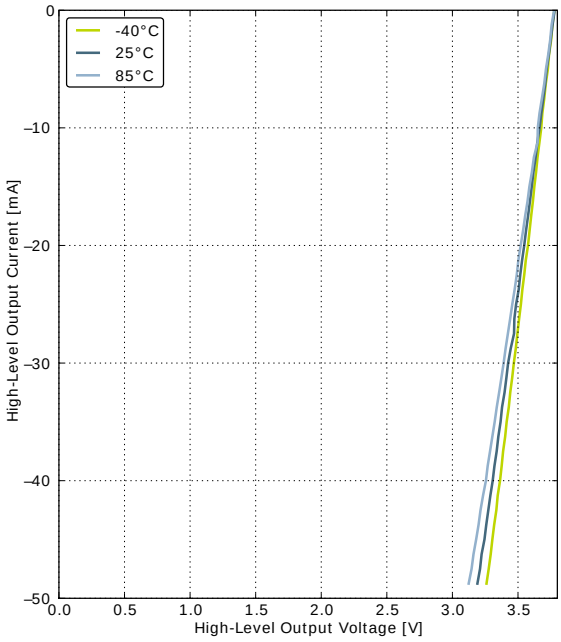
GPIO_Px_CTRL DRIVEMODE = LOWEST



GPIO_Px_CTRL DRIVEMODE = LOW



GPIO_Px_CTRL DRIVEMODE = STANDARD



GPIO_Px_CTRL DRIVEMODE = HIGH

3.9 Oscillators

3.9.1 LFXO

Table 3.9. LFXO

Symbol	Parameter	Condition	Min	Typ	Max	Unit
f_{LFXO}	Supported nominal crystal frequency			32.768		kHz
ESR_{LFXO}	Supported crystal equivalent series resistance (ESR)			30	120	kOhm
C_{LFXOL}	Supported crystal external load range		X[1]		25	pF
DC_{LFXO}	Duty cycle		48	50	53.5	%
I_{LFXO}	Current consumption for core and buffer after start-up.	ESR=30 kOhm, C_L=10 pF, LFXOBOOST in CMU_CTRL is 1		190		nA
t_{LFXO}	Start- up time.	ESR=30 kOhm, C_L=10 pF, 40% - 60% duty cycle has been reached, LFXOBOOST in CMU_CTRL is 1		400		ms

[1]See Minimum Load Capacitance (C_{LFXOL}) Requirement For Safe Crystal Startup figure and table

For safe startup of a given crystal, the load capacitance should be larger than the value indicated in Figure 3.20 (p. 27) and in Table 3.10 (p. 27) for a given LFXOBOOST setting. The minimum supported load capacitance depends on the crystal shunt capacitance, C_0, which is specified in crystal vendors' datasheet.

Figure 3.20. Minimum Load Capacitance (C_{LFXOL}) Requirement For Safe Crystal Startup

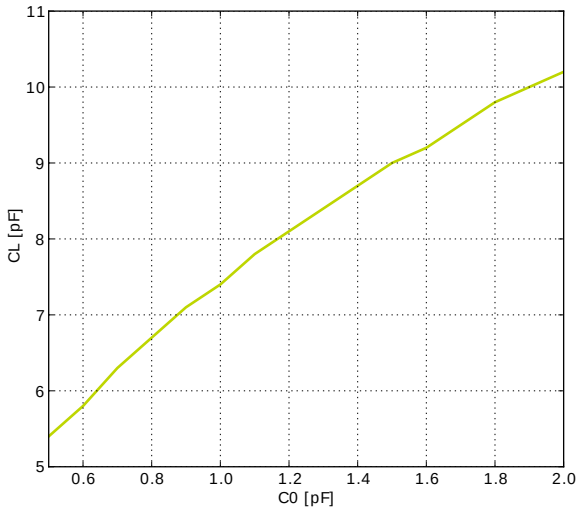


Table 3.10. Minimum Load Capacitance (C_{LFXOL}) Requirement For Safe Crystal Startup

Symbol	Capacitance [pF]															
Shunt Capacitance C_0	0.5	0.6	0.7	0.8	0.9	1.0	1.1	1.2	1.3	1.4	1.5	1.6	1.7	1.8	1.9	2.0
CL_{min} lfxoboost = 0	5.4	5.8	6.3	6.7	7.1	7.4	7.8	8.1	8.4	8.7	9.0	9.2	9.5	9.8	10.0	10.2

3.9.2 HFXO

Table 3.11. HFXO

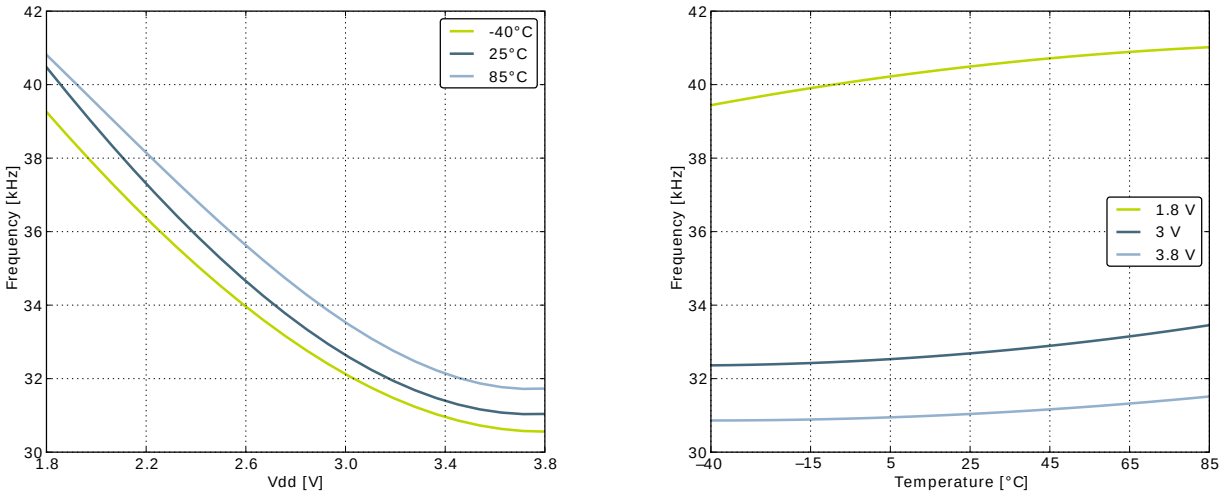
Symbol	Parameter	Condition	Min	Typ	Max	Unit
f_{HFXO}	Supported nominal crystal Frequency		4		32	MHz
ESR_{HFXO}	Supported crystal equivalent series resistance (ESR)	Crystal frequency 32 MHz		30	60	Ohm
		Crystal frequency 4 MHz		400	1500	Ohm
g_{mHFXO}	The transconductance of the HFXO input transistor at crystal startup	HFXOBOOST in CMU_CTRL equals 0b11	20			mS
C_{HFXOL}	Supported crystal external load range		5		25	pF
DC_{HFXO}	Duty cycle		46	50	54	%
I_{HFXO}	Current consumption for HFXO after startup	4 MHz: ESR=400 Ohm, C_L=20 pF, HFXOBOOST in CMU_CTRL equals 0b11		85		µA
		32 MHz: ESR=30 Ohm, C_L=10 pF, HFXOBOOST in CMU_CTRL equals 0b11		165		µA
t_{HFXO}	Startup time	32 MHz: ESR=30 Ohm, C_L=10 pF, HFXOBOOST in CMU_CTRL equals 0b11		400		µs
	Pulse width removed by glitch detector		1		4	ns

3.9.3 LFRCO

Table 3.12. LFRCO

Symbol	Parameter	Condition	Min	Typ	Max	Unit
f_{LFRCO}	Oscillation frequency , V_{DD}= 3.0 V, T_{AMB}=25°C			32		kHz
t_{LFRCO}	Startup time not including software calibration			150		µs
I_{LFRCO}	Current consumption			190		nA
TC_{LFRCO}	Temperature coefficient			±0.02		%/°C
VC_{LFRCO}	Supply voltage coefficient			±15		%/V
$TUNESTEP_{L-FRCO}$	Frequency step for LSB change in TUNING value			1.5		%

Figure 3.21. Calibrated LFRCO Frequency vs Temperature and Supply Voltage



3.9.4 HFRCO

Table 3.13. HFRCO

Symbol	Parameter	Condition	Min	Typ	Max	Unit
f_{HFRCO}	Oscillation frequency, V_{DD}= 3.0 V, T_{AMB}=25°C	28 MHz frequency band		28		MHz
		21 MHz frequency band		21		MHz
		14 MHz frequency band		14		MHz
		11 MHz frequency band		11		MHz
		7 MHz frequency band		7		MHz
		1 MHz frequency band		1		MHz
$t_{HFRCO\_settling}$	Settling time after start-up	f_{HFRCO} = 14 MHz		0.6		Cycles
I_{HFRCO}	Current consumption	f_{HFRCO} = 28 MHz		106		µA
		f_{HFRCO} = 21 MHz		93		µA
		f_{HFRCO} = 14 MHz		77		µA
		f_{HFRCO} = 11 MHz		72		µA
		f_{HFRCO} = 7 MHz		63		µA
		f_{HFRCO} = 1 MHz		22		µA
DC_{HFRCO}	Duty cycle	f_{HFRCO} = 14 MHz	48.5	50	51	%
TC_{HFRCO}	Temperature coefficient, V_{DD}= 3.0 V	f_{HFRCO} = 14 MHz		±0.01[1]		%/°C
		f_{HFRCO} = 28 MHz		±0.005[1]		%/°C
		f_{HFRCO} = 21 MHz		±0.01[1]		%/°C
		f_{HFRCO} = 11 MHz		±0.02[1]		%/°C
		f_{HFRCO} = 7 MHz		±0.02[1]		%/°C
		f_{HFRCO} = 1 MHz		±0.06[1]		%/°C
VC_{HFRCO}	Supply voltage coefficient, T_{AMB}=25°C	f_{HFRCO} = 14 MHz		±0.32[2]		%/V
		f_{HFRCO} = 28 MHz		±0.52[2]		%/V
		f_{HFRCO} = 21 MHz		±0.25[2]		%/V
		f_{HFRCO} = 11 MHz		±0.28[2]		%/V
		f_{HFRCO} = 7 MHz		±0.3[2]		%/V
		f_{HFRCO} = 1 MHz		±15[2]		%/V
$TUNESTEP_{H-FRCO}$	Frequency step for LSB change in TUNING value			0.3		%

[1]Calculated using (max(-40°C - 85°C) - min(-40°C - 85°C)) / f_{HFRCO} / (85°C - (-40°C))
[2]Calculated using (max(1.8V - 3.8V) - min(1.8V - 3.8V)) / f_{HFRCO} / (3.8V - 1.8V))

Figure 3.22. Calibrated HFRCO 1 MHz Band Frequency vs Temperature and Supply Voltage

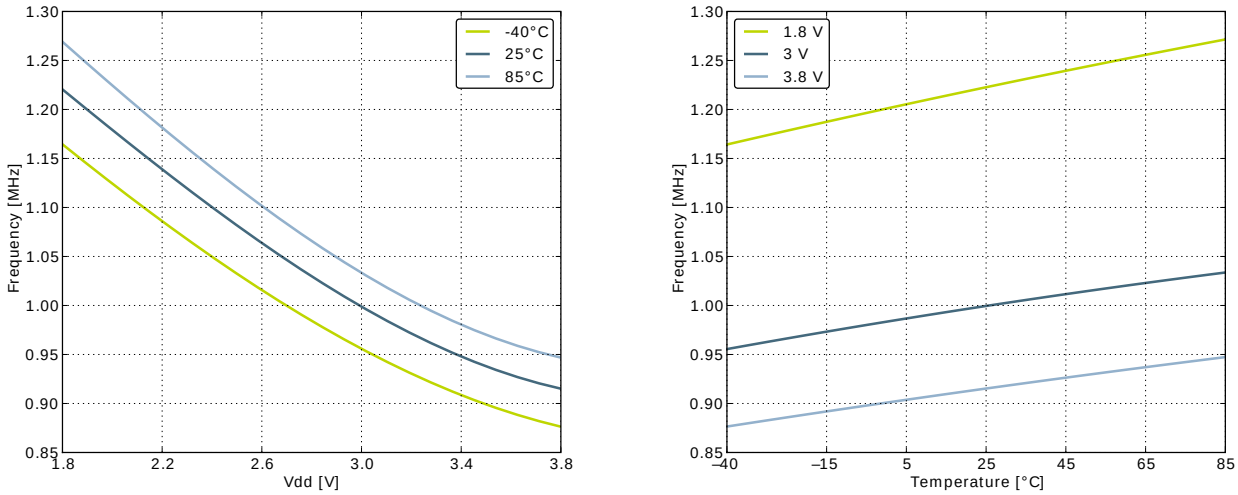


Figure 3.23. Calibrated HFRCO 7 MHz Band Frequency vs Temperature and Supply Voltage

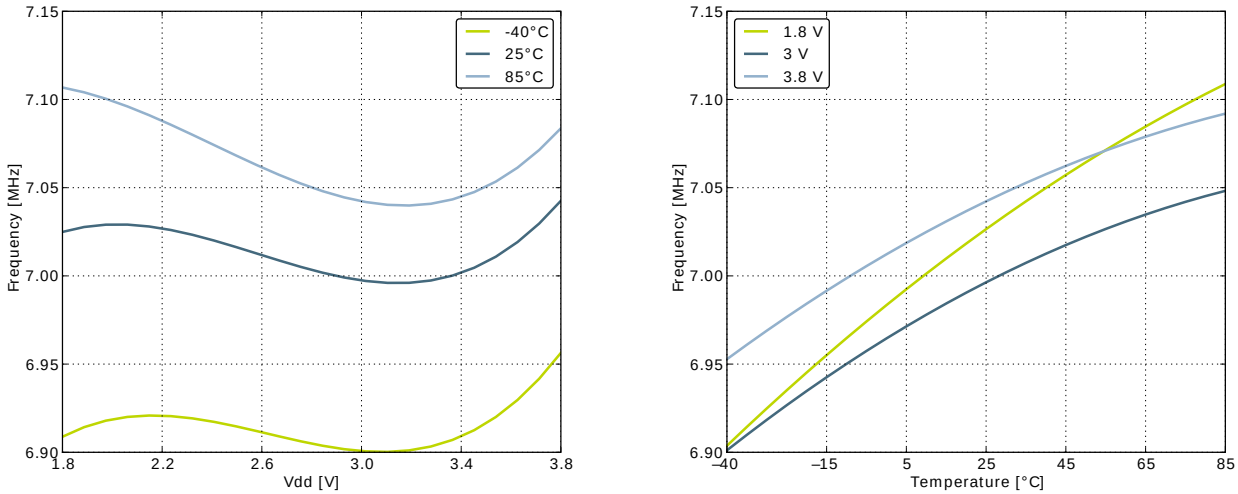


Figure 3.24. Calibrated HFRCO 11 MHz Band Frequency vs Temperature and Supply Voltage

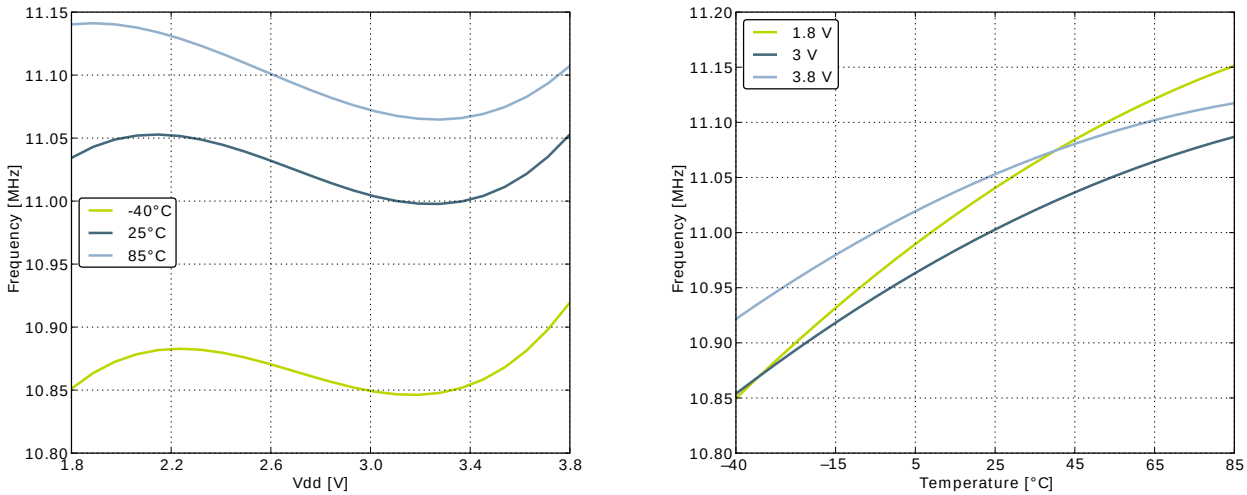


Figure 3.25. Calibrated HFRCO 14 MHz Band Frequency vs Temperature and Supply Voltage

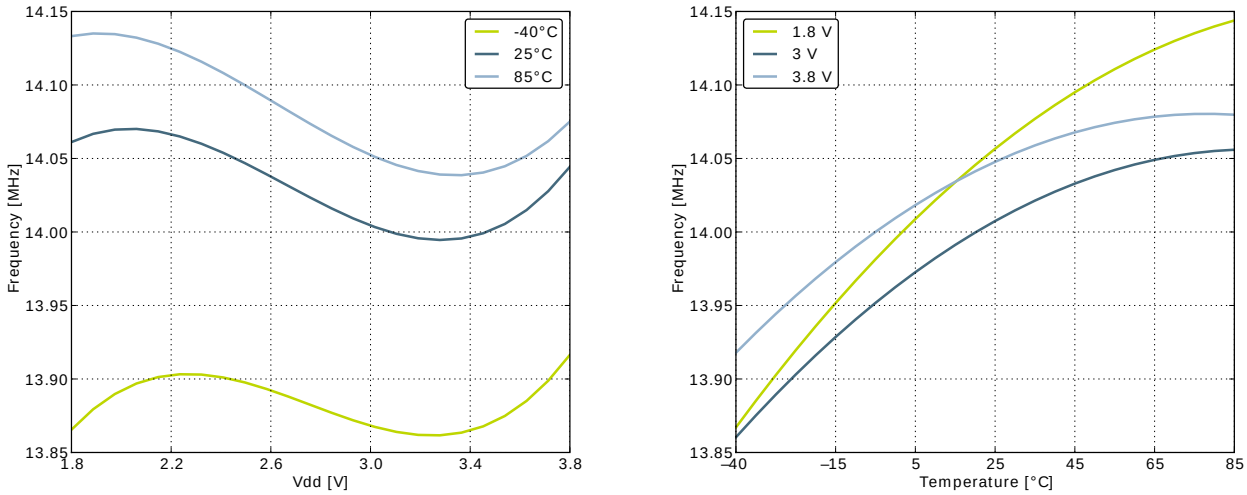


Figure 3.26. Calibrated HFRCO 21 MHz Band Frequency vs Temperature and Supply Voltage

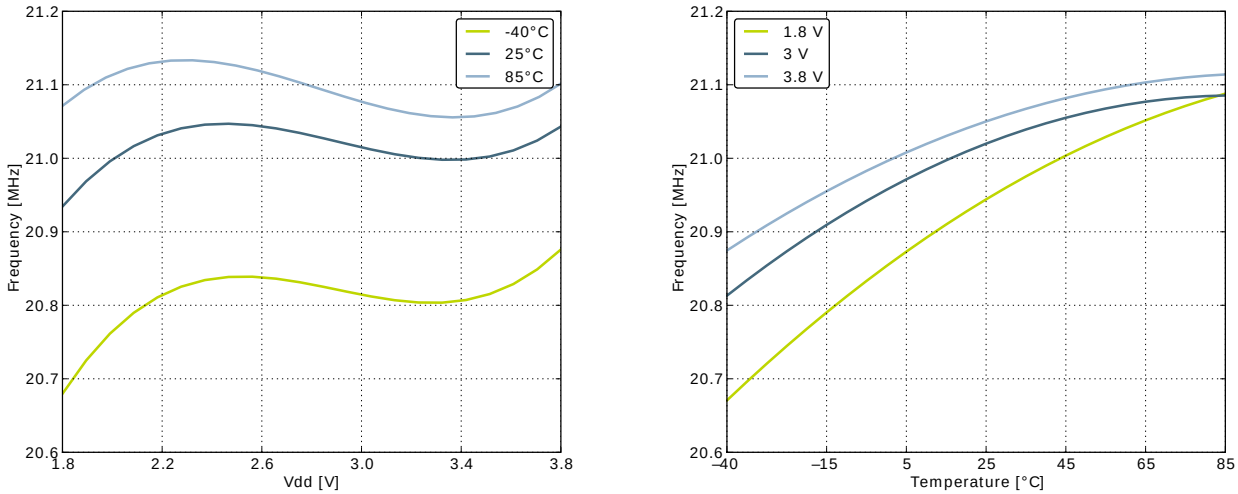
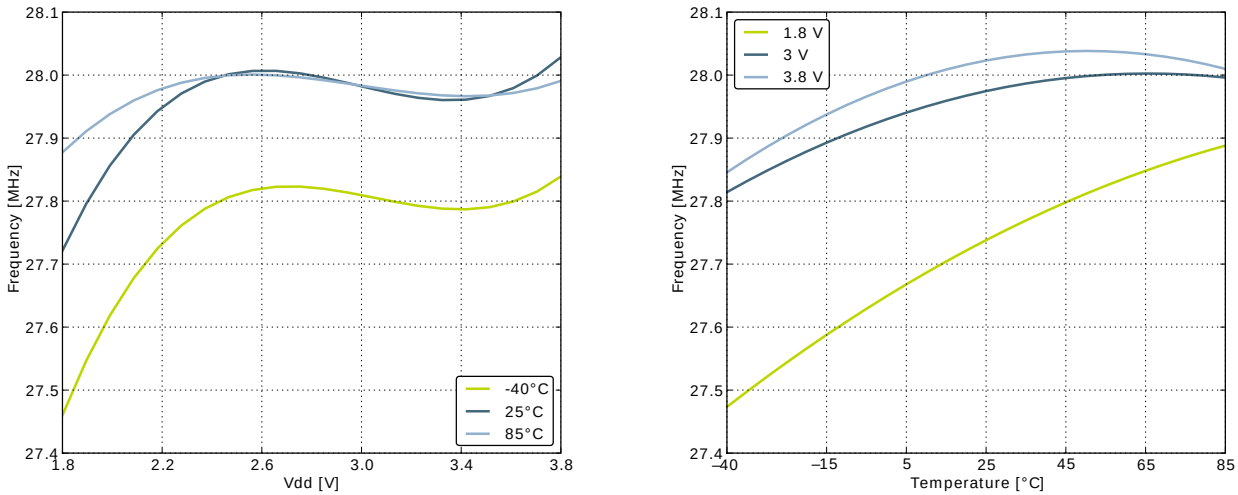


Figure 3.27. Calibrated HFRCO 28 MHz Band Frequency vs Temperature and Supply Voltage



3.9.5 ULFRCO

Table 3.14. ULFRCO

Symbol	Parameter	Condition	Min	Typ	Max	Unit
f_{ULFRCO}	Oscillation frequency	25°C, 3V	0.8		1.5	kHz
TC_{ULFRCO}	Temperature coefficient			0.05		%/°C
VC_{ULFRCO}	Supply voltage coefficient			-18.2		%/V

3.10 Analog Digital Converter (ADC)

Table 3.15. ADC

Symbol	Parameter	Condition	Min	Typ	Max	Unit
V_{ADCIN}	Input voltage range	Single ended	0		V_{REF}	V
		Differential	$-V_{REF}/2$		$V_{REF}/2$	V
$V_{ADCREFIN}$	Input range of external reference voltage, single ended and differential		1.25		V_{DD}	V
$V_{ADCREFIN\_CH7}$	Input range of external negative reference voltage on channel 7	See $V_{ADCREFIN}$	0		V_{DD} - 1.1	V
$V_{ADCREFIN\_CH6}$	Input range of external positive reference voltage on channel 6	See $V_{ADCREFIN}$	0.625		V_{DD}	V
$V_{ADCCMIN}$	Common mode input range		0		V_{DD}	V
I_{ADCIN}	Input current	2pF sampling capacitors		<100		nA
$CMRR_{ADC}$	Analog input common mode rejection ratio			65		dB
I_{ADC}	Average active current	1 MSamples/s, 12 bit, external reference		351		µA
		1 MSamples/s, 12 bit, internal reference		411		µA
		10 kSamples/s 12 bit, internal 1.25 V reference, WARMUPMODE in ADCn_CTRL set to 0b00, ADC_CLK running at 13MHz		67		µA
		10 kSamples/s 12 bit, internal 1.25 V reference, WARMUPMODE in ADCn_CTRL set to 0b01, ADC_CLK running at 13MHz		63		µA
		10 kSamples/s 12 bit, internal 1.25 V reference, WARMUPMODE in ADCn_CTRL set to 0b10, ADC_CLK running at 13MHz		64		µA
C_{ADCIN}	Input capacitance			2		pF
R_{ADCIN}	Input ON resistance		1			MOhm
$R_{ADCFILT}$	Input RC filter resistance			10		kOhm

Symbol	Parameter	Condition	Min	Typ	Max	Unit
$C_{ADCFILT}$	Input RC filter/decoupling capacitance			250		fF
f_{ADCCLK}	ADC Clock Frequency				13	MHz
$t_{ADCCONV}$	Conversion time	6 bit	7			ADC-CLK Cycles
		10 bit	11			ADC-CLK Cycles
		12 bit	13			ADC-CLK Cycles
t_{ADCACQ}	Acquisition time	Programmable	1		256	ADC-CLK Cycles
$t_{ADCACQVDD3}$	Required acquisition time for VDD/3 reference		2			µs
$t_{ADCSTART}$	Startup time of reference generator and ADC core in NORMAL mode			5		µs
	Startup time of reference generator and ADC core in KEEPADCWARM mode			1		µs
SNR_{ADC}	Signal to Noise Ratio (SNR)	1 MSamples/s, 12 bit, single ended, internal 1.25V reference		59		dB
		1 MSamples/s, 12 bit, single ended, internal 2.5V reference		63		dB
		1 MSamples/s, 12 bit, single ended, V_{DD} reference		65		dB
		1 MSamples/s, 12 bit, differential, internal 1.25V reference		60		dB
		1 MSamples/s, 12 bit, differential, internal 2.5V reference		65		dB
		1 MSamples/s, 12 bit, differential, 5V reference		54		dB
		1 MSamples/s, 12 bit, differential, V_{DD} reference		67		dB
		1 MSamples/s, 12 bit, differential, $2xV_{DD}$ reference		69		dB
		200 kSamples/s, 12 bit, single ended, internal 1.25V reference		62		dB
		200 kSamples/s, 12 bit, single ended, internal 2.5V reference		63		dB
		200 kSamples/s, 12 bit, single ended, V_{DD} reference		67		dB

Symbol	Parameter	Condition	Min	Typ	Max	Unit
		200 kSamples/s, 12 bit, differential, internal 1.25V reference		63		dB
		200 kSamples/s, 12 bit, differential, internal 2.5V reference		66		dB
		200 kSamples/s, 12 bit, differential, 5V reference		66		dB
		200 kSamples/s, 12 bit, differential, V_{DD} reference		69		dB
		200 kSamples/s, 12 bit, differential, 2xV_{DD} reference		70		dB
$SNDR_{ADC}$	Signal to Noise-puls-Distortion Ratio (SNDR)	1 MSamples/s, 12 bit, single ended, internal 1.25V reference		58		dB
		1 MSamples/s, 12 bit, single ended, internal 2.5V reference		62		dB
		1 MSamples/s, 12 bit, single ended, V_{DD} reference		64		dB
		1 MSamples/s, 12 bit, differential, internal 1.25V reference		60		dB
		1 MSamples/s, 12 bit, differential, internal 2.5V reference		64		dB
		1 MSamples/s, 12 bit, differential, 5V reference		54		dB
		1 MSamples/s, 12 bit, differential, V_{DD} reference		66		dB
		1 MSamples/s, 12 bit, differential, 2xV_{DD} reference		68		dB
		200 kSamples/s, 12 bit, single ended, internal 1.25V reference		61		dB
		200 kSamples/s, 12 bit, single ended, internal 2.5V reference		65		dB
		200 kSamples/s, 12 bit, single ended, V_{DD} reference		66		dB
		200 kSamples/s, 12 bit, differential, internal 1.25V reference		63		dB
		200 kSamples/s, 12 bit, differential, internal 2.5V reference		66		dB
		200 kSamples/s, 12 bit, differential, 5V reference		66		dB
		200 kSamples/s, 12 bit, differential, V_{DD} reference		68		dB
		200 kSamples/s, 12 bit, differential, 2xV_{DD} reference		69		dB

Symbol	Parameter	Condition	Min	Typ	Max	Unit
$SFDR_{ADC}$	Spurious-Free Dynamic Range (SFDR)	1 MSamples/s, 12 bit, single ended, internal 1.25V reference		64		dBc
		1 MSamples/s, 12 bit, single ended, internal 2.5V reference		76		dBc
		1 MSamples/s, 12 bit, single ended, V_{DD} reference		73		dBc
		1 MSamples/s, 12 bit, differential, internal 1.25V reference		66		dBc
		1 MSamples/s, 12 bit, differential, internal 2.5V reference		77		dBc
		1 MSamples/s, 12 bit, differential, V_{DD} reference		76		dBc
		1 MSamples/s, 12 bit, differential, $2xV_{DD}$ reference		75		dBc
		1 MSamples/s, 12 bit, differential, 5V reference		69		dBc
		200 kSamples/s, 12 bit, single ended, internal 1.25V reference		75		dBc
		200 kSamples/s, 12 bit, single ended, internal 2.5V reference		75		dBc
		200 kSamples/s, 12 bit, single ended, V_{DD} reference		76		dBc
		200 kSamples/s, 12 bit, differential, internal 1.25V reference		79		dBc
		200 kSamples/s, 12 bit, differential, internal 2.5V reference		79		dBc
		200 kSamples/s, 12 bit, differential, 5V reference		78		dBc
		200 kSamples/s, 12 bit, differential, V_{DD} reference		79		dBc
		200 kSamples/s, 12 bit, differential, $2xV_{DD}$ reference		79		dBc
$V_{ADCOFFSET}$	Offset voltage	After calibration, single ended		0.3		mV
		After calibration, differential		0.3		mV
$TGRAD_{ADCTH}$	Thermometer output gradient			-1.92		mV/°C
				-6.3		ADC Codes/ °C
DNL_{ADC}	Differential non-linearity (DNL)			±0.7		LSB
INL_{ADC}	Integral non-linearity (INL), End point method			±1.2		LSB

Symbol	Parameter	Condition	Min	Typ	Max	Unit
MC_{ADC}	No missing codes		11.999[1]	12		bits

[1]On the average every ADC will have one missing code, most likely to appear around 2048 +/- n*512 where n can be a value in the set {-3, -2, -1, 1, 2, 3}. There will be no missing code around 2048, and in spite of the missing code the ADC will be monotonic at all times so that a response to a slowly increasing input will always be a slowly increasing output. Around the one code that is missing, the neighbour codes will look wider in the DNL plot. The spectra will show spurs on the level of -78dBc for a full scale input for chips that have the missing code issue.

The integral non-linearity (INL) and differential non-linearity parameters are explained in Figure 3.28 (p. 37) and Figure 3.29 (p. 37) , respectively.

Figure 3.28. Integral Non-Linearity (INL)

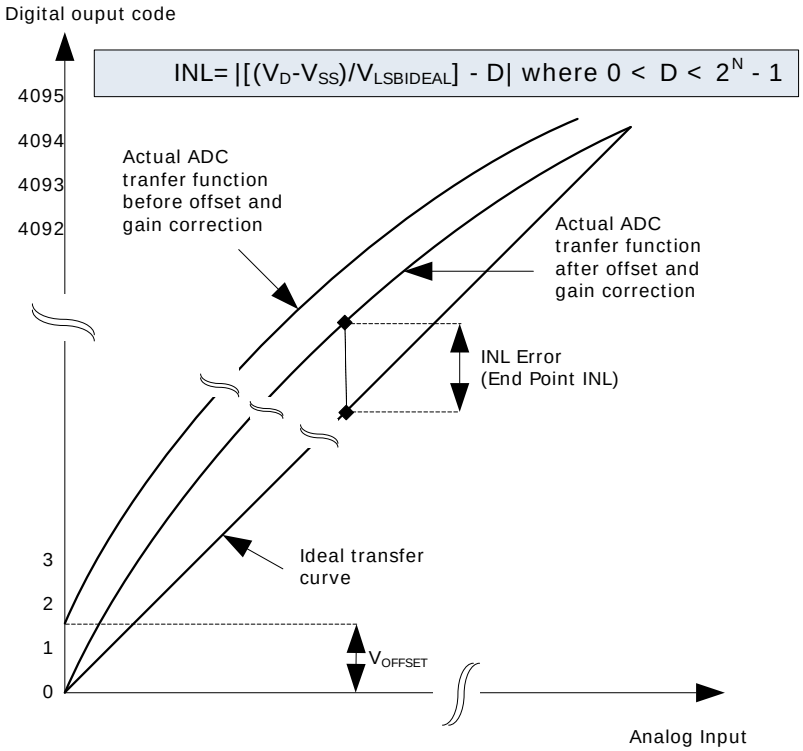
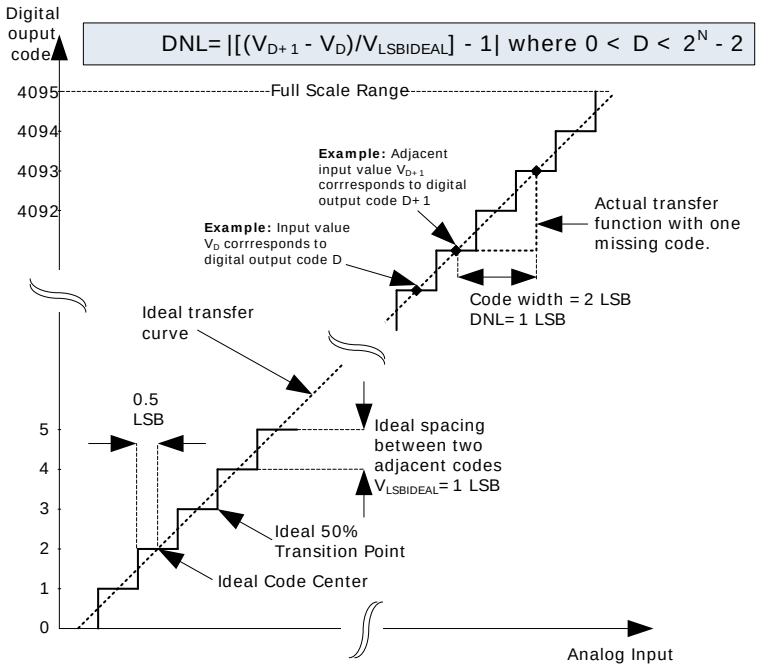
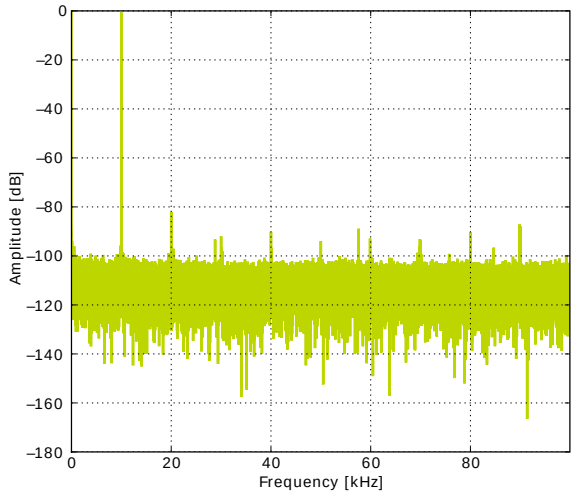


Figure 3.29. Differential Non-Linearity (DNL)

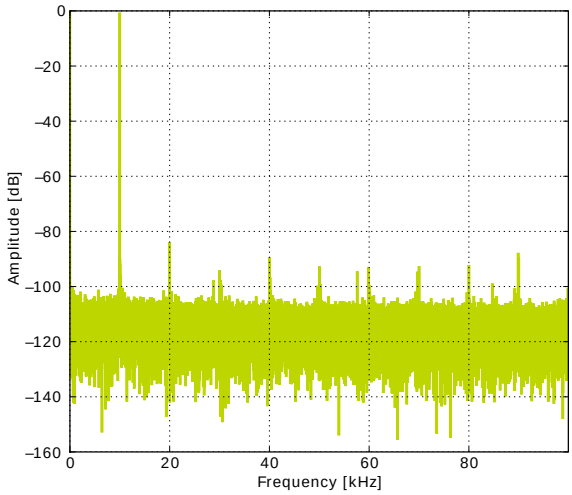


3.10.1 Typical performance

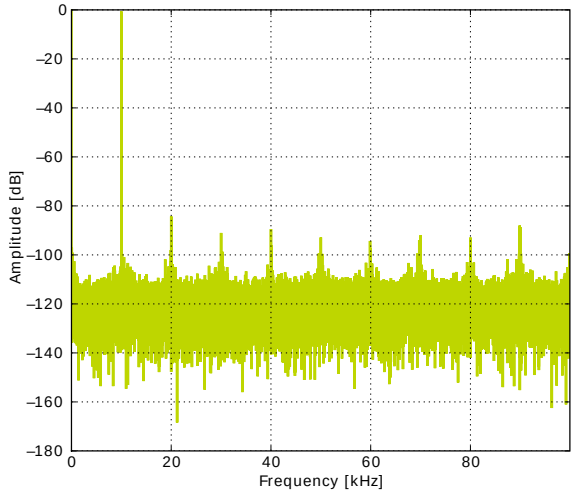
Figure 3.30. ADC Frequency Spectrum, Vdd = 3V, Temp = 25°



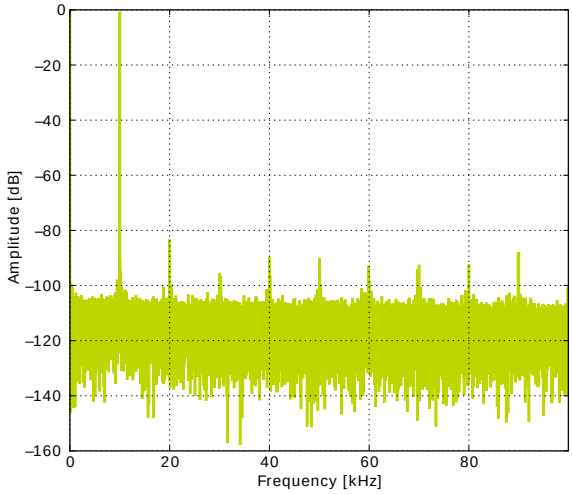
1.25V Reference



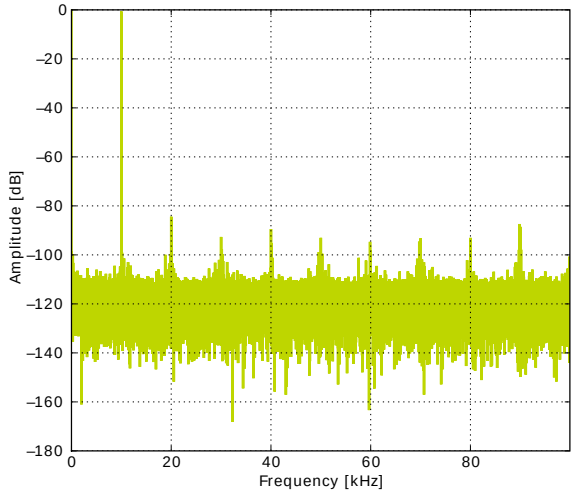
2.5V Reference



2XVDDVSS Reference

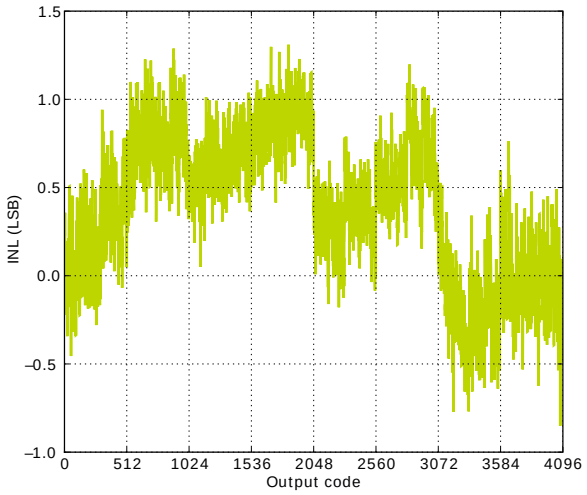


5VDIFF Reference

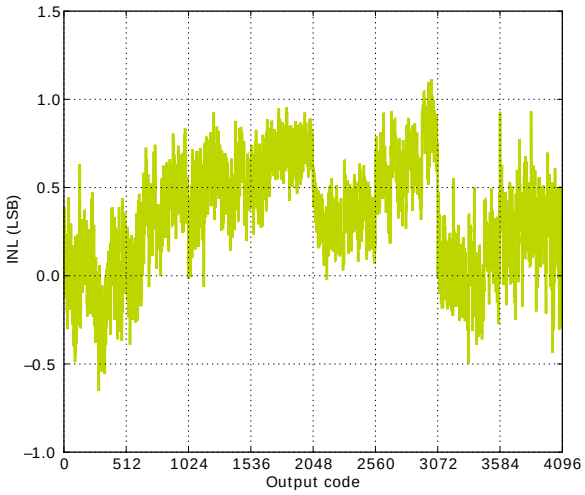


VDD Reference

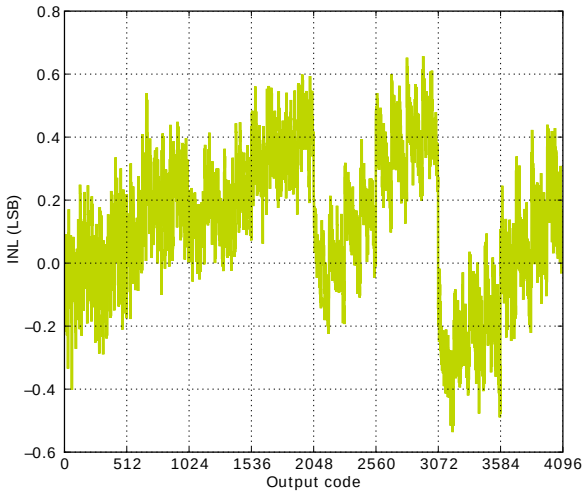
Figure 3.31. ADC Integral Linearity Error vs Code, Vdd = 3V, Temp = 25°



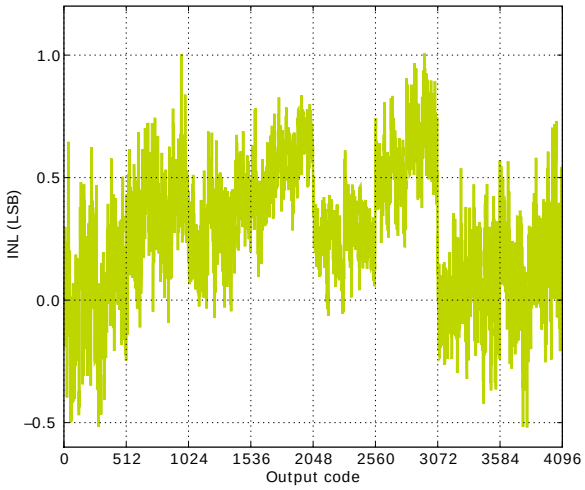
1.25V Reference



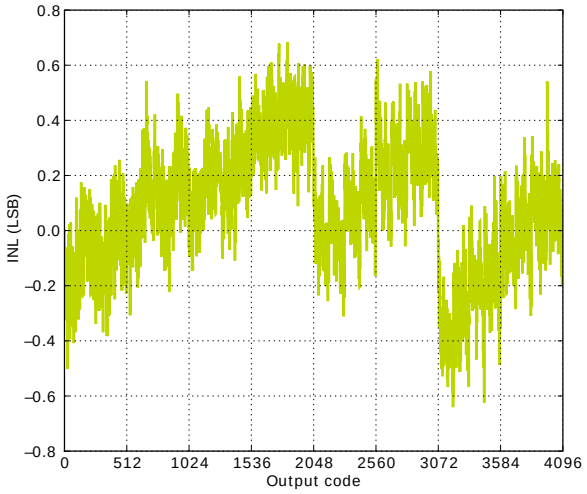
2.5V Reference



2XVDDVSS Reference

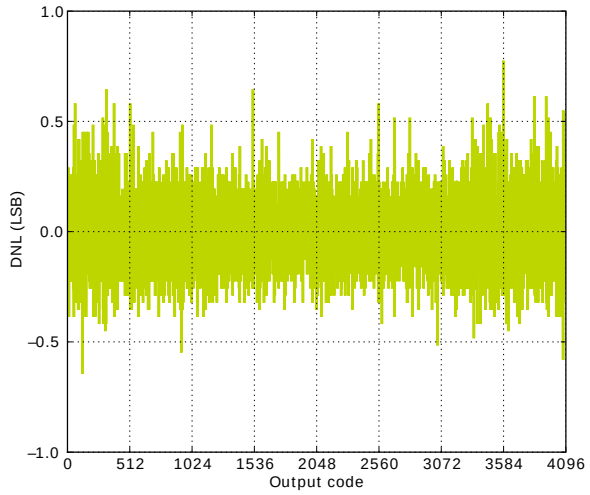


5VDIFF Reference

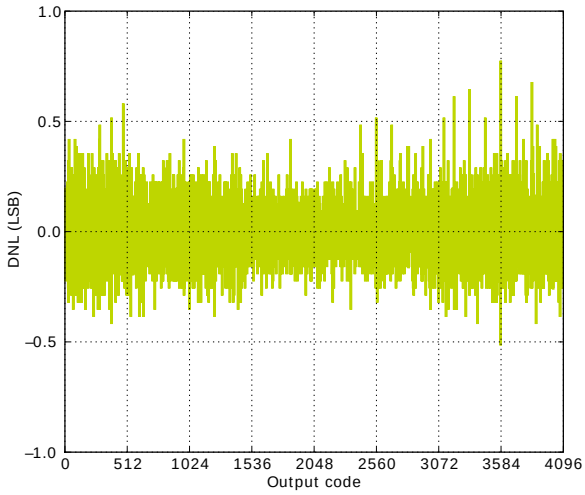


VDD Reference

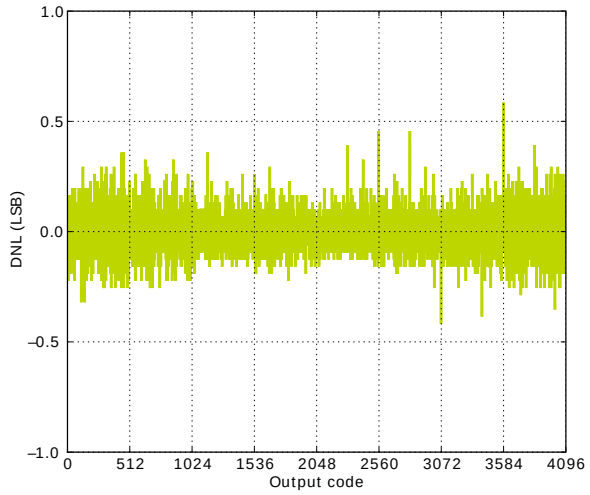
Figure 3.32. ADC Differential Linearity Error vs Code, Vdd = 3V, Temp = 25°



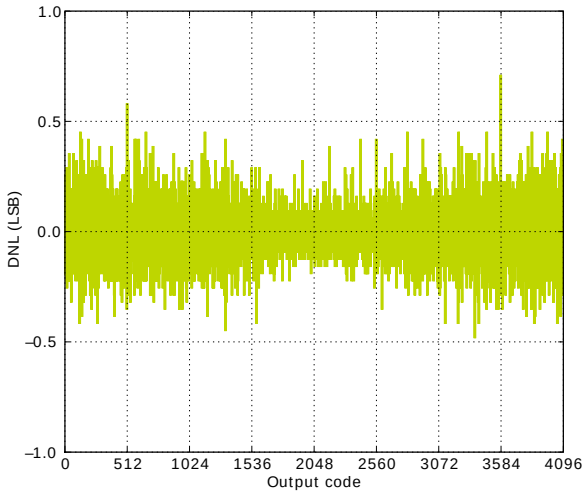
1.25V Reference



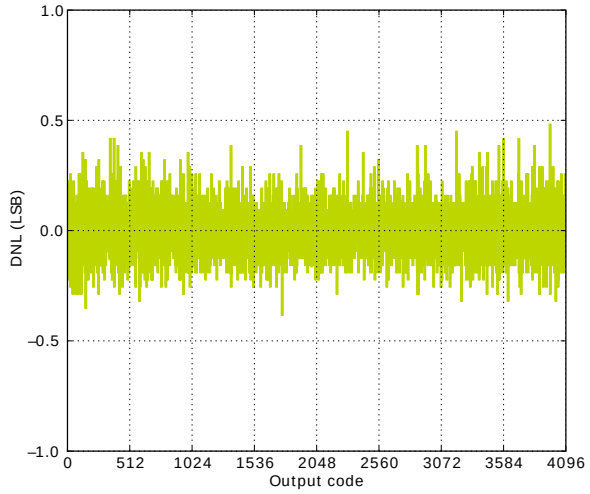
2.5V Reference



2XVDDVSS Reference

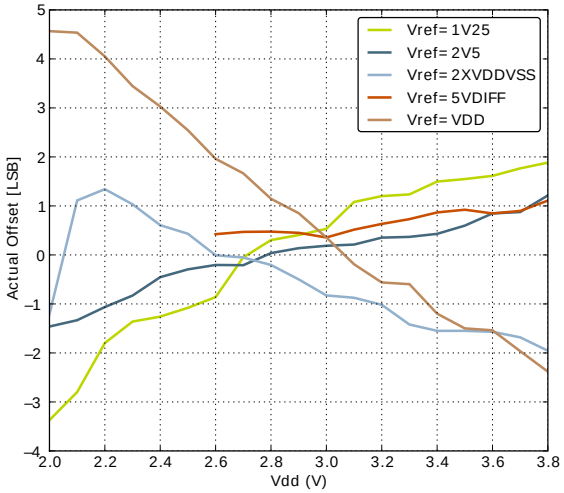


5VDIFF Reference

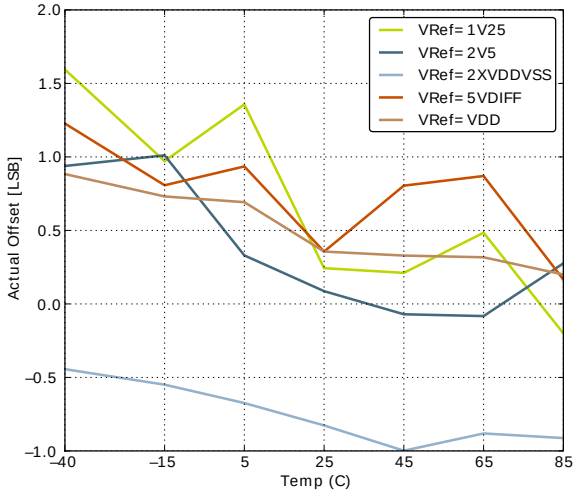


VDD Reference

Figure 3.33. ADC Absolute Offset, Common Mode = Vdd /2

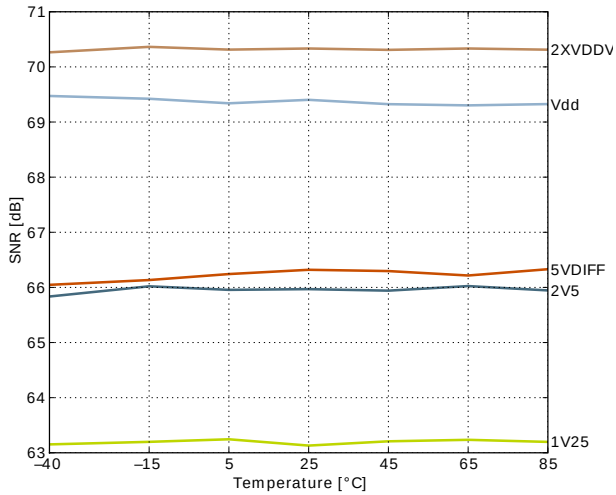


Offset vs Supply Voltage, Temp = 25°

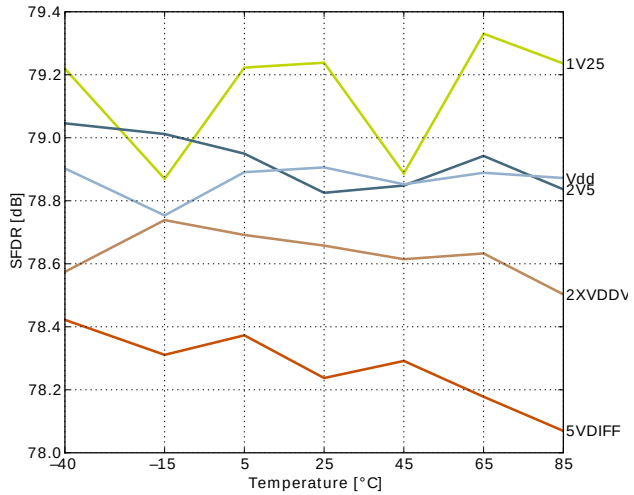


Offset vs Temperature, Vdd = 3V

Figure 3.34. ADC Dynamic Performance vs Temperature for all ADC References, Vdd = 3V



Signal to Noise Ratio (SNR)



Spurious-Free Dynamic Range (SFDR)

3.11 Digital Analog Converter (DAC)

Table 3.16. DAC

Symbol	Parameter	Condition	Min	Typ	Max	Unit
V_{DACOUT}	Output voltage range	VDD voltage reference, single ended	0		V_{DD}	V
		VDD voltage reference, differential	$-V_{DD}$		V_{DD}	V
V_{DACCM}	Output common mode voltage range		0		V_{DD}	V
I_{DAC}	Active current including references for 2 channels	500 kSamples/s, 12bit		400		µA
		100 kSamples/s, 12 bit		200		µA
		1 kSamples/s 12 bit		38		µA

Symbol	Parameter	Condition	Min	Typ	Max	Unit
SR_{DAC}	Sample rate				500	ksamples/s
f_{DAC}	DAC clock frequency	Continuous Mode			1000	kHz
		Sample/Hold Mode			250	kHz
		Sample/Off Mode			250	kHz
$CYC_{DACCONV}$	Clock cyckles per conversion			2		
$t_{DACCONV}$	Conversion time		2			µs
$t_{DACSETTLE}$	Settling time			5		µs
SNR_{DAC}	Signal to Noise Ratio (SNR)	500 kSamples/s, 12 bit, single ended, internal 1.25V reference		58		dB
		500 kSamples/s, 12 bit, single ended, internal 2.5V reference		59		dB
		500 kSamples/s, 12 bit, differential, internal 1.25V reference		58		dB
		500 kSamples/s, 12 bit, differential, internal 2.5V reference		58		dB
		500 kSamples/s, 12 bit, differential, V_{DD} reference		59		dB
$SNDR_{DAC}$	Signal to Noise-pulse Distortion Ratio (SNDR)	500 kSamples/s, 12 bit, single ended, internal 1.25V reference		57		dB
		500 kSamples/s, 12 bit, single ended, internal 2.5V reference		54		dB
		500 kSamples/s, 12 bit, differential, internal 1.25V reference		56		dB
		500 kSamples/s, 12 bit, differential, internal 2.5V reference		53		dB
		500 kSamples/s, 12 bit, differential, V_{DD} reference		55		dB
$SFDR_{DAC}$	Spurious-Free Dynamic Range(SFDR)	500 kSamples/s, 12 bit, single ended, internal 1.25V reference		62		dBc
		500 kSamples/s, 12 bit, single ended, internal 2.5V reference		56		dBc
		500 kSamples/s, 12 bit, differential, internal 1.25V reference		61		dBc
		500 kSamples/s, 12 bit, differential, internal 2.5V reference		55		dBc
		500 kSamples/s, 12 bit, differential, V_{DD} reference		60		dBc
$V_{DACOFFSET}$	Offset voltage	After calibration, single ended		2		mV

Symbol	Parameter	Condition	Min	Typ	Max	Unit
		After calibration, differential		2		mV
$V_{DACSHMDRIFT}$	Sample-hold mode voltage drift			540		µV/ms
DNL_{DAC}	Differential non-linearity			±1		LSB
INL_{DAC}	Integral non-linearity			±5		LSB
MC_{DAC}	No missing codes			12		bits

3.12 Analog Comparator (ACMP)

Table 3.17. ACMP

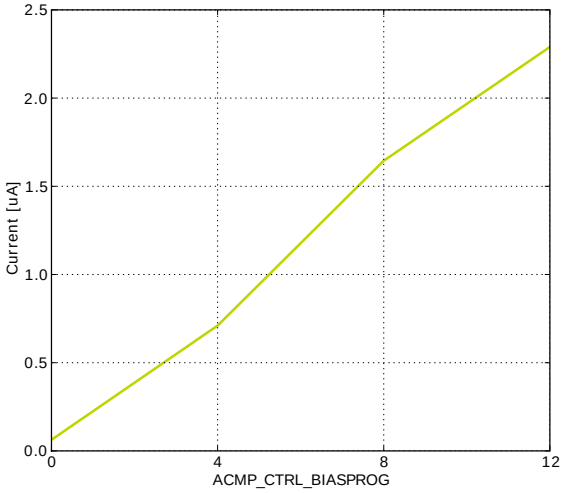
Symbol	Parameter	Condition	Min	Typ	Max	Unit
V_{ACMPIN}	Input voltage range		0		V_{DD}	V
V_{ACMPCM}	ACMP Common Mode voltage range		0		V_{DD}	V
I_{ACMP}	Active current	BIASPROG=0b0000, FULLBIAS=0 and HALFBIAS=1 in ACMPn_CTRL register		55		nA
		BIASPROG=0b1111, FULLBIAS=0 and HALFBIAS=0 in ACMPn_CTRL register		2.82		µA
		BIASPROG=0b1111, FULLBIAS=1 and HALFBIAS=0 in ACMPn_CTRL register		195		µA
$I_{ACMPREF}$	Current consumption of internal voltage reference	Internal voltage reference off. Using external voltage reference		0		µA
		Internal voltage reference, LPREF=1		50		nA
		Internal voltage reference, LPREF=0		6		µA
$V_{ACMPOFFSET}$	Offset voltage	Single ended		10		mV
		Differential		10		mV
$V_{ACMPHYST}$	ACMP hysteresis	Programmable		17		mV
R_{CSRES}	Capacitive Sense Internal Resistance	CSRESSEL=0b00 in ACMPn_INPUTSEL		39		kOhm
		CSRESSEL=0b01 in ACMPn_INPUTSEL		71		kOhm
		CSRESSEL=0b10 in ACMPn_INPUTSEL		104		kOhm
		CSRESSEL=0b11 in ACMPn_INPUTSEL		136		kOhm

The total ACMP current is the sum of the contributions from the ACMP and its internal voltage reference as given in Equation 3.1 (p. 43) . $I_{ACMPREF}$ is zero if an external voltage reference is used.

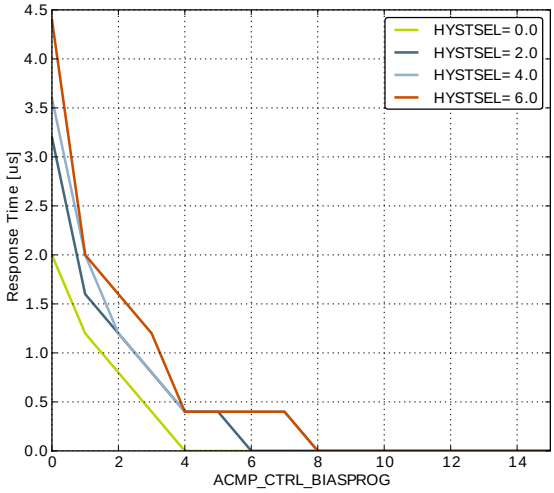
Total ACMP Active Current

$$I_{ACMPTOTAL} = I_{ACMP} + I_{ACMPREF} \quad (3.1)$$

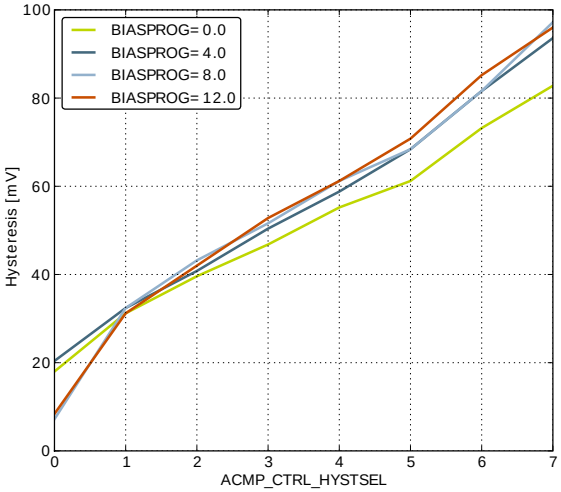
Figure 3.35. Typical ACMP Characteristics



Current consumption



Response time



Hysteresis

3.13 Voltage Comparator (VCMP)

Table 3.18. VCMP

Symbol	Parameter	Condition	Min	Typ	Max	Unit
V_{VCMPIN}	Input voltage range			V_{DD}		V
V_{VCMPCM}	VCMP Common Mode voltage range			V_{DD}		V
I_{VCMP}	Active current	BIASPROG=0b0000 and HALFBIAS=1 in VCMPn_CTRL register		0.1		µA
		BIASPROG=0b1111 and HALFBIAS=0 in VCMPn_CTRL register. LPREF=0.		14.7		µA
$t_{VCMPREF}$	Startup time reference generator	NORMAL		10		µs
$V_{VCMPOFFSET}$	Offset voltage	Single ended		10		mV
		Differential		10		mV
$V_{VCMPHYST}$	VCMP hysteresis			17		mV

The V_{DD} trigger level can be configured by setting the TRIGLEVEL field of the VCMP_CTRL register in accordance with the following equation:

VCMP Trigger Level as a Function of Level Setting

$$V_{DD\ Trigger\ Level}=1.667V+0.034 \times TRIGLEVEL \quad (3.2)$$

3.14 Digital Peripherals

Table 3.19. Digital Peripherals

Symbol	Parameter	Condition	Min	Typ	Max	Unit
I_{USART}	USART current	USART idle current, clock enabled		7.5		µA/MHz
I_{UART}	UART current	UART idle current, clock enabled		5.63		µA/MHz
I_{LEUART}	LEUART current	LEUART idle current, clock enabled		150		nA
I_{I2C}	I2C current	I2C idle current, clock enabled		6.25		µA/MHz
I_{TIMER}	TIMER current	TIMER_0 idle current, clock enabled		8.75		µA/MHz
$I_{LETIMER}$	LETIMER current	LETIMER idle current, clock enabled		150		nA
I_{PCNT}	PCNT current	PCNT idle current, clock enabled		100		nA
I_{RTC}	RTC current	RTC idle current, clock enabled		100		nA
I_{AES}	AES current	AES idle current, clock enabled		2.5		µA/MHz

Symbol	Parameter	Condition	Min	Typ	Max	Unit
I_{GPIO}	GPIO current	GPIO idle current, clock enabled		5.31		µA/MHz
I_{EBI}	EBI current	EBI idle current, clock enabled		1.56		µA/MHz
I_{PRS}	PRS current	PRS idle current		2,81		µA/MHz
I_{DMA}	DMA current	Clock enable		8.12		µA/MHz

4 Pinout and Package

Note

Please refer to the application note "AN0002 EFM32 Hardware Design Considerations" for guidelines on designing Printed Circuit Boards (PCB's) for the EFM32G290.

4.1 Pinout

The *EFM32G290* pinout is shown in Figure 4.1 (p. 47) and Table 4.1 (p. 47). Alternate locations are denoted by "#" followed by the location number (Multiple locations on the same pin are split with "/"). Alternate locations can be configured in the LOCATION bitfield in the *_ROUTE register in the module in question.

Figure 4.1. EFM32G290 Pinout (top view, not to scale)

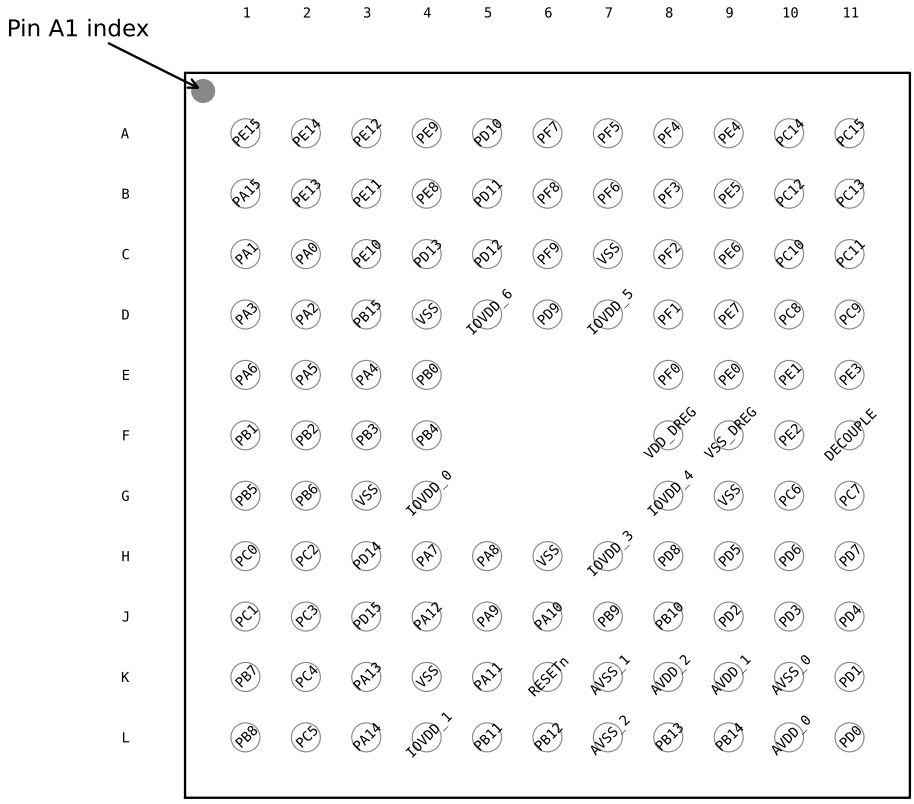


Table 4.1. Device Pinout

BGA112 Pin# and Name		Pin Alternate Functionality / Description				
Pin #	Pin Name	Analog	EBI	Timers	Communication	Other
A1	PE15		EBI_AD07 #0		LEU0_RX #2	
A2	PE14		EBI_AD06 #0		LEU0_TX #2	
A3	PE12		EBI_AD04 #0	TIM1_CC2 #1	US0_CLK #0	

BGA112 Pin# and Name		Pin Alternate Functionality / Description				
Pin #	Pin Name	Analog	EBI	Timers	Communication	Other
A4	PE9		EBI_AD01 #0	PCNT2_S1IN #1		
A5	PD10		EBI_CS1 #0			
A6	PF7			TIM0_CC1 #2	U0_RX #0	
A7	PF5		EBI_REn #0	TIM0_CDTI2 #2		
A8	PF4		EBI_WEn #0	TIM0_CDTI1 #2		
A9	PE4				US0_CS #1	
A10	PC14	ACMP1_CH6		TIM0_CDTI1 #1/3 TIM1_CC1 #0 PCNT0_S1IN #0	U0_TX #3	
A11	PC15	ACMP1_CH7		TIM0_CDTI2 #1/3 TIM1_CC2 #0	U0_RX #3	DBG_SWO #1
B1	PA15		EBI_AD08 #0			
B2	PE13		EBI_AD05 #0		US0_CS #0	ACMP0_O #0
B3	PE11		EBI_AD03 #0	TIM1_CC1 #1	US0_RX #0	
B4	PE8		EBI_AD00 #0	PCNT2_S0IN #1		
B5	PD11		EBI_CS2 #0			
B6	PF8			TIM0_CC2 #2		
B7	PF6			TIM0_CC0 #2	U0_TX #0	
B8	PF3		EBI_ALE #0	TIM0_CDTI0 #2		
B9	PE5				US0_CLK #1	
B10	PC12	ACMP1_CH4				CMU_CLK0 #1
B11	PC13	ACMP1_CH5		TIM0_CDTI0 #1/3 TIM1_CC0 #0 PCNT0_S0IN #0		
C1	PA1		EBI_AD10 #0	TIM0_CC1 #0/1	I2C0_SCL #0	CMU_CLK1 #0
C2	PA0		EBI_AD09 #0	TIM0_CC0 #0/1	I2C0_SDA #0	
C3	PE10		EBI_AD02 #0	TIM1_CC0 #1	US0_TX #0	
C4	PD13					
C5	PD12		EBI_CS3 #0			
C6	PF9					
C7	VSS	Ground				
C8	PF2		EBI_ARDY #0			ACMP1_O #0 DBG_SWO #0
C9	PE6				US0_RX #1	
C10	PC10	ACMP1_CH2		TIM2_CC2 #2	US0_RX #2	
C11	PC11	ACMP1_CH3			US0_TX #2	
D1	PA3		EBI_AD12 #0	TIM0_CDTI0 #0	U0_TX #2	
D2	PA2		EBI_AD11 #0	TIM0_CC2 #0/1		CMU_CLK0 #0
D3	PB15					
D4	VSS	Ground				
D5	IOVDD_6	Digital IO power supply 6.				
D6	PD9		EBI_CS0 #0			

BGA112 Pin# and Name		Pin Alternate Functionality / Description				
Pin #	Pin Name	Analog	EBI	Timers	Communication	Other
D7	IOVDD_5	Digital IO power supply 5.				
D8	PF1			LETIM0_OUT1 #2		DBG_SWDIO #0/1
D9	PE7				US0_TX #1	
D10	PC8	ACMP1_CH0		TIM2_CC0 #2	US0_CS #2	
D11	PC9	ACMP1_CH1		TIM2_CC1 #2	US0_CLK #2	
E1	PA6		EBI_AD15 #0		LEU1_RX #1	
E2	PA5		EBI_AD14 #0	TIM0_CDTI2 #0	LEU1_TX #1	
E3	PA4		EBI_AD13 #0	TIM0_CDTI1 #0	U0_RX #2	
E4	PB0			TIM1_CC0 #2		
E8	PF0			LETIM0_OUT0 #2		DBG_SWCLK #0/1
E9	PE0			PCNT0_S0IN #1	U0_TX #1	
E10	PE1			PCNT0_S1IN #1	U0_RX #1	
E11	PE3					ACMP1_O #1
F1	PB1			TIM1_CC1 #2		
F2	PB2			TIM1_CC2 #2		
F3	PB3			PCNT1_S0IN #1	US2_TX #1	
F4	PB4			PCNT1_S1IN #1	US2_RX #1	
F8	VDD_DREG	Power supply for on-chip voltage regulator.				
F9	VSS_DREG	Ground for on-chip voltage regulator.				
F10	PE2					ACMP0_O #1
F11	DECOUPLE	Decouple output for on-chip voltage regulator. An external capacitance of size $C_{DECOUPLE}$ is required at this pin.				
G1	PB5				US2_CLK #1	
G2	PB6				US2_CS #1	
G3	VSS	Ground				
G4	IOVDD_0	Digital IO power supply 0.				
G8	IOVDD_4	Digital IO power supply 4.				
G9	VSS	Ground				
G10	PC6	ACMP0_CH6			LEU1_TX #0 I2C0_SDA #2	
G11	PC7	ACMP0_CH7			LEU1_RX #0 I2C0_SCL #2	
H1	PC0	ACMP0_CH0		PCNT0_S0IN #2	US1_TX #0	
H2	PC2	ACMP0_CH2			US2_TX #0	
H3	PD14				I2C0_SDA #3	
H4	PA7					
H5	PA8			TIM2_CC0 #0		
H6	VSS	Ground				
H7	IOVDD_3	Digital IO power supply 3.				
H8	PD8					CMU_CLK1 #1
H9	PD5	ADC0_CH5			LEU0_RX #0	

BGA112 Pin# and Name		Pin Alternate Functionality / Description				
Pin #	Pin Name	Analog	EBI	Timers	Communication	Other
H10	PD6	ADC0_CH6		LETIM0_OUT0 #0	I2C0_SDA #1	
H11	PD7	ADC0_CH7		LETIM0_OUT1 #0	I2C0_SCL #1	
J1	PC1	ACMP0_CH1		PCNT0_S1IN #2	US1_RX #0	
J2	PC3	ACMP0_CH3			US2_RX #0	
J3	PD15				I2C0_SCL #3	
J4	PA12			TIM2_CC0 #1		
J5	PA9			TIM2_CC1 #0		
J6	PA10			TIM2_CC2 #0		
J7	PB9					
J8	PB10					
J9	PD2	ADC0_CH2		TIM0_CC1 #3	US1_CLK #1	
J10	PD3	ADC0_CH3		TIM0_CC2 #3	US1_CS #1	
J11	PD4	ADC0_CH4			LEU0_TX #0	
K1	PB7	LFXTAL_P			US1_CLK #0	
K2	PC4	ACMP0_CH4		LETIM0_OUT0 #3 PCNT1_S0IN #0	US2_CLK #0	
K3	PA13			TIM2_CC1 #1		
K4	VSS	Ground				
K5	PA11					
K6	RESETn	Reset input. Active low, with internal pull-up.				
K7	AVSS_1	Analog ground 1.				
K8	AVDD_2	Analog power supply 2.				
K9	AVDD_1	Analog power supply 1.				
K10	AVSS_0	Analog ground 0.				
K11	PD1	ADC0_CH1		TIM0_CC0 #3 PCNT2_S1IN #0	US1_RX #1	
L1	PB8	LFXTAL_N			US1_CS #0	
L2	PC5	ACMP0_CH5		LETIM0_OUT1 #3 PCNT1_S1IN #0	US2_CS #0	
L3	PA14			TIM2_CC2 #1		
L4	IOVDD_1	Digital IO power supply 1.				
L5	PB11	DAC0_OUT0		LETIM0_OUT0 #1		
L6	PB12	DAC0_OUT1		LETIM0_OUT1 #1		
L7	AVSS_2	Analog ground 2.				
L8	PB13	HFXTAL_P			LEU0_TX #1	
L9	PB14	HFXTAL_N			LEU0_RX #1	
L10	AVDD_0	Analog power supply 0.				
L11	PD0	ADC0_CH0		PCNT2_S0IN #0	US1_TX #1	

4.2 Alternate functionality pinout

A wide selection of alternate functionality is available for multiplexing to various pins. This is shown in Table 4.2 (p. 51). The table shows the name of the alternate functionality in the first column, followed by columns showing the possible LOCATION bitfield settings.

Note

Some functionality, such as analog interfaces, do not have alternate settings or a LOCATION bitfield. In these cases, the pinout is shown in the column corresponding to LOCATION 0.

Table 4.2. Alternate functionality overview

Alternate	LOCATION				
Functionality	0	1	2	3	Description
ACMP0_CH0	PC0				Analog comparator ACMP0, channel 0.
ACMP0_CH1	PC1				Analog comparator ACMP0, channel 1.
ACMP0_CH2	PC2				Analog comparator ACMP0, channel 2.
ACMP0_CH3	PC3				Analog comparator ACMP0, channel 3.
ACMP0_CH4	PC4				Analog comparator ACMP0, channel 4.
ACMP0_CH5	PC5				Analog comparator ACMP0, channel 5.
ACMP0_CH6	PC6				Analog comparator ACMP0, channel 6.
ACMP0_CH7	PC7				Analog comparator ACMP0, channel 7.
ACMP0_O	PE13	PE2			Analog comparator ACMP0, digital output.
ACMP1_CH0	PC8				Analog comparator ACMP1, channel 0.
ACMP1_CH1	PC9				Analog comparator ACMP1, channel 1.
ACMP1_CH2	PC10				Analog comparator ACMP1, channel 2.
ACMP1_CH3	PC11				Analog comparator ACMP1, channel 3.
ACMP1_CH4	PC12				Analog comparator ACMP1, channel 4.
ACMP1_CH5	PC13				Analog comparator ACMP1, channel 5.
ACMP1_CH6	PC14				Analog comparator ACMP1, channel 6.
ACMP1_CH7	PC15				Analog comparator ACMP1, channel 7.
ACMP1_O	PF2	PE3			Analog comparator ACMP1, digital output.
ADC0_CH0	PD0				Analog to digital converter ADC0, input channel number 0.
ADC0_CH1	PD1				Analog to digital converter ADC0, input channel number 1.
ADC0_CH2	PD2				Analog to digital converter ADC0, input channel number 2.
ADC0_CH3	PD3				Analog to digital converter ADC0, input channel number 3.
ADC0_CH4	PD4				Analog to digital converter ADC0, input channel number 4.
ADC0_CH5	PD5				Analog to digital converter ADC0, input channel number 5.
ADC0_CH6	PD6				Analog to digital converter ADC0, input channel number 6.
ADC0_CH7	PD7				Analog to digital converter ADC0, input channel number 7.
CMU_CLK0	PA2	PC12			Clock Management Unit, clock output number 0.
CMU_CLK1	PA1	PD8			Clock Management Unit, clock output number 1.
DAC0_OUT0	PB11				Digital to Analog Converter DAC0 output channel number 0.
DAC0_OUT1	PB12				Digital to Analog Converter DAC0 output channel number 1.
DBG_SWCLK	PF0	PF0			Debug-interface Serial Wire clock input.

Alternate	LOCATION				
Functionality	0	1	2	3	Description
					Note that this function is enabled to pin out of reset, and has a built-in pull down.
DBG_SWDIO	PF1	PF1			Debug-interface Serial Wire data input / output. Note that this function is enabled to pin out of reset, and has a built-in pull up.
DBG_SWO	PF2	PC15			Debug-interface Serial Wire viewer Output. Note that this function is not enabled after reset, and must be enabled by software to be used.
EBI_AD00	PE8				External Bus Interface (EBI) address and data input / output pin 00.
EBI_AD01	PE9				External Bus Interface (EBI) address and data input / output pin 01.
EBI_AD02	PE10				External Bus Interface (EBI) address and data input / output pin 02.
EBI_AD03	PE11				External Bus Interface (EBI) address and data input / output pin 03.
EBI_AD04	PE12				External Bus Interface (EBI) address and data input / output pin 04.
EBI_AD05	PE13				External Bus Interface (EBI) address and data input / output pin 05.
EBI_AD06	PE14				External Bus Interface (EBI) address and data input / output pin 06.
EBI_AD07	PE15				External Bus Interface (EBI) address and data input / output pin 07.
EBI_AD08	PA15				External Bus Interface (EBI) address and data input / output pin 08.
EBI_AD09	PA0				External Bus Interface (EBI) address and data input / output pin 09.
EBI_AD10	PA1				External Bus Interface (EBI) address and data input / output pin 10.
EBI_AD11	PA2				External Bus Interface (EBI) address and data input / output pin 11.
EBI_AD12	PA3				External Bus Interface (EBI) address and data input / output pin 12.
EBI_AD13	PA4				External Bus Interface (EBI) address and data input / output pin 13.
EBI_AD14	PA5				External Bus Interface (EBI) address and data input / output pin 14.
EBI_AD15	PA6				External Bus Interface (EBI) address and data input / output pin 15.
EBI_ALE	PF3				External Bus Interface (EBI) Address Latch Enable output.
EBI_ARDY	PF2				External Bus Interface (EBI) Hardware Ready Control input.
EBI_CS0	PD9				External Bus Interface (EBI) Chip Select output 0.
EBI_CS1	PD10				External Bus Interface (EBI) Chip Select output 1.
EBI_CS2	PD11				External Bus Interface (EBI) Chip Select output 2.
EBI_CS3	PD12				External Bus Interface (EBI) Chip Select output 3.
EBI_REn	PF5				External Bus Interface (EBI) Read Enable output.
EBI_WEn	PF4				External Bus Interface (EBI) Write Enable output.
HFXTAL_N	PB14				High Frequency Crystal (4 - 32 MHz) negative pin. Also used as external optional clock input pin.
HFXTAL_P	PB13				High Frequency Crystal (4 - 32 MHz) positive pin.
I2C0_SCL	PA1	PD7	PC7	PD15	I2C0 Serial Clock Line input / output.
I2C0_SDA	PA0	PD6	PC6	PD14	I2C0 Serial Data input / output.
LETIM0_OUT0	PD6	PB11	PF0	PC4	Low Energy Timer LETIM0, output channel 0.
LETIM0_OUT1	PD7	PB12	PF1	PC5	Low Energy Timer LETIM0, output channel 1.
LEU0_RX	PD5	PB14	PE15		LEUART0 Receive input.
LEU0_TX	PD4	PB13	PE14		LEUART0 Transmit output. Also used as receive input in half duplex communication.
LEU1_RX	PC7	PA6			LEUART1 Receive input.
LEU1_TX	PC6	PA5			LEUART1 Transmit output. Also used as receive input in half duplex communication.

Alternate	LOCATION				
Functionality	0	1	2	3	Description
LFXTAL_N	PB8				Low Frequency Crystal (typically 32.768 kHz) negative pin. Also used as an optional external clock input pin.
LFXTAL_P	PB7				Low Frequency Crystal (typically 32.768 kHz) positive pin.
PCNT0_S0IN	PC13	PE0	PC0		Pulse Counter PCNT0 input number 0.
PCNT0_S1IN	PC14	PE1	PC1		Pulse Counter PCNT0 input number 1.
PCNT1_S0IN	PC4	PB3			Pulse Counter PCNT1 input number 0.
PCNT1_S1IN	PC5	PB4			Pulse Counter PCNT1 input number 1.
PCNT2_S0IN	PD0	PE8			Pulse Counter PCNT2 input number 0.
PCNT2_S1IN	PD1	PE9			Pulse Counter PCNT2 input number 1.
TIM0_CC0	PA0	PA0	PF6	PD1	Timer 0 Capture Compare input / output channel 0.
TIM0_CC1	PA1	PA1	PF7	PD2	Timer 0 Capture Compare input / output channel 1.
TIM0_CC2	PA2	PA2	PF8	PD3	Timer 0 Capture Compare input / output channel 2.
TIM0_CDTI0	PA3	PC13	PF3	PC13	Timer 0 Complimentary Deat Time Insertion channel 0.
TIM0_CDTI1	PA4	PC14	PF4	PC14	Timer 0 Complimentary Deat Time Insertion channel 1.
TIM0_CDTI2	PA5	PC15	PF5	PC15	Timer 0 Complimentary Deat Time Insertion channel 2.
TIM1_CC0	PC13	PE10	PB0		Timer 1 Capture Compare input / output channel 0.
TIM1_CC1	PC14	PE11	PB1		Timer 1 Capture Compare input / output channel 1.
TIM1_CC2	PC15	PE12	PB2		Timer 1 Capture Compare input / output channel 2.
TIM2_CC0	PA8	PA12	PC8		Timer 2 Capture Compare input / output channel 0.
TIM2_CC1	PA9	PA13	PC9		Timer 2 Capture Compare input / output channel 1.
TIM2_CC2	PA10	PA14	PC10		Timer 2 Capture Compare input / output channel 2.
U0_RX	PF7	PE1	PA4	PC15	UART0 Receive input.
U0_TX	PF6	PE0	PA3	PC14	UART0 Transmit output. Also used as receive input in half duplex communication.
US0_CLK	PE12	PE5	PC9		USART0 clock input / output.
US0_CS	PE13	PE4	PC8		USART0 chip select input / output.
US0_RX	PE11	PE6	PC10		USART0 Asynchronous Receive. USART0 Synchronous mode Master Input / Slave Output (MISO).
US0_TX	PE10	PE7	PC11		USART0 Asynchronous Transmit.Also used as receive input in half duplex communication. USART0 Synchronous mode Master Output / Slave Input (MOSI).
US1_CLK	PB7	PD2			USART1 clock input / output.
US1_CS	PB8	PD3			USART1 chip select input / output.
US1_RX	PC1	PD1			USART1 Asynchronous Receive. USART1 Synchronous mode Master Input / Slave Output (MISO).
US1_TX	PC0	PD0			USART1 Asynchronous Transmit.Also used as receive input in half duplex communication. USART1 Synchronous mode Master Output / Slave Input (MOSI).
US2_CLK	PC4	PB5			USART2 clock input / output.
US2_CS	PC5	PB6			USART2 chip select input / output.
US2_RX	PC3	PB4			USART2 Asynchronous Receive. USART2 Synchronous mode Master Input / Slave Output (MISO).
US2_TX	PC2	PB3			USART2 Asynchronous Transmit.Also used as receive input in half duplex communication.

Alternate	LOCATION				
Functionality	0	1	2	3	Description
					USART2 Synchronous mode Master Output / Slave Input (MOSI).

4.3 GPIO pinout overview

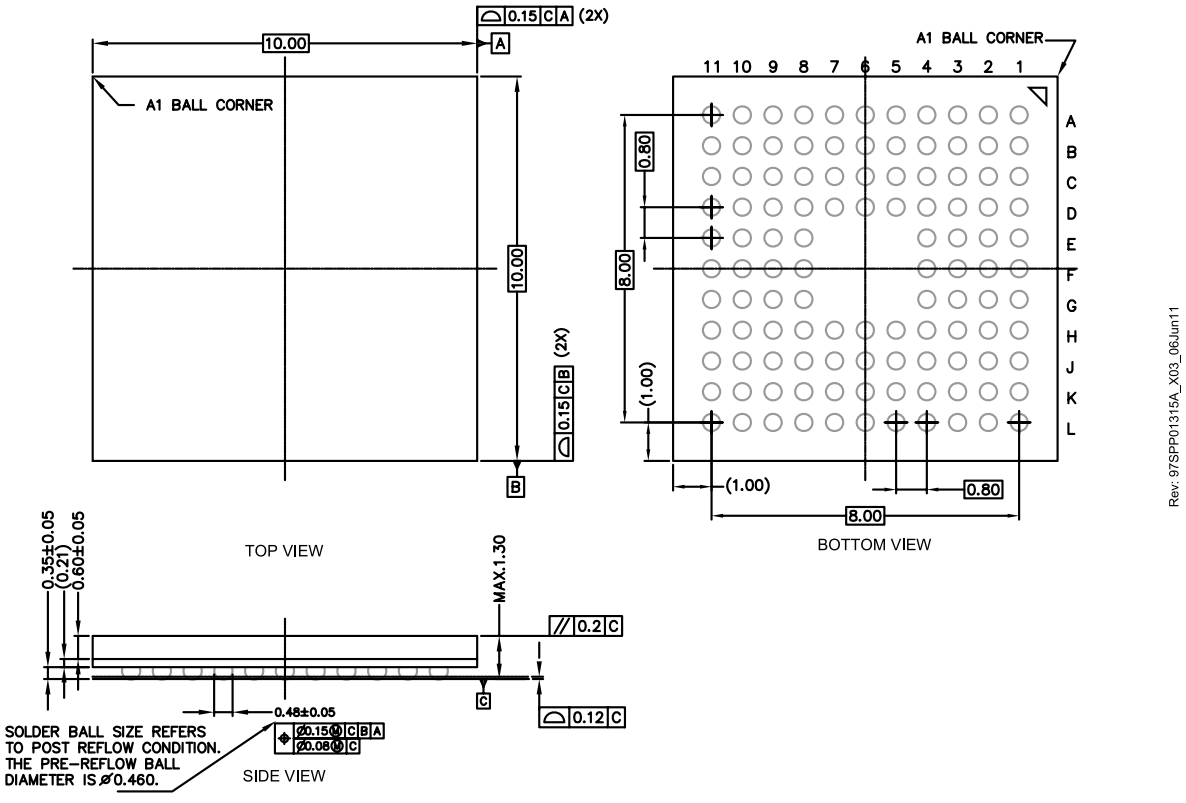
The specific GPIO pins available in *EFM32G290* is shown in Table 4.3 (p. 54). Each GPIO port is organized as 16-bit ports indicated by letters A through F, and the individual pin on this port in indicated by a number from 15 down to 0.

Table 4.3. GPIO Pinout

Port	Pin 15	Pin 14	Pin 13	Pin 12	Pin 11	Pin 10	Pin 9	Pin 8	Pin 7	Pin 6	Pin 5	Pin 4	Pin 3	Pin 2	Pin 1	Pin 0
Port A	PA15	PA14	PA13	PA12	PA11	PA10	PA9	PA8	PA7	PA6	PA5	PA4	PA3	PA2	PA1	PA0
Port B	PB15	PB14	PB13	PB12	PB11	PB10	PB9	PB8	PB7	PB6	PB5	PB4	PB3	PB2	PB1	PB0
Port C	PC15	PC14	PC13	PC12	PC11	PC10	PC9	PC8	PC7	PC6	PC5	PC4	PC3	PC2	PC1	PC0
Port D	PD15	PD14	PD13	PD12	PD11	PD10	PD9	PD8	PD7	PD6	PD5	PD4	PD3	PD2	PD1	PD0
Port E	PE15	PE14	PE13	PE12	PE11	PE10	PE9	PE8	PE7	PE6	PE5	PE4	PE3	PE2	PE1	PE0
Port F	-	-	-	-	-	-	PF9	PF8	PF7	PF6	PF5	PF4	PF3	PF2	PF1	PF0

4.4 BGA112 Package

Figure 4.2. BGA112



Note:

1. The dimensions in parenthesis are reference.

2. Datum 'C' and seating plane are defined by the crown of the solder balls.
3. All dimensions are in millimeters.

The BGA112 Package uses Sn96.5/Ag3/Cu0.5 solderballs.

All EFM32 packages are RoHS compliant and free of Bromine (Br) and Antimony (Sb).

5 PCB Layout and Soldering

5.1 Recommended PCB Layout

Figure 5.1. BGA112 PCB Land Pattern

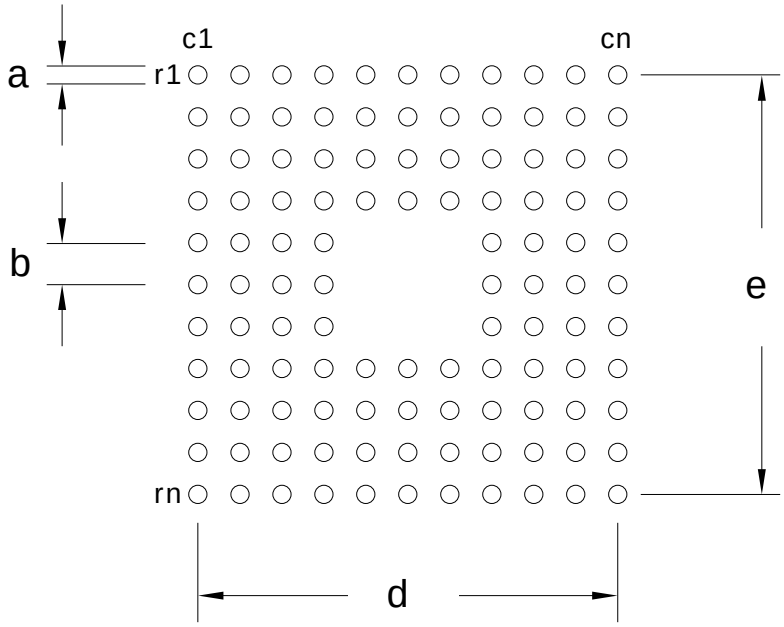


Table 5.1. BGA112 PCB Land Pattern Dimensions (Dimensions in mm)

Symbol	Dim. (mm)	Symbol	Row name and column number
a	0.35	r1	A
b	0.80	rn	L
d	8.00	c1	1
e	8.00	cn	11

Figure 5.2. BGA112 PCB Solder Mask

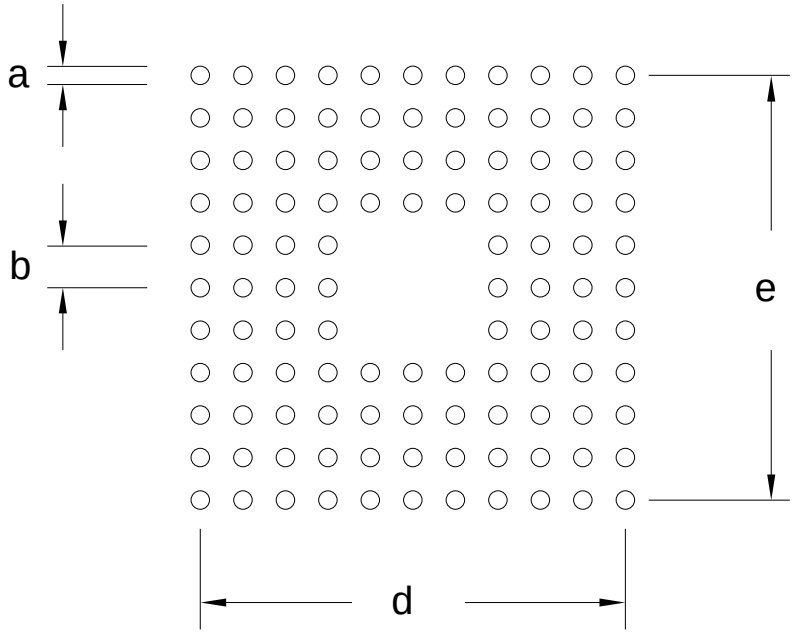


Table 5.2. BGA112 PCB Solder Mask Dimensions (Dimensions in mm)

Symbol	Dim. (mm)
a	0.48
b	0.80
d	8.00
e	8.00

Figure 5.3. BGA112 PCB Stencil Design

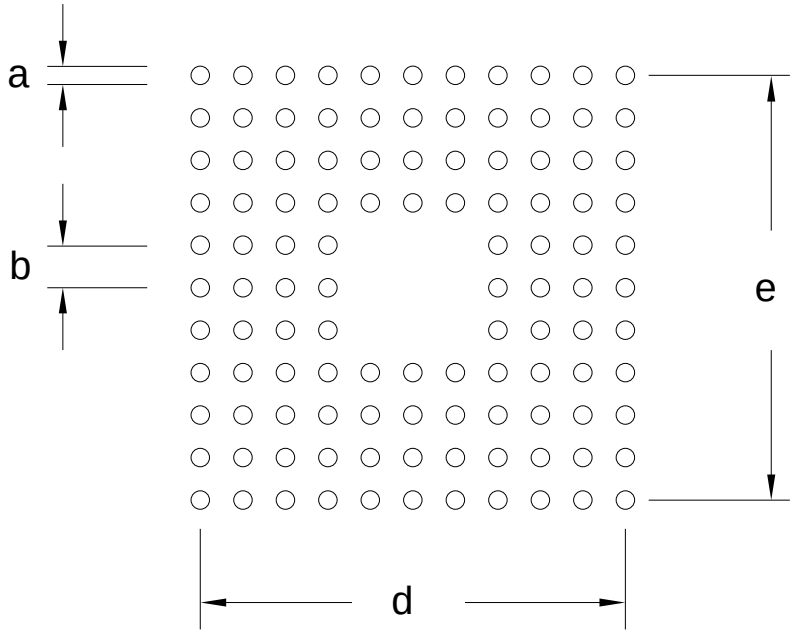


Table 5.3. BGA112 PCB Stencil Design Dimensions (Dimensions in mm)

Symbol	Dim. (mm)
a	0.33
b	0.80
d	8.00
e	8.00

1. The drawings are not to scale.
2. All dimensions are in millimeters.
3. All drawings are subject to change without notice.
4. The PCB Land Pattern drawing is in compliance with IPC-7351B.
5. Stencil thickness 0.125 mm.

5.2 Soldering Information

The latest IPC/JEDEC J-STD-020 recommendations for Pb-Free reflow soldering should be followed.

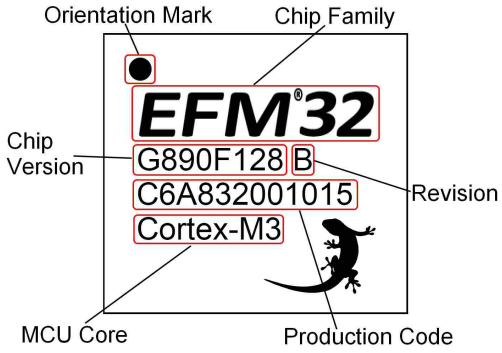
The packages have a Moisture Sensitivity Level rating of 3, please see the latest IPC/JEDEC J-STD-033 standard for MSL description and level 3 bake conditions.

6 Chip Marking, Revision and Errata

6.1 Chip Marking

In the illustration below package fields and position are shown.

Figure 6.1. Example Chip Marking



6.2 Revision

The revision of a chip can be determined from the "Revision" field in Figure 6.1 (p. 59). If the revision says "ES" (Engineering Sample), the revision must be read out electronically as specified in the reference manual.

6.3 Errata

Please see the dxxxx_efm32g290_errata.pdf for description and resolution of device erratas. This document is available in Simplicity Studio or online at http://www.energymicro.com/downloads/datasheets.

7 Revision History

7.1 Revision 1.40

February 27nd, 2012

Updated Power Managment section.

Corrected operating voltage from 1.8 V to 1.85 V.

Corrected $TGRAD_{ADCTH}$ parameter.

Corrected BGA112 package drawing.

Updated PCB land pattern, solder mask and stencil design.

7.2 Revision 1.30

May 20th, 2011

Updated LFXO load capacitance section

7.3 Revision 1.20

December 17th, 2010

Increased max storage temperature.

Added data for <150°C and <70°C on Flash data retention.

Changed latch-up sensitivity test description.

Added IO leakage current

Added Flash current consumption

Updated HFRCO data

Updated LFRCO data

Added graph for ADC Absolute Offset over temperature

Added graph for ADC Temperature sensor readout

7.4 Revision 1.11

November 17th, 2010

Corrected maximum DAC clock speed for continuous mode.

Added DAC sample-hold mode voltage drift rate.

Added pulse widths detected by the HFXO glitch detector.

Added power sequencing information to Power Management section.

7.5 Revision 1.10

September 13th, 2010

Added typical values for $R_{ADCFILT}$ and $C_{ADCFILT}$.

Added two conditions for DAC clock frequency; one for sample/hold and one for sample/off.

Added RoHS information and specified leadframe/solderballs material.

Added Serial Bootloader to feature list and system summary.

Updated ADC characterization data.

Updated DAC characterization data.

Updated RCO characterization data.

Updated ACMP characterization data.

Updated VCMP characterization data.

7.6 Revision 1.00

April 23rd, 2010

ADC_VCM line removed.

Added pinout illustration and additional pinout table.

Changed "Errata" chapter. Errata description moved to separate document.

Document changed status from "Preliminary".

Updated "Electrical Characteristics" chapter.

7.7 Revision 0.85

February 19th, 2010

Renamed DBG_SWV pin to DBG_SWO.

7.8 Revision 0.83

January 25th, 2010

Updated errata section.

Specified flash word width in Section 3.7 (p. 19)

Added Capacitive Sense Internal Resistor values in Section 3.12 (p. 43) .

7.9 Revision 0.82

December 9th, 2009

Updated conctact information.

ADC current consumption numbers updated in Section 3.10 (p. 33)

7.10 Revision 0.81

November 20th, 2009

Section 3.1 (p. 9) updated.

Storage temperature in Section 3.2 (p. 9) updated.

Temperature coefficient of band-gap reference in Section 3.6 (p. 18) added.

Erase times in Section 3.7 (p. 19) updated.

Definitions of DNL and INL added in Figure 3.28 (p. 37) and Figure 3.29 (p. 37) .

Current consumption of digital peripherals added in Section 3.14 (p. 45) .

Pinout information in Table 4.1 (p. 47) corrected.

Updated errata section.

7.11 Revision 0.80

Initial preliminary revision, October 19th, 2009

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