S8051XC3

Super-Fast 8051 Microcontroller Core with Configurable Features and Peripherals

The S8051XC3 IP core implements a high-performance, low-energy, 8-bit microcontroller that executes the MCS®51 instruction set and includes a configurable range of features and integrated peripherals.

The core's sophisticated architecture yields the fastest 8051-compatible 8-bit MCU available anywhere (at the time of its release). It runs with a single clock per machine cycle, and requires an average of 1.5 to 1.8 machine cycles per instruction, depending on configuration. Dhrystone 2.1 tests show it to run from 9.41 to 26.85 times faster than the original 8051 at the same frequency, without requiring an external arithmetic acceleration unit (such as an MDU). Representative 65nm LP ASIC results have reached 500 MHz, for an effective speed-up of 1,000 times over 80C51 chips. Interrupt latency is a remarkably low two cycles.

The S8051XC3 is also one of the most energy efficient 8-bit processors available. Its small silicon footprint—the CPU size can be under 6,500 gates—means very little power leakage. Furthermore, dynamic power of the CPU at a 40nm technology is as low as 2.3µW/MHz, and its higher performance allows clocking at lower frequencies. The core allows energy consumption to be adjusted to the processing workload via dynamic frequency scaling and independent control of the CPU and peripherals clock.

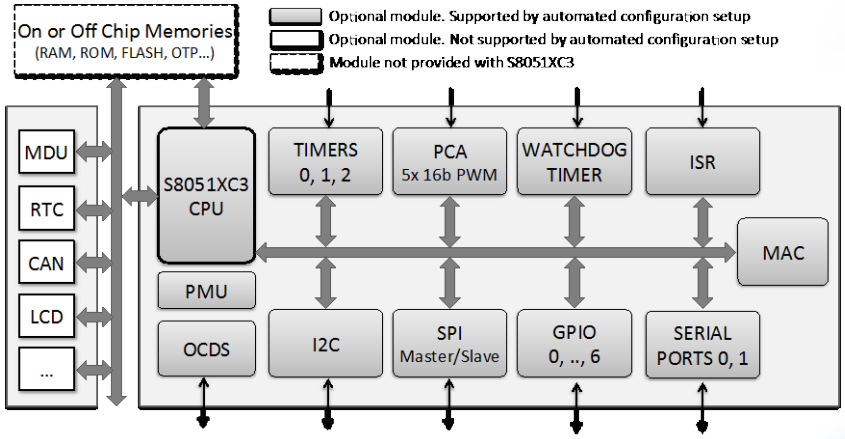
The core's rich set of optional features and integrated peripherals allows designers to adjust performance and silicon requirements to best match an application's specific requirements. (Several pre-configured versions at different price points are also available.) Software development is facilitated by a single-wire or JTAG debugging interface, which operates seamlessly within IDEs such as those from IAR and Keil.

This new core builds on CAST's experience with hundreds of 8051 IP customers going back to 1997. Designed for easy reuse in ASICs, structured ASICs, or FPGAs, the core is strictly synchronous, with positive-edge clocking (except in the optional debug & SPI modules), synchronous or asynchronous reset, and no internal tri-states.

Applications

The royalty-free S8051XC3 is a resource- and cost-effective solution for offloading main processors in complex SoCs, running deeply embedded systems, or managing analog sensors and other peripherals in IP subsystems. Application areas include Internet of Things (IoT) and wearable electronic devices, industrial control systems, and more.

Block Diagram



Features

Fully compatible with the MCS®51 instruction set

Best Performance Available

- Up to 26.85x speed-up over the original 8051 at the same clock
- More than 1,000 times faster than the original 8051 when clocked at maximum frequency

Energy Efficient

- Small silicon footprint for less power leakage, lower static power consumption
- Better DMIPs/MHz power ratio allows energy to be saved by operating at a lower frequency
- Ultra-low dynamic power (2.3µW/MHz in 40nm)
- Advanced power management supports dynamic frequency scaling, and CPU and/or peripherals clock gating

Configurable Microcontroller

- Automatic instantiation of user selectable MCU peripherals
- Pre-integration with other CAST IP on request
- User-configurable CPU and memory architecture to match application needs

Easy Firmware Development

- CDP-XC on-chip debug interface, supports JTAG and Single-Wire
- USB-based, low cost CDP-XC debug pods
- Integration with IAR Embedded Workbench & Keil uVision™ IDEs
- Software and Hardware breakpoints, and Trace
- Cycle-accurate Simulation Model

Flexible Memory Architecture

- 64KB or 8MB address space
- 8, 16, or 32-bit memory interface
- Integration with slow memories or peripherals easier with acknowledged transactions
- Independent XTEM bus
- Optional extra 16-bit or 24-bit DPTR

Efficient Interrupts Handling

- Up to 23 interrupts, with 2 or 4 interrupt priority levels
- Ultra-low interrupt latency: two cycles from interrupt assertion to ISR start

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Peripheral and Options

S8051XC3 users can select among a rich set of pre-integrated and pre-verified peripherals and core options. (Verilog defines, e.g. ‘define USE_PMU, are used for this purpose.) Options not included by default but that can be added on request are noted by *italics*.

Timers/Counters

- **Timer 0 & 1**: 80C51-like 16-bit timers/counters
- **Timer 2**: 80515-like 16-bit counter, with compare/capture unit
- **PCA**: 80251-like programmable counter array with 5 PWM channels
- **WDT**: 80251-like Watchdog Timer

Interfaces

- **I2C 0 & 1**: Master-Slave ports for the Phillips Inter-Integrated Circuit (I2C) serial bus
- **SPI**: Master-Slave port for the Serial Peripheral bus Interface serial bus
- **Serial 0**: 80C51- or 80251-like Full-Duplex UART/USART
- **GPIO 0-4**: 80C51-like 8-bit parallel ports
- ***GPIO 5****: 80C515-like parallel port 5*
- ***GPIO 6****: 80C451-like, printer-like 8-bit parallel port 6*
- **SFR**: Up to 112 Special Function Registers Interface
- **ISR**: 80251-like Interrupt Controller with up 23 sources, and two or four priority levels***CAN****: CANBus 2.0 and FD Controller*
- ***LIN:*** *Local Interconnect Network (LIN) Bus Controller*
- ***LCD/TFT:*** *LCD or TFT display controller*
- **OCDS**: On-chip debugging system interface

Arithmetic Units

- ***MDU***: Multiply Divide Unit for 16 x 16-bit multiplication, 32/16- and 16/16-bit division, and 32-bit normalization and L/R shifting
- **MAC**: Multiply-Accumulate Unit (16 x 16-bit multiplication/40-bit accumulator)

Performance Acceleration & Architectural Options

- **AIEA**: Advanced instruction execution architecture, which includes a number of performance optimizations
- *VDMA*: Direct Memory Access controller, with up to eight channels**D-DPTR**: Dual Data Pointers with Automated Increment/Decrement/Switch capability
- **32MIF:** 32-bit memory code/date memory interface
- **PMU:** Power management unit

Available Versions

Three versions of the core are available, offering a range of capabilities and prices:

- **S8051XC3-F** includes all options, and is user-configurable.
- **S8051XC3-C** retains configurability of the -F version, with these exceptions: a) only allows for 8-bit memory data/code memory interfaces; b) some features of the advanced instruction execution architecture are disabled, limiting the performance to 15.62x the performance of the original 80C51; and c) I2C, SPI and RTC are not included.
- **S8051XC3-A** includes user-configurable options matching the original Intel 8051 peripheral set: 64kB memory interface, two timers, one serial port, four parallel I/O Ports, two-level interrupt controller, and one DPTR register.

Implementation Results and Performance

The Dhrystone 2.1 benchmark score varies from 0.088 to 0.252 DMIPS/MHz, which translates to speed improvements from 9.4 to 26.85 times over the standard 80C51 assuming the same clock frequency, or 350x to more than 1,000 times increase when the S8051XC3 is clocked at 450MHz.

Sample Dhrystone 2.1 benchmark results are as follows.

Version	DMIPS/MHz	80C51 Ratio
S8051XC3-F	0.252	26.8
S8051XC3-C	0.147	15.6
S8051XC3-A	0.088	9.4

Reference designs have been evaluated in a variety of technologies. The following are sample results for the cores CPU using a 90nm ASIC technology.

Version	Maximum Speed	Minimum Area
S8051XC3-F	355 MHz	11.5k gates
S8051XC3-C	395 MHz	9.3k gates
S8051XC3-A	475 MHz	6.2k gates

Deliverables

The core is available in Verilog RTL or as targeted FPGA netlist, and its deliverables include everything required for a successful implementation, including a behavioral model, an automated constrained random verification (CRV) test-bench, comprehensive documentation, and sample synthesis and simulation scripts. Hardware debug pods and reference design boards are also available.

Support

The core as delivered is warranted against defects for ninety days from purchase. Thirty days of phone and email technical support are included, starting with the first interaction. Additional maintenance and support options are available; contact CAST Sales.

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