8-bit Microcontroller with A/D converter

1. Description

The T80C5112 is a high performance ROM/OTP version of the 80C51 8-bit microcontroller.

The T80C5112 retains all the features of the standard 80C51 with 8 Kbytes ROM/OTP program memory, 256 bytes of internal RAM, a 8-source , 4-level interrupt system, an on-chip oscillator and two timer/counters.

The T80C5112 is dedicated for analog interfacing applications. For this, it has an 10-bit, 8 channels A/D converter and a five channels Programmable Counter Array.

In addition, the T80C5112 has a Hardware Watchdog Timer with its own low power oscillator, a versatile serial channel that facilitates multiprocessor communication (EUART) with an independent baud rate generator, a SPI serial bus controller and a X2 speed improvement mechanism. The X2 feature allows to keep the same CPU power at a divided by two oscillator frequency.

The fully static design of the T80C5112 allows to reduce system power consumption by bringing the clock frequency down to any value, even DC, without loss of data.

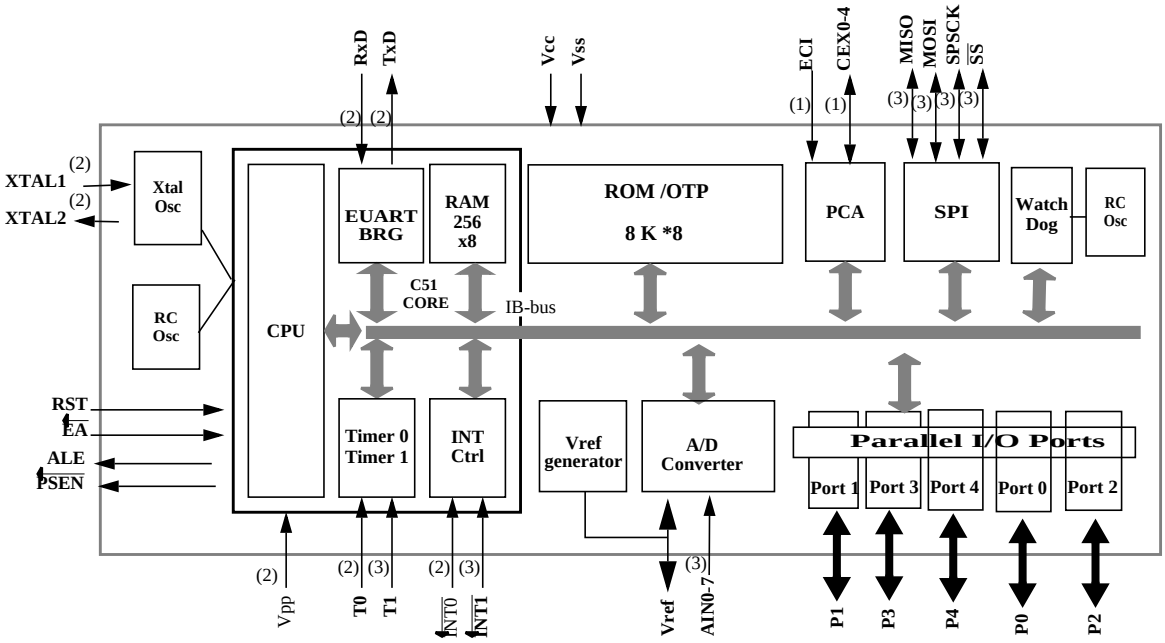
The T80C5112 has 3 software-selectable modes of reduced activity for further reduction in power consumption. In the idle mode the CPU is frozen while the peripherals are still operating. In the quiet mode, the A/D converter only is operating. In the power-down mode the RAM is saved and all other functions are inoperative. Two oscillators source, crystal and RC, provide a versatile power management.

The T80C5112 is proposed in 48/52 pin count packages with Port 0 and Port 2 (address / data busses).

2. Features

- 80C51 Compatible
  - Five I/O ports
  - Two 16-bit timer/counters
  - 256 bytes RAM
- 8Kbytes ROM/OTP program memory with 64 bytes encryption array and 3 security levels.
- High-Speed Architecture
  - 33MHz @ 5V (66 MHz equivalent)
  - 20MHz @ 3V (40 MHz equivalent)
  - X2 Speed Improvement capability (6 clocks/ machine cycle)
- 10-bit, 8 channels A/D converter
- Hardware Watchdog Timer with integrated low power oscillator (20µA) and Reset-Out
- Programmable I/O mode: standard C51, input only, push-pull, open drain.
- Asynchronous port reset, Power On Reset
- Full duplex Enhanced UART with baud rate generator
- SPI, master/slave mode
- Dual system clock
  - Crystal or ceramic oscillator with hardware set up (32 KHz or 33/40 MHz)
  - Internal RC oscillator (12 MHz)
  - Programmable prescaler
  - Active oscillator during reset defined by hardware set up
  - Timer 0 subclock mode for Real Time Clock.
- Programmable counter array with High speed output, Compare / Capture, Pulse Width Modulation and Watchdog timer capabilities
- Interrupt Structure with:
  - 8 Interrupt sources,
  - 4 interrupt priority levels
- Power Control modes:
  - Idle mode
  - Power-down mode
  - Power-off Flag, Power fail detect, Power on Reset
- Power supply: 2.7 to 5.5V
- Temperature ranges: Commercial (0 to 70C) and Industrial (-40 to 85 C), optionnal extented
- Package:LQFP48 (body 7*7*1.4mm), PLCC52

3. Block Diagram



(1): Alternate function of Port 1

(2): Alternate function of Port 3

(3): Alternate function of Port 4

4. alias SFR Mapping

The Special Function Registers (SFRs) of the T80C5112 belongs to the following categories:

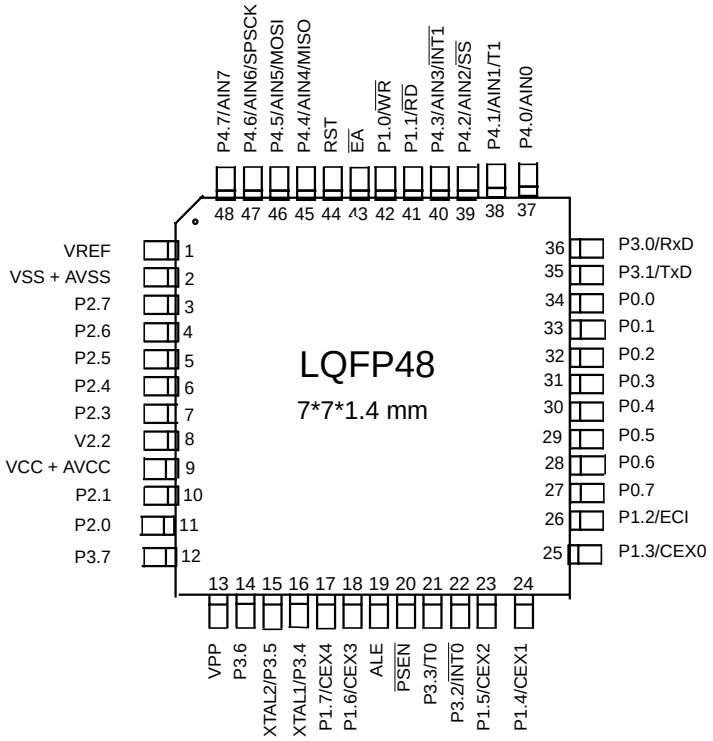
- C51 core registers: ACC, B, DPH, DPL, PSW, SP, AUXR, AUXR1
- I/O port registers: P0, P1, P2, P3, P4, P1M1, P1M2, P3M1, P3M2, P4M1, P4M2
- Timer registers: TCON, TH0, TH1, TMOD, TL0, TL1
- Serial I/O port registers: SADDR, SADEN, SBUF, SCON, BRL, BDRCON
- Power and clock control registers: CKCON0, CKCON1, OSCCON, CKSEL, PCON, CKRL
- Interrupt system registers: IE, IE1, IPL0, IPL1, IPH0, IPH1
- WatchDog Timer: WDTRST, WDTPRG
- SPI: SPCON, SPSTA, SPDAT
- PCA: CCAP0L, CCAP1L, CCAP2L, CCAP3L, CCAP4L, CCAP0H, CCAP1H, CCAP2H, CCAP3H, CCAP4H, CCAPM0, CCAPM1, CCAPM2, CCAPM3, CCAPM4, CL, CH, CMOD, CCON
- ADC: ADCCON, ADCCLK, ADCDATH, ADCDATL, ADCF

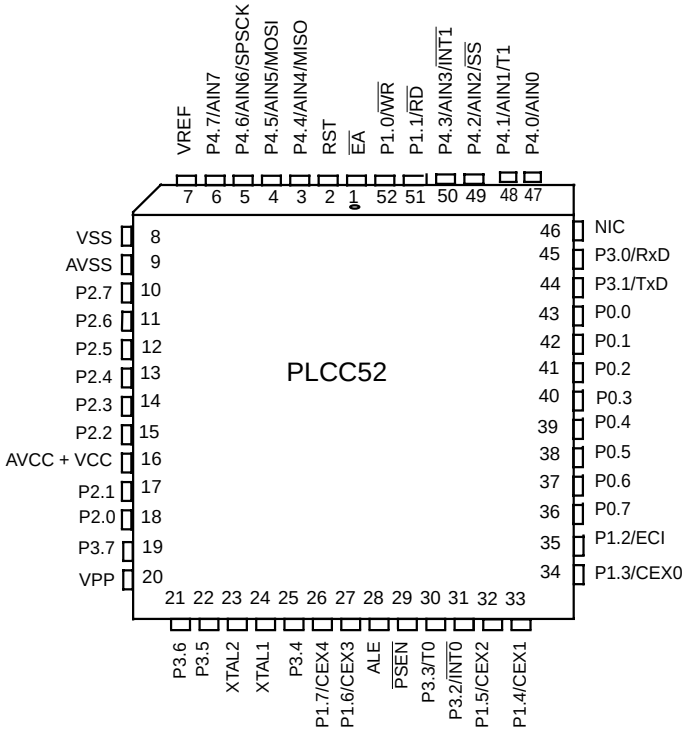
Table 1. SFR Addresses and Reset Values

	0/8	1/9	2/A	3/B	4/C	5/D	6/E	7/F	
F8h		CH 0000 0000	CCAP0H XXXX XXXX	CCAP1H XXXX XXXX	CCAP2H XXXX XXXX	CCAP3H XXXX XXXX	CCAP4H XXXX XXXX		FFh
F0h	B 0000 0000		ADCLK 0000 0000	ADCON 0000 0000	ADDL XXXXXX00	ADDH 0000 0000	ADCF 0000 0000		F7h
E8h		CL 0000 0000	CCAP0L XXXX XXXX	CCAP1L XXXX XXXX	CCAP2L XXXX XXXX	CCAP3L XXXX XXXX	CCAP4L XXXX XXXX	CONF 1111 111X	EFh
E0h	ACC 0000 0000		P1M2 0000 0000		P3M2 0000 0000	P4M2 0000 0000			E7h
D8h	CCON 00X0 0000	CMOD X000 0000	CCAPM0 00XX X000	CCAPM1 X000 0000	CCAPM2 X000 0000	CCAPM3 X000 0000	CCAPM4 X000 0000		DFh
D0h	PSW 0000 0000				P1M1 0000 0000	P3M1 0000 0000	P4M1 0000 0000		D7h
C8h									CFh
C0h	P4 1111 1111			SPCON 0001 0100	SPSTA XXXXXXXX	SPDAT XXXX XXXX			C7h
B8h	IPL0 0000 0000	SADEN 0000 0000							BFh
B0h	P3 1111 1111	IE1 0000 0000	IPL1 0000 0000	IPH1 0000 0000				IPH0 X000 0000	B7h
A8h	IE0 0000 0000	SADDR 0000 0000						CKCON1 XXXX XXX0	AFh
A0h	P2 1111 1111		AUXR1 XXXXXXX0				WDRST 0000 0000	WDTPRG 0000 0000	A7h
98h	SCON 0000 0000	SBUF XXXX XXXX	BRL 0000 0000	BDRCON 0000 0000					9Fh
90h	P1 1111 1111							CKRL 1111 1111	97h
88h	TCON 0000 0000	TMOD 0000 0000	TL0 0000 0000	TL1 0000 0000	TH0 0000 0000	TH1 0000 0000	AUXR XXXXXXX0	CKCON0 X000X000	8Fh
80h	P0 1111 1111	SP 0000 0111	DPL 0000 0000	DPH 0000 0000		CKSEL XXXX XXXC	OSCCON XXXX XXCC	PCON 00X1 0000	87h
	0/8	1/9	2/A	3/B	4/C	5/D	6/E	7/F	

Notes: "C", value defined by the configuration byte, see Section “Configuration byte”, page 11

5. Pin Configuration





*NIC: No Internal Connection

MNEMONIC	PIN NUMBER		TYPE	NAME AND FUNCTION
	LQFP	PLCC		
	48	52		
V_{SS}	X	X	I	**Ground:** 0V reference.
V_{CC}	X	X	I	**Power Supply:** This is the power supply voltage for normal, idle and power-down operation.
AV_{SS}		X	I	**Analog Ground:** 0V reference.
AV_{CC}			I	**Analog Power Supply:** This is the power supply voltage for normal and idle operation of the A/D
VREF	X	X	I	**VREF :** A/D converter positive reference input.
VPP	X	X	I	**Vpp :** Programming Supply Voltage: This pin also receives the 12V programming pulse which will start the EPROM programming and the manufacturer test modes.
P1.0-P1.7	X	X	I/O	Port 1: Port 1 is an 8-bit bidirectional I/O port with internal pull-ups. Port 1 pins that have 1s written to them are pulled high by the internal pull-ups and can be used as inputs. Alternate functions for Port 1 include:
			I/O	**$\overline{WR}$ (P1.0):** External data memory write strobe
			I/O	**$\overline{RD}$ (P1.1):** External data memory readstrobe
			I/O	**ECI (P1.2):** External Clock for the PCA
			I/O	**CEX0 (P1.3):** Capture/Compare External I/O for PCA module 0
			I/O	**CEX1 (P1.4):** Capture/Compare External I/O for PCA module 1
			I/O	**CEX2 (P1.5):** Capture/Compare External I/O for PCA module 2
			I/O	**CEX3 (P1.6):** Capture/Compare External I/O for PCA module 3
			I/O	**CEX4 (P1.7):** Capture/Compare External I/O for PCA module 4
P3.0-P3.7	X	X	I/O	Port 3: Port 3 is an 8-bit bidirectional I/O port with internal pull-ups. Port 3 pins that have 1s written to them are pulled high by the internal pull-ups and can be used as inputs. P3.4 and P3.5 are valid I/O pins only when the T80C5112 is using the internal RC oscillator, OSCB. P3.6 is an input only pin Port 3 also serves the special features of the 80C51 family, as listed below.
			I/O	**RXD (P3.0):** Serial input port
			I/O	**TXD (P3.1):** Serial output port
			I/O	**$\overline{INT0}$ (P3.2):** External interrupt 0
			I/O	**T0 (P3.3):** Timer 0 external input
			I/O	**XTAL1 (P3.4):** Input to the inverting oscillator amplifier and input to the internal clock generator circuits, selected by hardware set up[a]
			I/O	**XTAL2 (P3.5):** Output from the inverting oscillator amplifier, selected by hardware set up
P4.0-P4.7	X	X	I/O	**Port 4**: Port 4 is an 8-bit bidirectional I/O port. Each bit can be set as pure CMOS input or as push-pull output. Port 4 is also the input port of the Analog to digital converter and used for oscillator and reset.
			I/O	**AIN0 (P4.0):** A/D converter input 0
			I/O	**AIN1 (P4.1):** A/D converter input 1 **T1:** Timer 1 external input
			I/O	**AIN2 (P4.2):** A/D converter input 2 **$\overline{SS}$:** Slave select input of the SPI controller

			I/O	**AIN3 (P4.3):** A/D converter input 3 **$\overline{INT1}$:** External interrupt 1
			I/O	**AIN4 (P4.4):** A/D converter input 4 **MISO:** Master IN, Slave OUT of the SPI controller
			I/O	**AIN5 (P4.5):** A/D converter input 5 **MOSI:** Master OUT, Slave IN of the SPI controller
			I/O	**AIN6 (P4.6):** A/D converter input 6 **SPSCK:** Clock I/O of the SPI controlle
			I/O	**AIN7 (P4.7):** A/D converter input 7
P0.0-P0.7	X	X	I/O	**Port 0**: Port 0 is an open-drain, bidirectional I/O port. Port 0 pins that have 1s written to them float and can be used as high impedance inputs. Port 0 is also the multiplexed low-order address and data bus during access to external program and data memory. In this application, it uses strong internal pull-up when emitting 1s.
P2.0-P2.7	X	X	I/O	**Port 2**: Port 2 is an 8-bit bidirectional I/O port with internal pull-ups. Port 2 pins that have 1s written to them are pulled high by the internal pull-ups and can be used as inputs. As inputs, Port 2 pins that are externally pulled low will source current because of the internal pull-ups. Port 2 emits the high-order address byte during fetches from external program memory and during accesses to external data memory that use 16-bit addresses (MOVX @DPTR).In this application, it uses strong internal pull-ups emitting 1s. During accesses to external data memory that use 8-bit addresses (MOVX @Ri), port 2 emits the contents of the P2 SFR.
RST	X	X	I	**RST:** A high on this pin for two machine cycles while the oscillator is running, resets the device. An internal diffused resistor to V_{SS} permits a power-on reset using only an external capacitor to $V_{CC.}$ If the hardware watchdog reaches its time-out, the reset pin becomes an output during the time the internal reset is activated.
ALE	X	X	O	**Address Latch Enable:** Output pulse for latching the low byte of the address during an access to external memory. In normal operation, ALE is emitted at a constant rate of 1/6 (1/3 in X2 mode) the oscillator frequency, and can be used for external timing or clocking. Note that one ALE pulse is skipped during each access to external data memory. ALE can be disabled by setting SFR's AUXR.0 bit. With this bit set, ALE will be inactive during internal fetches.
$\overline{PSEN}$	X	X	O	**Program Store ENable:** The read strobe to external program memory. When executing code from the external program memory, $\overline{PSEN}$ is activated twice each machine cycle, except that two $\overline{PSEN}$ activations are skipped during each access to external data memory. $\overline{PSEN}$ is not activated during fetches from internal program memory.
$\overline{EA}$	X	X	I	**External Access Enable:** $\overline{EA}$ must be externally held low to enable the device to fetch code from external program memory locations 0000H and 1FFFH . If EA is held high, the device executes from internal program memory unless the program counter contains an address greater than 1FFFH. $\overline{EA}$ must be held low for ROMless devices. If security level 1 is programmed, $\overline{EA}$ will be internally latched on Reset.
XTAL1		X	I	**XTAL1 :** Input to the inverting oscillator amplifier and input to the internal clock generator circuits, selected by hardware set up[b]
XTAL2		X	O	**XTAL2 :** Output from the inverting oscillator amplifier, selected by hardware set up

a. Hardware set up :
+Configuration bits programmed with the code for ROM version
+Configuration bits for EPROM version
b. Hardware set up :
+Configuration bits programmed with the code for ROM version
+Configuration bits for EPROM version

6. Clock system

6.1. Overview

The T80C5112 oscillator system provides a reliable clocking system with full mastering of speed versus CPU power trade off. Several clocks sources are possible:

- External clock input
- High speed crystal or ceramic oscillator
- Low speed crystal oscillator
- Integrated high speed RC oscillator
- The low speed RC oscillator of the watchdog is a backup clocking source when no clock are selected in active or idle modes.

The selected clock source can be divided by 2-512 before clocking the CPU and the peripherals. When X2 function is set, the CPU need 6 clock periods per cycle.

Active oscillator at reset is defined by bits in a configuration byte programmed on an OTP programmer or by metal mask.

Clocking is controlled by several SFR registers : OSCON, CKCON0, CKCON1, CKRL.

6.2. Blocks description

The T80C5112 includes the following oscillators:

- Crystal oscillator, with two possible gains optimized for 32 kHz or 33 MHz.
- Integrated high speed RC oscillator, with typical frequency of 12 MHz
- Integrated low speed, low power RC oscillator, with typical frequency of 200 kHz; this oscillator is used to clock the hardware watchdog and as back up oscillator when the CPU receives no clock signal in active or idle modes.

6.2.1. Crystal oscillator : OSCA

The crystal oscillator uses two external pins, XTAL1 for input and XTAL2 for output.

XT_SP in configuration byte allows to select between two possible gains optimized for 32 kHz or 33 MHz. Both crystal and ceramic resonnators can be used.

OSCAEN in OSCCON register is an enable signal for the crystal oscillator or the external oscillator input.

When the crystal oscillator is not selected, XTAL1 can be used as a standard C51 I/O port, and X2 can be used as a standard C51 I/O port.

6.2.2. Integrated high speed RC oscillator : OSCB

The high speed RC oscillator do not need any external component; its typical frequency is 12 MHz. Note that the on chip oscillator has a +-25% frequency tolerance and for that reason may not be suitable for use in some applications.

OSCBEN in OSCCON register is an enable signal for the high speed RC oscillator.

6.2.3. Integrated low speed, low power RC oscillator : OSCC

The low speed, low power RC oscillator is used to clock the hardware watchdog and do not need any external component; its typical frequency is 200 kHz.

This oscillator is also used as back up oscillator when the CPU receive no clock signal in active or idle modes.

RCLF_OFF is the configuration bit used to switch on or off the low speed RC oscillator.

Note that the on chip oscillator has a +-25% frequency tolerance and for that reason may not be suitable for use in some applications.

6.2.4. Clock selector

CKS bit in CKS register is used to select from crystal to RC oscillator.

OSCBEN bit in OSCCON register is used to enable the RC oscillator.

OSCAEN bit in OSCCON register is used to enable the crystal oscillator or the external oscillator input.

If both oscillators are disabled, the low speed oscillator, OSCC is used as a backup source for the CPU and the peripherals.

This feature provides a stand alone low frequency mode which can be activated when needed.

6.2.5. Clock prescaler

Before supplying the CPU and the peripherals, the main clock is divided by a factor to 2 to 512, as defined by the CKRL register. The CPU needs from 12 to 256*12 clock periods per instruction. This allows:

- To accept any cyclic ratio to be accepted on XTAL1 input.
- To reduce the CPU power consumption.

The X2 bit allows to bypass the clock prescaler ; in this case, the CPU need only 6 clock periods per machine cycle. In X2 mode, as this divider is bypassed, the signals on XTAL1 must have a cyclic ratio between 40 to 60%

6.3. Functional Block diagram

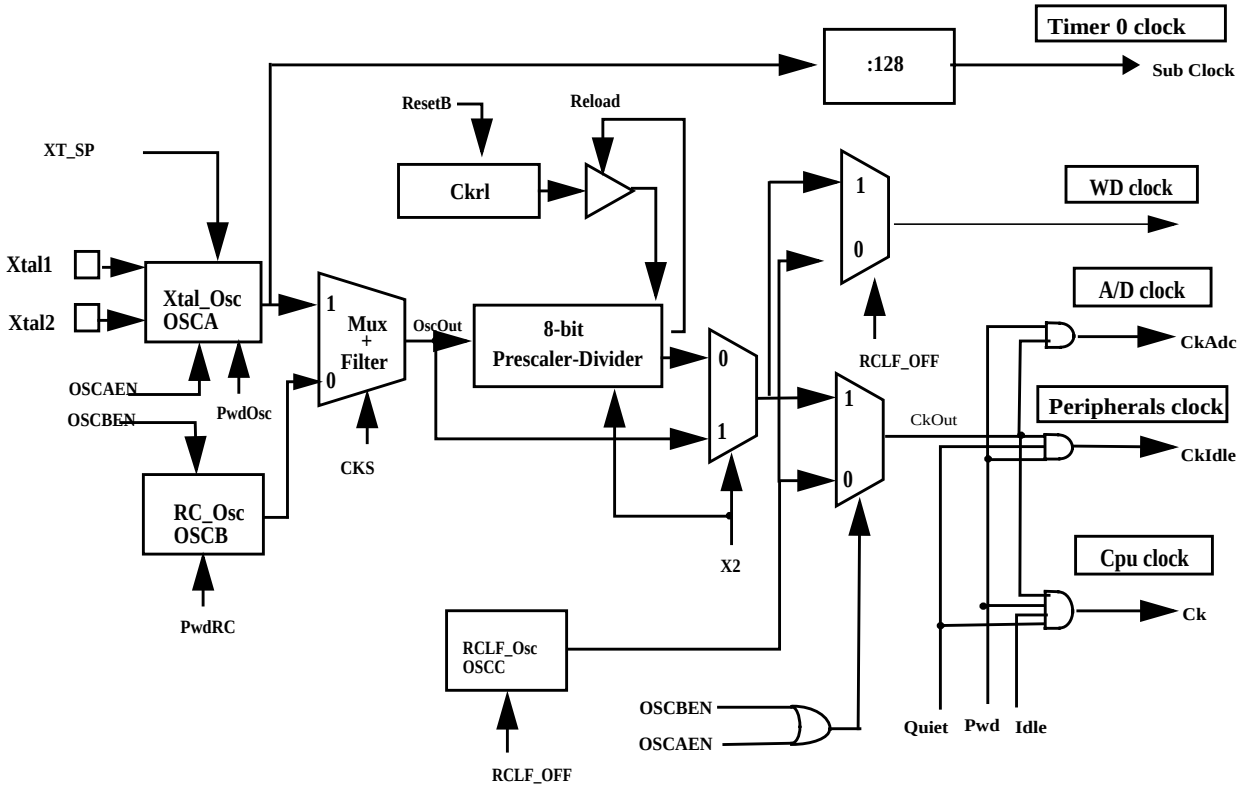


Figure 1. Functional block diagram

6.4. Operating modes

6.4.1. Reset :

- An hardware RESET select Xtal_Osc or RC_Osc depending on the RST_OSC configuration bit

6.4.2. Functional modes :

6.4.2.1. NORMAL MODES :

- CPU and Peripherals clock depend on the software selection using CKCON0, CKCON1, CKSEL and CKRL registers
  - CKS bit selects either Xtal_Osc or RC_Osc
  - CKRL register determines the frequency of the selected clock, unless X2 bit is set.
    In this case the prescaler/divider is not used, so CPU core needs only 6-clock period per machine cycle. According to the value of the peripheral X2 individual bit, each peripherals need 6 or 12 clock period per instructions.
  - It is always possible to switch dynamicaly by software from Xtal_Osc to RC_Osc, and vice versa by changing CKS bit, a synchronization cell allowing to avoid any spike during transition.

6.4.2.2. IDLE MODES :

- IDLE modes are achieved by using any instruction that writes into PCON.0 sfr
- IDLE modes A and B depend on previous software sequence, prior to writing into PCON.0 register :
  - IDLE MODE A : Xtal_Osc is running (OSCAEN = 1) and selected (CKS = 1)
  - IDLE MODE B : RC_Osc is running (OSCBEN = 1) and selected (CKS = 0)
  - The unused oscillator Xtal_Osc or RC_Osc can be stopped by software by clearing OSCAEN or OSCBEN respectively.
  - Exit from IDLE mode is acheived by Reset, or by activation of an enabled interrupt.
  - In both case, PCON.0 is cleared by hardware.
  - Exit from IDLE modes will leave the ocillators control bits OSCAEN, OSCBEN and CKS unchanged.

6.4.2.3. POWER DOWN MODES :

- POWER DOWN modes are achieved by using any instruction that writes into PCON.1 sfr
- Exit from POWER DOWN mode is acheived either by an harware Reset, by an external interruption.
  - By RST signal : The CPU will restart in the mode defined by RST_OSC.
  - By INT0 or INT1 interruptions, if enabled. The ocillators control bits OSCAEN, OSCBEN and CKS will not be changed, so the selected oscillator before entering into Power-down will be activated.

PD	IDLE	CKS	OSCBEN	OSCAEN	RCLF _OFF	Selected Mode	Comment
0	0	1	X	1	X	NORMAL MODE A	OSCA: XTAL clock
X	X	1	X	0	1	INVALID	no active clock
0	0	1	0	0	0	RESCUE MODE	OSCC: Low speed RC clock active
0	0	0	1	X	X	NORMAL MODE B,	OSCB: high speed RC clock
X	X	0	0	X	1	INVALID	
0	0	0	0	0	0	RESCUE MODE	OSCC: Low speed RC clock active
0	1	1	X	1	X	IDLE MODE A	The CPU is off, OSCA supplies the peripherics
0	1	0	1	X	X	IDLE MODE B	The CPU is off, OSCB supplies the peripherics
1	X	X	X	1	0	POWER DOWN MODE with WD	The CPU and peripherics are off, but OSCC is still running for WD
1	X	X	X	X	1	TOTAL POWER DOWN	The CPU is off, OSCA and OSCB are stopped OSCC is stopped

6.4.2.4. Prescaler Divider :

- An hardware RESET selects the prescaler divider :
  - CKRL = FFh: internal clock = OscOut / 2 (Standard C51 feature)
  - X2 = 0,
  - SEL_OSC signal selects Xtal_Osc or RC_Osc, depending on the value of the RST_OSC configuration bit.
- After Reset, any value between FFh down to 00h can be written by software into CKRL sfr in order to divide frequency of the selected oscillator:
  - CKRL = 00h : minimum frequency = OscOut / 512
  - CKRL = FFh : maximum frequency = OscOut / 2

- A software instruction which set X2 bit desactivates the precaler/divider, so the internal clock is either Xtal_Osc or RC_Osc depending on SEL_OSC bit.

6.5. Timer 0 : Clock Inputs

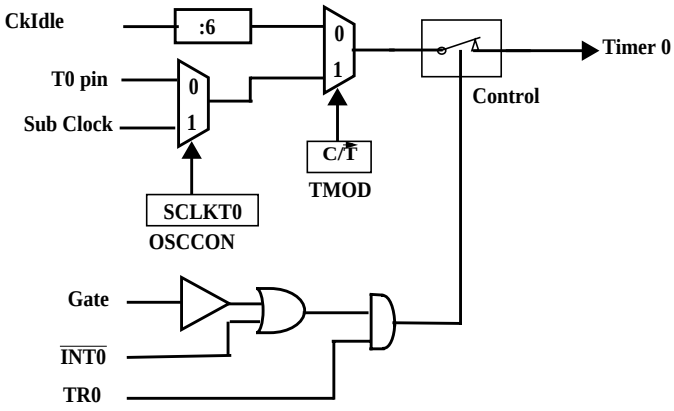


Figure 2. Timer 0 : Clock Inputs

The SCLKT0 bit in OSCCON register allows to select Timer 0 Subsidiary clock. This allow to perform a Real Time Clock function.

SCLKT0 = 0 : Timer 0 uses the standard T0 pin as clock input (Standard mode)

SCLKT0 = 1 : Timer 0 uses the special Sub Clock as clock input.

When the subclock input is selected for Timer 0 and the crystal oscillator is selected for CPU and peripherals, the CKRL prescaler must be set to FF (division factor 2) in order to assure a proper count on Timer 0.

With a 32 kHz crystal, the timer interrupt can be set from 1/256 to 256 seconds to perform a Real Time Clock (RTC) function. The power consumption will be very low as the CPU is in idle mode at 32 KHz most of the time. When more CPU power is needed, the internal RC oscillator is activated and used by the CPU and the others peripherals.

6.6. Registers

6.6.1. Configuration byte

The configuration byte is a special register. Its content is defined by the diffusion mask in the ROM version or is reread or written by the OTP programmer in the OTP version. This register can also be accessed as a read only register.

CONF - Configuration byte (EFh)

7	6	5	4	3	2	1	0
LB1	LB2	LB3	RST_OSC	XT_SP	RST_EXT	OSCC_OFF	

Bit Number	Bit Mnemonic	Description
7:5	-	**Program memory lock bits** See chapter program memory for the definition of these bits..

Bit Number	Bit Mnemonic	Description
4	RST_OSC	**Selected oscillator at reset** This bit is used to define the value of some bits controlling the oscillator activity at reset: 1: The crystal oscillator is sectected and active 0: The RC oscillator is selected; it is also active if the WDRC is inactive.
3	XT_SP	**Crystal oscillator speed** This bit is used to define the performance of the crystal oscillator. 1: High speed, up to 33 MHz 0: Low speed, low power, optimised for 32 kHz.
2	EXT_RST	**External Reset** This bit defines the behavior of the P3.6/$\overline{RST}$ pin 1: P3.6/$\overline{RST}$ is the reset pin 0: P3.6/$\overline{RST}$ is an input pin
1	OSCC_OFF	Control for watchdog RC oscillator This bit is used to switch the watchdog RC oscillator and the watchdog source 1: WDRC oscillator is off; the watchdog is clocked by the main oscillator. 0: WDRC oscillator is on and clock the watchdog
0	-	**Reserved** The value read from this bit is indeterminate. Do not reset this bit.

Initial value after erasing : 1111 111X

6.6.2. Clock control register

The clock control register is used to define the clock system behavior

OSCCON - Clock Control Register (86h)

7	6	5	4	3	2	1	0
-	-	-	-	-	**SCLKT0**	**OSCBEN**	**OSCAEN**

Bit Number	Bit Mnemonic	Description
7	-	**Reserved** The value read from this bit is indeterminate. Do not set this bit.
6	-	**Reserved** The value read from this bit is indeterminate. Do not set this bit.
5	-	**Reserved** The value read from this bit is indeterminate. Do not set this bit.
4	-	**Reserved** The value read from this bit is indeterminate. Do not set this bit.
3	-	**Reserved** The value read from this bit is indeterminate. Do not set this bit.
2	SCLKT0	**Sub Clock Timer0** Cleared by software to select T0 pin Set by software to select T0 Sub Clock
1	OSCBEN	**Enable RC oscillator** This bit is used to enable the high speed RC oscillator 0: The oscillator is disabled 1: The oscillator is enabled.
0	OSCAEN	**Enable crystal oscillator** This bit is used to enable the crystal oscillator 0: The oscillator is disabled 1: The oscillator is enabled.

Reset Value = 0XXX X0 "RST_OSC" "RST_OSC" b
Not bit addressable

6.6.3. Clock selection register

The clock selectionl register is used to define the clock system behavior

CKSEL - Clock Selection Register (85h)

7	6	5	4	3	2	1	0
	-	-	-	-	-	-	CKS

Bit Number	Bit Mnemonic	Description
7	-	**Reserved** The value read from this bit is indeterminate. Do not set this bit.
6	-	**Reserved** The value read from this bit is indeterminate. Do not set this bit.
5	-	**Reserved** The value read from this bit is indeterminate. Do not set this bit.
4	-	**Reserved** The value read from this bit is indeterminate. Do not set this bit.
3	-	**Reserved** The value read from this bit is indeterminate. Do not set this bit.
2	-	**Reserved** The value read from this bit is indeterminate. Do not set this bit.
1	-	**Reserved** The value read from this bit is indeterminate. Do not set this bit.
0	CKS	**Active oscillator selection** This bit is used to select the active oscillator 1: The crystal oscillator is selected 0: The high speed RC oscillator is selected.

Reset Value = XXXX XXX "RST_OSC" b
Not bit addressable

6.6.4. Clock prescaler register

This register is used to reload the clock prescaler of the CPU and peripheral clock.

CKRL - Clock prescaler Register (97h)

7	6	5	4	3	2	1	0
M							

Bit Number	Bit Mnemonic	Description
7:0	CKRL	0000 0000b: Division factor equal 512 1111 1111b: Division factor equal 2 M: Division factor equal 2*(256-M)

Reset Value = 1111 1111b
Not bit addressable

6.6.5. Clock control register

This register is used to control the X2 mode of the CPU and peripheral clock.

Table 2. CKCON0 Register

CKCON0 - Clock Control Register (8Fh)

7	6	5	4	3	2	1	0
-	WdX2	PcaX2	SiX2	-	T1X2	T0X2	X2

Bit Number	Bit Mnemonic	Description
7	-	Reserved
6	WdX2	**Watchdog clock** (This control bit is validated when the CPU clock X2 is set; when X2 is low, this bit has no effect) Clear to select 6 clock periods per peripheral clock cycle. Set to select 12 clock periods per peripheral clock cycle.
5	PcaX2	**Programmable Counter Array clock** (This control bit is validated when the CPU clock X2 is set; when X2 is low, this bit has no effect) Clear to select 6 clock periods per peripheral clock cycle. Set to select 12 clock periods per peripheral clock cycle.
4	SiX2	**Enhanced UART clock (Mode 0 and 2)** (This control bit is validated when the CPU clock X2 is set; when X2 is low, this bit has no effect) Clear to select 6 clock periods per peripheral clock cycle. Set to select 12 clock periods per peripheral clock cycle.
3	-	Reserved
2	T1X2	**Timer1 clock** (This control bit is validated when the CPU clock X2 is set; when X2 is low, this bit has no effect) Clear to select 6 clock periods per peripheral clock cycle. Set to select 12 clock periods per peripheral clock cycle
1	T0X2	**Timer0 clock** (This control bit is validated when the CPU clock X2 is set; when X2 is low, this bit has no effect) Clear to select 6 clock periods per peripheral clock cycle. Set to select 12 clock periods per peripheral clock cycle
0	X2	CPU clock Clear to select 12 clock periods per machine cycle (STD mode) for CPU and all the peripherals. Set to select 6clock periods per machine cycle (X2 mode) and to enable the individual peripherals "X2" bits.

Reset Value = X000 0000b
Not bit addressable

Table 3. CKCON1 Register

CKCON1 - Clock Control Register

7	6	5	4	3	2	1	0
-	-	-	-	-	-	BRGX2	SPIX2

Bit Number	Bit Mnemonic	Description
7	-	Reserved
6	-	Reserved
5	-	Reserved
4	-	Reserved
3	-	Reserved
2	-	Reserved
1	-	Reserved
0	SPIX2	**SPI clock** (This control bit is validated when the CPU clock X2 is set; when X2 is low, this bit has no effect) Clear to select 6 clock periods per peripheral clock cycle. Set to select 12 clock periods per peripheral clock cycle

Reset Value = XXXX XX00b
Not bit addressable

7. Reset and Power Management

7.1. Introduction

The power monitoring and management can be used to supervise the Power Supply (VDD) and to start up properly when T80C5112 is powered up.

It consists of the features listed below and explained hereafter:

- Power on Reset
- Power-Fail reset
- Power-Off flag
- Idle mode
- Power-Down mode
- Reduced EMI mode

All these features are controlled by several registers, the Power Control register (PCON) and the Auxiliary register (AUXR) detailed at the end of this chapter.

AUX register not available on all versions.

7.2. Functional description

Figure 3 shows the block diagram of the possible sources of microcontroller reset.

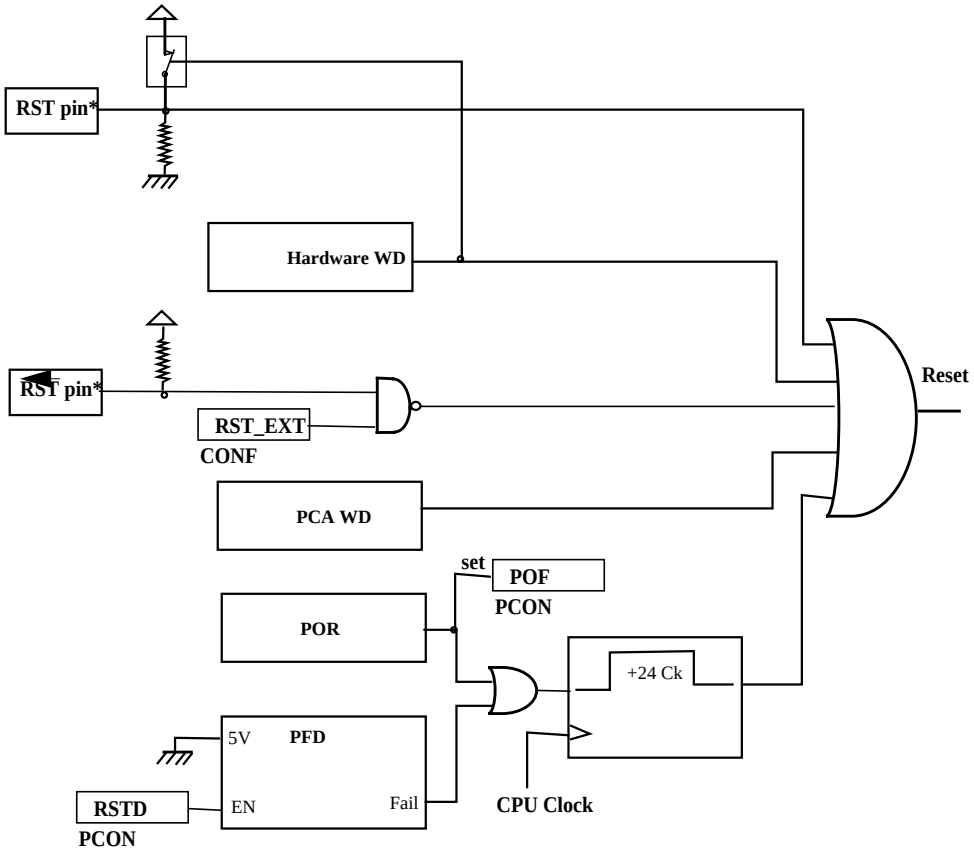


Figure 3. Reset sources

Notes: RST pin available only on 48 and 52 pins versions.

Notes: $\overline{RST}$ pin available only on LPC versions.

7.3. Power-On Reset

The T80C5112 has a power on reset (POR) module which reset the chip during the initial power raise. The internal power on reset pulse duration is 24 clock periods of the CPU clock. The chip can also be reseted by the P3.6/ $\overline{RST}$/Vpp pin provided the EXT_RST bit of the configuration byte is high.

This module set the POF bit vhen Vcc is below the memory data retention voltage.

The behavior or POR and PFD is shown on Figure 4.

7.4. Power-Fail Detector

The Power-Fail Detector (PFD) is controlled by RSTD bit in PCON register. The PFD is disabled upon reset.

When enabled, the power supply is continuously monitored and an internal reset is generated(1) if VDD goes below V_{RST} for at least 60 ns.

If the power supply rises again over V_{RST+}(2), the internal reset completes after 24 CPU clock periods.

If RSTD is reset, the power supply monitoring is disabled.

In Power-Down mode, the PFD is automatically disabled; this avoids extra consumption and allows VDD reduction to V_{RET}.

Note:
1. The internal reset is not propagated on the RST pin.
2 See AC/DC section for the specifications of Vrst.

Caution:
When VDD is reduced to V_{RET} in Power-Down mode the VDD voltage is not accuratly monitored. In this case, RAM content may be damage if VDD goes below V_{RET} and circuit behavior is unpredictable unless an external reset is applied. The POF bit can be used to verify if memory contains valid data.

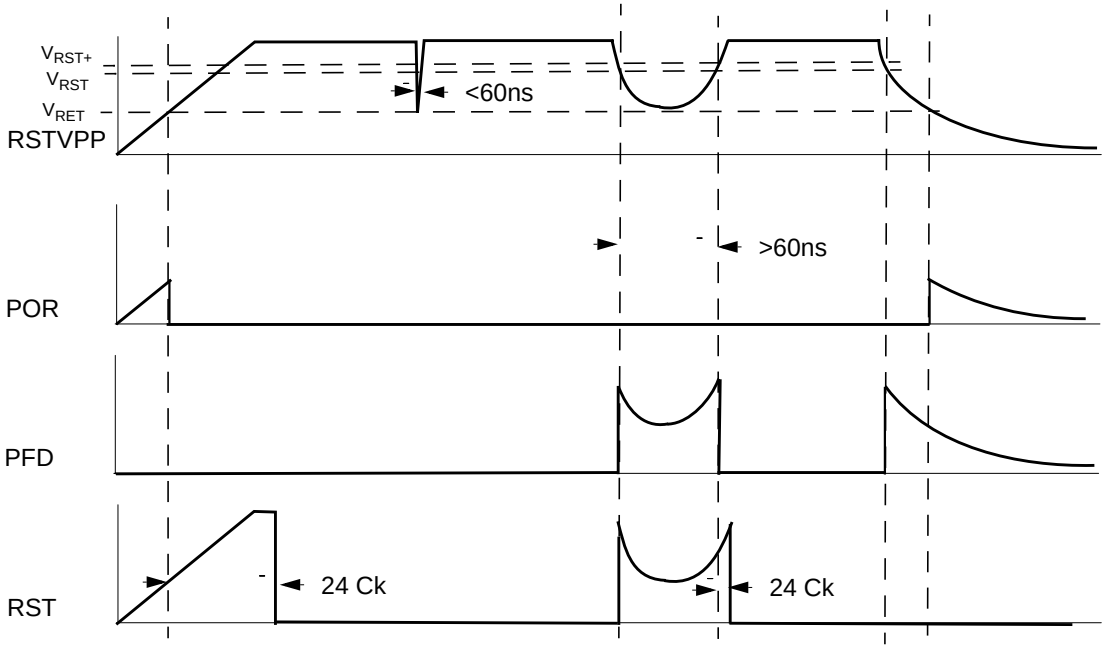


Figure 4. Power Fail Reset timing diagram

7.5. Power-Off Flag

When the power is turned off or fails, the data retention is not guaranteed. A Power-Off Flag (POF, see 7.6.1.) allows to detect this condition. POF is set by hardware during a reset which follows a power-up or a power-fail. This is a cold reset. A warm reset is an external or a watchdog reset without power failure, hence which preserves the internal memory content and POF. To use POF, test and clear this bit just after reset. Then it will be set only after a cold reset.

Notes: When power supply monitoring is disabled (RSTD= 1 or in Power-Down mode), POF information is not delivered with the same accuracy. It is recommended to clear and not to take in account the POF value after exit from a power down mode with VDD reduction.

Notes: The POF flag is set only if Vcc is lower below the memory data retention voltage. Hence, the PFD may detect a power fail while the POF bit is still valid.

7.6. Registers

7.6.1. PCON: Power configuration register

Table 4. PCON Register

PCON (S:87h)
Power configuration Register

7	6	5	4	3	2	1	0
SMOD1	**SMOD0**	**RSTD**	**POF**	**GF1**	**GF0**	**PD**	**IDL**

Bit Number	Bit Mnemonic	Description
7	SMOD1	**Double Baud Rate bit** Set to double the Baud Rate when Timer 1 is used and mode 1, 2 or 3 is selected in SCON register.
6	SMOD0	**SCON Select bit** When cleared, read/write accesses to SCON.7 are to SM0 bit and read/write accesses to SCON.6 are to SM1 bit. When set, read/write accesses to SCON.7 are to FE bit and read/write accesses to SCON.6 are to OVR bit. SCON is Serial Port Control register.
5	RSTD	**Reset Detector Disable bit** Clear to disable the Power-Fail detector. Set to enable the Power-Fail detector.
4	POF	**Power-Off flag** Set by hardware when VDD rises above V_{RET+} to indicate that the Power Supply has been set off. Must be cleared by software.
3	GF1	**General Purpose flag 1** One use is to indicate wether an interrupt occurred during normal operation or during Idle mode.
2	GF0	**General Purpose flag 0** One use is to indicate wether an interrupt occurred during normal operation or during Idle mode.
1	PD	**Power-Down Mode bit** Cleared by hardware when an interrupt or reset occurs. Set to activate the Power-Down mode. If IDL and PD are both set, PD takes precedence.
0	IDL	**Idle Mode bit** Cleared by hardware when an interrupt or reset occurs. Set to activate the Idle mode. If IDL and PD are both set, PD takes precedence.

Reset Value= 0000 0000b

7.7. Port pins

The value of port pins in the different operating modes is shown on the figure below.

Table 5. Pin Conditions in Special Operating Modes

Mode	Program Memory	Port 1 pins	Port 3 pins	Port 4 pins
Reset	Don't care	Weak High	Weak High	Weak High
Idle	Internal	Data	Data	Data
Power-Down	Internal	Data	Data	Data

7.8. Reduced EMI mode

The ALE signal is used to demultiplex address and data buses on port 0 when used with external program or data memory. Nevertheless, during internal code execution, ALE signal is still generated. In order to reduce EMI, ALE signal can be disabled by setting AO bit.

The AO bit is located in AUXR register at bit location 0. As soon as AO is set, ALE is no longer output but remains active during MOVX and MOVC instructions and external fetches. During ALE disabling, ALE pin is weakly pulled high.

Table 6. AUXR Register

AUXR - Auxiliary Register (8Eh)

7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	**AO**

Bit Number	Bit Mnemonic	Description
7	-	**Reserved** The value read from this bit is indeterminate. Do not set this bit.
6	-	**Reserved** The value read from this bit is indeterminate. Do not set this bit.
5	-	**Reserved** The value read from this bit is indeterminate. Do not set this bit.
4	-	**Reserved** The value read from this bit is indeterminate. Do not set this bit.
3	-	**Reserved** The value read from this bit is indeterminate. Do not set this bit.
2	-	**Reserved** The value read from this bit is indeterminate. Do not set this bit.
1	-	**Reserved** The value read from this bit is indeterminate. Do not set this bit.
0	AO	**ALE Output bit** Clear to restore ALE operation during internal fetches. Set to disable ALE operation during internal fetches.

Reset Value = XXXX XXX0b
Not bit addressable

8. Hardware Watchdog Timer

The WDT is intended as a recovery method in situations where the CPU may be subjected to software upset. The WDT consists of a 14-bit counter and the WatchDog Timer ReSeT (WDTRST) SFR. The WDT is by default disabled from exiting reset. To enable the WDT, user must write 01EH and 0E1H in sequence to the WDTRST, SFR location 0A6H. When WDT is enabled, it will increment every machine cycle (6 internal clock periods) and there is no way to disable the WDT except through reset (either hardware reset or WDT overflow reset). The T0 bit of the WDTPRG register is used to select the overflow after 10 or 14 bits. When WDT overflows, it will generate an internal reset. It will also drive an output RESET HIGH pulse at the emulator RST-pin.

If the crystal oscillator is selected with whe low speed option (32kHz), the low speed RC oscillator must not be used. In this case the WDT will also use the low speed crystal oscillator.

8.1. Using the WDT

To enable the WDT, user must write 01EH and 0E1H in sequence to the WDTRST, SFR location 0A6H. When WDT is enabled, the user needs to service it by writing to 01EH and 0E1H to WDTRST to avoid WDT overflow. The 14-bit counter overflows when it reaches 16383 (3FFFH) or 1024 (1FFFH) and this will reset the device. When WDT is enabled, it will increment every machine cycle while the oscillator is running. This means the user must reset the WDT at least every 16383 machine cycle. To reset the WDT the user must write 01EH and 0E1H to WDTRST. WDTRST is a write only register. The WDT counter cannot be read or written. When WDT overflows, it will generate an output RESET pulse at the RST-pin. The RESET pulse duration is 96 x T_{OSC} , where T_{OSC} = $1/F_{OSC}$. To make the best use of the WDT, it should be serviced in those sections of code that will periodically be executed within the time required to prevent a WDT reset.

To have a more powerful WDT, a 2^7 counter has been added to extend the Time-out capability, ranking from 16ms to 2s @ F_{OSC} = 12MHz and T0=0. To manage this feature, refer to WDTPRG register description, Table 8. (SFR0A7h).

Table 7. WDTRST Register

WDTRST Address (0A6h)

	7	6	5	4	3	2	1
Reset value	X	X	X	X	X	X	X

Write only, this SFR is used to reset/enable the WDT by writing 01EH then 0E1H in sequence.

Table 8. WDTPRG Register

WDTPRG Address (0A7h)

7	6	5	4	3	2	1	0
T4	T3	T2	T1	T0	S2	S1	S0

Bit Number	Bit Mnemonic	Description
7	T4	**Reserved** Do not try to set this bit.
6	T3	
5	T2	
4	T1	
3	T0	WDT overflow select bit 0 : Overflow after 14 bits 1 : Overflow after 10 bits
2	S2	WDT Time-out select bit 2
1	S1	WDT Time-out select bit 1
0	S0	WDT Time-out select bit 0
		S2S1S0 — Selected Time-out with T0=0 000 — (2^{14} - 1) machine cycles, 16.3 ms @ 12 MHz 001 — (2^{15} - 1) machine cycles, 32.7 ms @ 12 MHz 010 — (2^{16} - 1) machine cycles, 65.5 ms @ 12 MHz 011 — (2^{17} - 1) machine cycles, 131 ms @ 12 MHz 100 — (2^{18} - 1) machine cycles, 262 ms @ 12 MHz 101 — (2^{19} - 1) machine cycles, 542 ms @ 12 MHz 110 — (2^{20} - 1) machine cycles, 1.05 s @ 12 MHz 111 — (2^{21} - 1) machine cycles, 2.09 s @ 12 MHz S2S1 S0 — Selected Time-out with T0=1 000 — (2^{10} - 1) machine cycles, 60 ms @ 200 kHz 001 — (2^{11} - 1) machine cycles, 120ms @ 200 kHz 010 — (2^{12} - 1) machine cycles, 240ms @ 200 kHz 011 — (2^{13} - 1) machine cycles, 480ms @ 200 kHz 100 — (2^{14} - 1) machine cycles, 860ms @ 200 kHz 101 — (2^{15} - 1) machine cycles, 1.7s @ 200 kHz 110 — (2^{16} - 1) machine cycles, 3.4s @ 200 kHz 111 — (2^{17} - 1) machine cycles, 6.8s @ 200 kHz

Reset value XXX0 0000

Write only register

8.1.1. WDT during Power Down and Idle

8.1.1.1. Power down and OSCC inactive

In Power Down mode the oscillator stops, which means the WDT also stops. While in Power Down mode the user does not need to service the WDT. There are 2 methods of exiting Power Down mode: by a hardware reset or via a level activated external interrupt which is enabled prior to entering Power Down mode. When Power Down is exited with hardware reset, servicing the WDT should occur as it normally should whenever the T80C5112 is reset. Exiting Power Down with an interrupt is significantly different. The interrupt is held low long enough for the oscillator to stabilize. When the interrupt is brought high, the interrupt is serviced. To prevent the WDT from resetting the device while the interrupt pin is held low, the WDT is not started until the interrupt is pulled high. It is suggested that the WDT be reseted during the interrupt service routine.

To ensure that the WDT does not overflow within a few states of exiting of powerdown, it is best to reset the WDT just before entering powerdown.

8.1.1.2. Power down and OSCC active

In Power Down mode the low speed RC oscillator never stops. If the WDT is active before entering power down, the T80C5112 will be reseted once and will start executing the program code. The software may then decide to leave the WDT inactive.

If the high speed RC oscillator is selected at reset, this mode may be used to periodically awake the T80C5112 and check for an external event while keeping the average consumption at a very low level.

There are 2 methods of exiting Power Down mode: by a hardware or watchdog reset or via a level activated external interrupt which is enabled prior to entering Power Down mode. When Power Down is exited with hardware or watch dog reset, servicing the WDT should occur as it normally should whenever the T80C5112 is reset. Exiting Power Down with an interrupt is significantly different. As the WDT and interrupt are asynchronous events, the WDT may overflow within a few states of exiting of powerdown. To limit the probability of such an event, it is suggested that the WDT be reseted during the interrupt service routine.

8.1.1.3. Idle mode

In the Idle mode, the oscillator continues to run. To prevent the WDT from resetting the T80C5112 while in Idle mode, the user should always set up a timer that will periodically exit Idle, service the WDT, and re-enter Idle mode.

9. Ports

The T80C5112 has 5 I/O ports, from port 0 to port 4.. The number of possible I/O on each package option is shown on Table 9.

At least 39 pins of the T80C5112 may be used as I/Os when a two-pin external oscillator.

Table 9. Number of available I/O versus pin number

	48	52
Supply pins	2	3
I/O	39	39
Inputs	1	1
Maximun I/O count	40	40

All port1, port3 and port4 I/O port pins on the T80C5112 may be software configured to one of four types on a bit-by-bit basis, as shown in Table 10. These are: quasi-bidirectional (standard 80C51 port outputs), push-pull, open drain, and input only. Two configuration registers for each port choose the output type for each port pin.

Table 10. Port Output Configuration settings using PxM1 and PxM2 registers

PxM1.y bit	PxM2.y bit	Port Output Mode
0	0	Quasi bidirectional
0	1	Push-Pull
1	0	Input Only (High Impedance)
1	1	Open Drain

9.1. Ports types

9.1.1. Quasi-Bidirectional Output Configuration

The default port output configuration for standard T80C5112 I/O ports is the quasi-bidirectional output that is common on the 80C51 and most of its derivatives. This output type can be used as both an input and output without the need to reconfigure the port. This is possible because when the port outputs a logic high, it is weakly driven, allowing an external device to pull the pin low. When the pin is pulled low, it is driven strongly and able to sink a fairly large current. These features are somewhat similar to an open drain output except that there are three pull-up transistors in the quasi-bidirectional output that serve different purposes. One of these pull-ups, called the "very weak" pull-up, is turned on whenever the port latch for the pin contains a logic 1. The very weak pull-up sources a very small current that will pull the pin high if it is left floating. A second pull-up, called the "weak" pull-up, is turned on when the port latch for the pin contains a logic 1 and the pin itself is also at a logic 1 level. This pull-up provides the primary source current for a quasi-bidirectional pin that is outputting a 1. If a pin that has a logic 1 on it is pulled low by an external device, the weak pull-up turns off, and only the very weak pull-up remains on. In order to pull the pin low under these conditions, the external device has to sink enough current to overpower the weak pull-up and take the voltage on the port pin below its input threshold.

The third pull-up is referred to as the "strong" pull-up. This pull-up is used to speed up low-to-high transitions on a quasi-bidirectional port pin when the port latch changes from a logic 0 to a logic 1. When this occurs, the strong pull-up turns on for a brief time, two CPU clocks, in order to pull the port pin high quickly. Then it turns off again.

The quasi-bidirectional port configuration is shown in Figure 5.

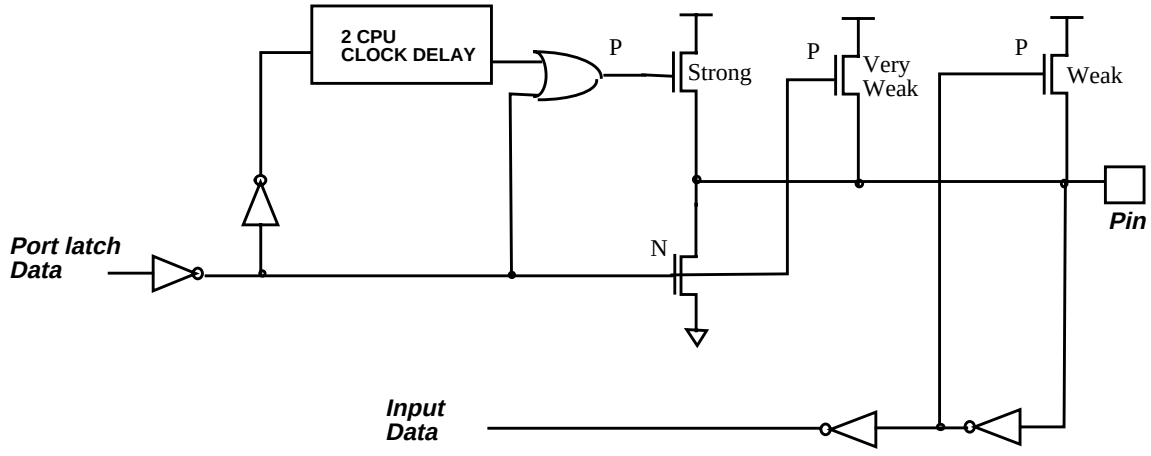


Figure 5. Quasi-Bidirectional Output

9.1.2. Open Drain Output Configuration

The open drain output configuration turns off all pull-ups and only drives the pull-down transistor of the port driver when the port latch contains a logic 0. To be used as a logic output, a port configured in this manner must have an external pull-up, typically a resistor tied to Vdd. The pull-down for this mode is the same as for the quasi-bidirectional mode. The open drain port configuration is shown in Figure 6.

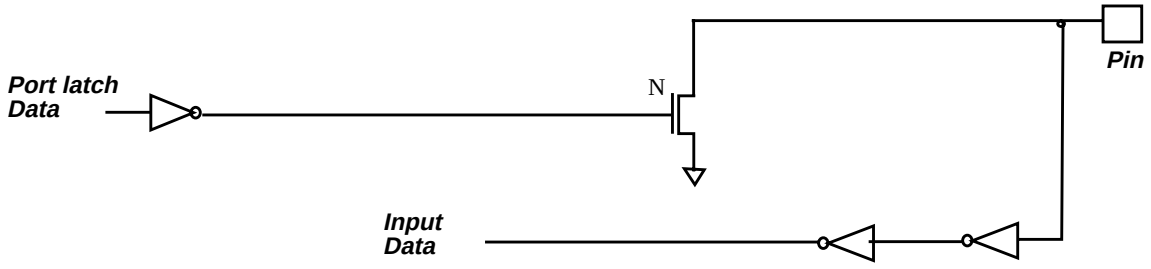


Figure 6. Open Drain Output

9.1.3. Push-Pull Output Configuration

The push-pull output configuration has the same pull-down structure as both the open drain and the quasi-bidirectional output modes, but provides a continuous strong pull-up when the port latch contains a logic 1. The push-pull mode may be used when more source current is needed from a port output. The push-pull port configuration is shown in Figure 7.

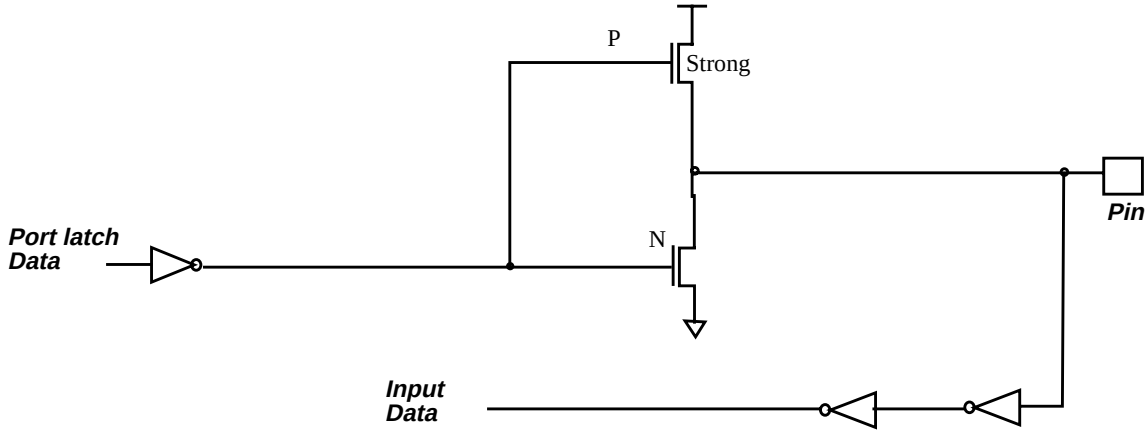


Figure 7. Push-Pull Output

9.1.4. Input only Configuration

The input only configuration is a pure input with neither pull-up nor pull-down.

The input only configuration is shown in Figure 7.

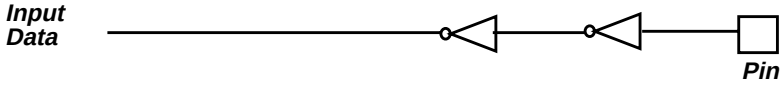


Figure 8. Input only

9.2. Ports description

9.2.1. Ports P1, P3 and P4

Every output on the T80C5112 may potentially be used as a 20 mA sink LED drive output. However, there is a maximum total output current for all ports which must not be exceeded. All ports pins of the T80C5112 have slew rate controlled outputs. This is to limit noise generated by quickly switching output signals. The slew rate is factory set to approximately 10 ns rise and fall times.

The inputs of each I/O port of the T80C5112 are TTL level Schmitt triggers with hysteresis.

9.2.2. Ports P0 and P2

High pin count version of the T80C5112 have standard address and data ports P0 and P2. These ports are standard C51 ports (Quasi-bidirectional I/O). The control lines are provided on the pins : ALE, PSEN, $\overline{EA}$, Reset; $\overline{RD}$ and $\overline{WR}$ signals are on the bits P1.1 and P1.0 .

9.3. Registers

Table 11. P1M1 Register

P1M1 Address (D4h)

7	6	5	4	3	2	1	0
P1M1.7	P1M1.6	P1M1.5	P1M1.4	P1M1.3	P1M1.2	P1M1.1	P1M1.0

Bit Number	Bit Mnemonic	Description
7 : 0	P1M1.x	**Port Output configuration bit** See Table 10. for configuration definition

Reset value 0000 00XX

Table 12. P1M2 Register

P1M2 Address (E2h)

7	6	5	4	3	2	1	0
P1M2.7	P1M2.6	P1M2.5	P1M2.4	P1M2.3	P1M2.2	P1M2.1	P1M2.0

Bit Number	Bit Mnemonic	Description
7 : 0	P1M2.x	**Port Output configuration bit** See Table 10. for configuration definition

Reset value 0000 00XX

Table 13. P3M1 Register

P3M1 Address (D5h)

7	6	5	4	3	2	1	0
P3M1.7	P3M1.6	P3M1.5	P3M1.4	P3M1.3	P3M1.2	P3M1.1	P3M1.0

Bit Number	Bit Mnemonic	Description
7 : 0	P3M1.x	**Port Output configuration bit** See Table 10. for configuration definition

Reset value 0000 0000

Table 14. P3M2 Register

P3M2 Address (E4h)

7	6	5	4	3	2	1	0
P3M2.7	P3M2.6	P3M2.5	P3M2.4	P3M2.3	P3M2.2	P3M2.1	P3M2.0

Bit Number	Bit Mnemonic	Description
7 : 0	P3M2.x	**Port Output configuration bit** See Table 10. for configuration definition

Reset value 0000 0000

Table 15. P4M1 Register

P4M1 Address (D6h)

7	6	5	4	3	2	1	0
P4M1.7	P4M1.6	P4M1.5	P4M1.4	P4M1.3	P4M1.2	P4M1.1	P4M1.0

Bit Number	Bit Mnemonic	Description
7 : 0	P4M1.x	**Port Output configuration bit** See Table 10. for configuration definition

Reset value 0000 0000

Table 16. P4M2 Register

P4M2 Address (E5h)

7	6	5	4	3	2	1	0
P4M2.7	**P4M2.6**	**P4M2.5**	**P4M2.4**	**P4M2.3**	**P4M2.2**	**P4M2.1**	**P4M2.0**

Bit Number	Bit Mnemonic	Description
7: 0	P4M2.x	**Port Output configuration bit** See Table 10. for configuration definition

Reset value 0000 0000

10. Dual Data Pointer Register Ddptr

The additional data pointer can be used to speed up code execution and reduce code size in a number of ways.

The dual DPTR structure is a way by which the chip will specify the address of an external data memory location. There are two 16-bit DPTR registers that address the external memory, and a single bit called DPS = AUXR1/bit0 (See Table 17.) that allows the program code to switch between them (Refer to Figure 9).

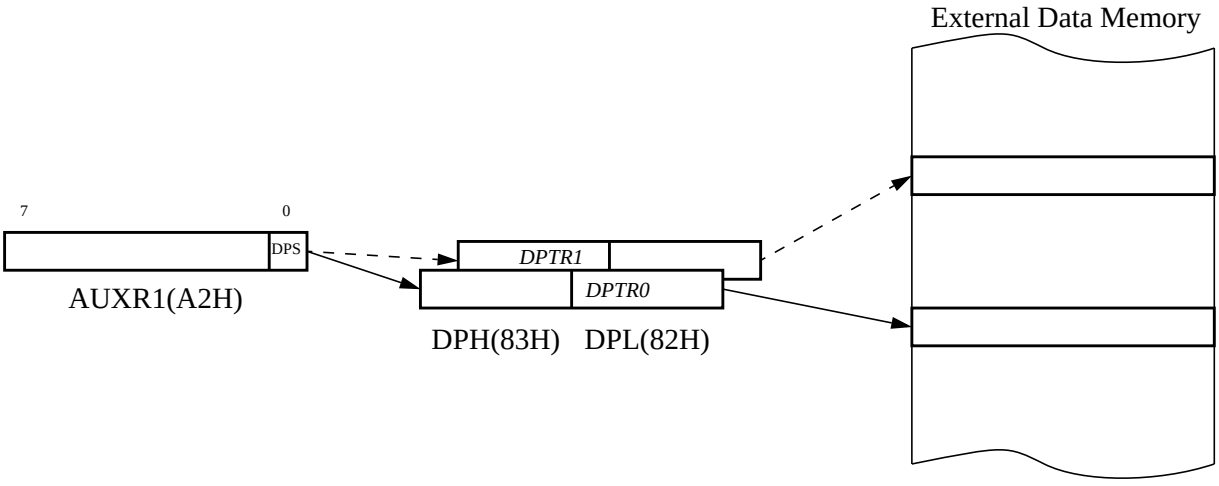


Figure 9. Use of Dual Pointer

Table 17. AUXR1: Auxiliary Register 1

7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	**DPS**

Bit Number	Bit Mnemonic	Description
7	-	**Reserved** The value read from this bit is indeterminate. Do not set this bit.
6	-	**Reserved** The value read from this bit is indeterminate. Do not set this bit.
5	-	**Reserved** The value read from this bit is indeterminate. Do not set this bit.
4	-	**Reserved** The value read from this bit is indeterminate. Do not set this bit.
3	-	**Reserved** The value read from this bit is indeterminate. Do not set this bit.
2	-	**Reserved** The value read from this bit is indeterminate. Do not set this bit.
1	-	**Reserved** The value read from this bit is indeterminate. Do not set this bit.
0	DPS	**Data Pointer Selection** Clear to select DPTR0. Set to select DPTR1.

User software should not write 1s to reserved bits. These bits may be used in future 8051 family products to invoke new feature. In that case, the reset value of the new bit will be 0, and its active value will be 1. The value read from a reserved bit is indeterminate.

Application

Software can take advantage of the additional data pointers to both increase speed and reduce code size, for example, block operations (copy, compare, search ...) are well served by using one data pointer as a ’source’ pointer and the other one as a "destination" pointer.

```
; Block move using dual data pointers
; Destroys DPTR0, DPTR1, A and PSW
; note: DPS exits opposite of entry state
; unless an extra INC AUXR1 is added
;
00A2 AUXR1 EQU 0A2H
;
0000 909000MOV DPTR,#SOURCE ; address of SOURCE
0003 05A2 INC AUXR1 ; switch data pointers
0005 90A000 MOV DPTR,#DEST ; address of DEST
0008 LOOP:
0008 05A2 INC AUXR1 ; switch data pointers
000A E0 MOVX A,@DPTR ; get a byte from SOURCE
000B A3 INC DPTR ; increment SOURCE address
000C 05A2 INC AUXR1 ; switch data pointers
000E F0 MOVX @DPTR,A ; write the byte to DEST
000F A3 INC DPTR ; increment DEST address
0010 70F6JNZ LOOP ; check for 0 terminator
0012 05A2 INC AUXR1 ; (optional) restore DPS
```

INC is a short (2 bytes) and fast (12 clocks) way to manipulate the DPS bit in the AUXR1 SFR. However, note that the INC instruction does not directly force the DPS bit to a particular state, but simply toggles it. In simple routines, such as the block move example, only the fact that DPS is toggled in the proper sequence matters, not its actual value. In other words, the block move routine works the same whether DPS is '0' or '1' on entry. Observe that without the last instruction (INC AUXR1), the routine will exit with DPS in the opposite state.

11. Serial I/O Ports enhancements

The serial I/O ports in the T80C5112 are compatible with the serial I/O port in the 80C52.
They provide both synchronous and asynchronous communication modes. They operate as Universal Asynchronous Receiver and Transmitter (UART) in three full-duplex modes (Modes 1, 2 and 3). Asynchronous transmission and reception can occur simultaneously and at different baud rates

Serial I/O ports include the following enhancements:

- Framing error detection
- Automatic address recognition

11.1. Framing Error Detection

Framing bit error detection is provided for the three asynchronous modes (modes 1, 2 and 3). To enable the framing bit error detection feature, set SMOD0 bit in PCON register (See Figure 10).

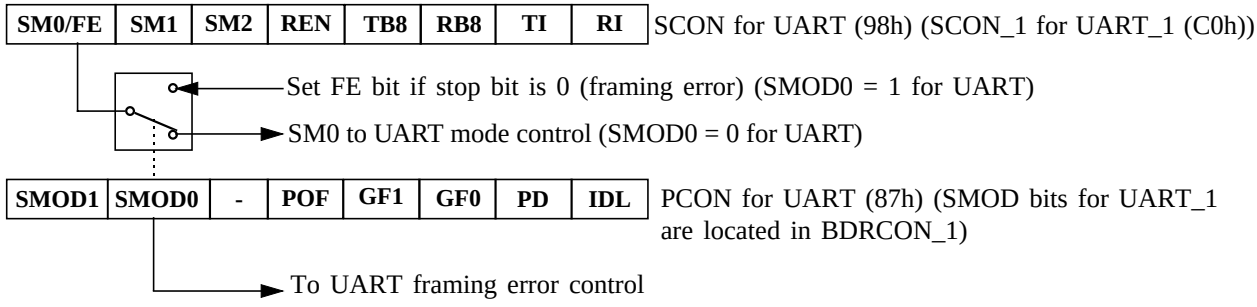


Figure 10. Framing Error Block Diagram

When this feature is enabled, the receiver checks each incoming data frame for a valid stop bit. An invalid stop bit may result from noise on the serial lines or from simultaneous transmission by two CPUs. If a valid stop bit is not found, the Framing Error bit (FE) in SCON register (See Table 18) bit is set.
Software may examine FE bit after each reception to check for data errors. Once set, only software or a reset can clear FE bit. Subsequently received frames with valid stop bits cannot clear FE bit. When FE feature is enabled, RI rises on stop bit instead of the last data bit (See Figure 11. and Figure 12.).

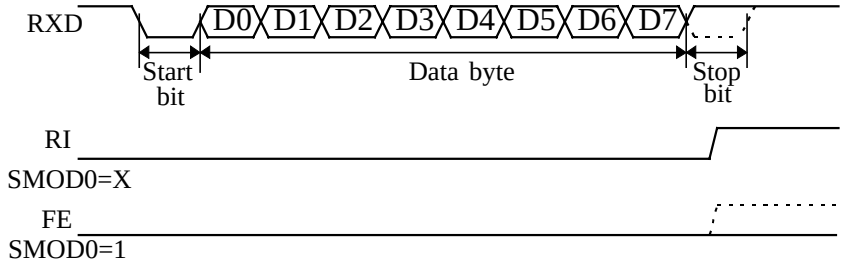


Figure 11. UART Timings in Mode 1

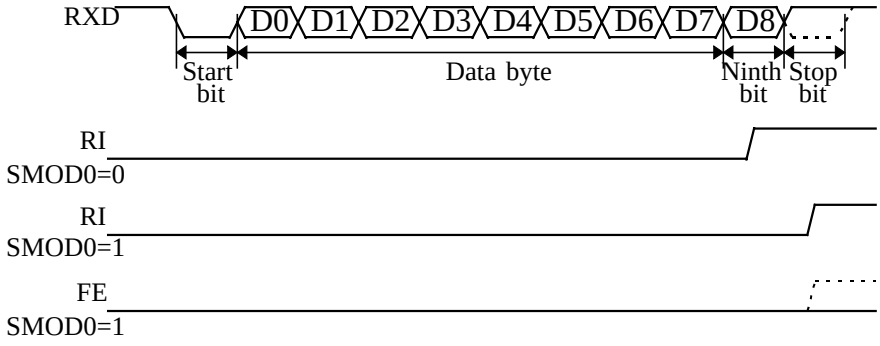


Figure 12. UART Timings in Modes 2 and 3

11.2. Automatic Address Recognition

The automatic address recognition feature is enabled for each UART when the multiprocessor communication feature is enabled (SM2 bit in SCON register is set).
Implemented in hardware, automatic address recognition enhances the multiprocessor communication feature by allowing the serial port to examine the address of each incoming command frame. Only when the serial port recognizes its own address, the receiver sets RI bit in SCON register to generate an interrupt. This ensures that the CPU is not interrupted by command frames addressed to other devices.
If desired, you may enable the automatic address recognition feature in mode 1. In this configuration, the stop bit takes the place of the ninth data bit. Bit RI is set only when the received command frame address matches the device's address and is terminated by a valid stop bit.
To support automatic address recognition, a device is identified by a given address and a broadcast address.

NOTE: The multiprocessor communication and automatic address recognition features cannot be enabled in mode 0 (i.e. setting SM2 bit in SCON register in mode 0 has no effect).

11.2.1. Given Address

Each UART has an individual address that is specified in SADDR register; the SADEN register is a mask byte that contains don't-care bits (defined by zeros) to form the device's given address. The don't-care bits provide the flexibility to address one or more slaves at a time. The following example illustrates how a given address is formed. To address a device by its individual address, the SADEN mask byte must be `1111 1111b`.
For example:

```
SADDR      0101 0110b
SADEN      1111 1100b
Given      0101 01XXb
```

The following is an example of how to use given addresses to address different slaves:

```
Slave A:   SADDR      1111 0001b
           SADEN      1111 1010b
           Given      1111 0X0Xb

Slave B:   SADDR      1111 0011b
           SADEN      1111 1001b
           Given      1111 0XX1b

Slave C:   SADDR      1111 0010b
           SADEN      1111 1101b
           Given      1111 00X1b
```

The SADEN byte is selected so that each slave may be addressed separately.
For slave A, bit 0 (the LSB) is a don't-care bit; for slaves B and C, bit 0 is a 1. To communicate with slave A only, the master must send an address where bit 0 is clear (e.g. 1111 0000b).
For slave A, bit 1 is a 1; for slaves B and C, bit 1 is a don't care bit. To communicate with slaves B and C, but not slave A, the master must send an address with bits 0 and 1 both set (e.g. 1111 0011b).
To communicate with slaves A, B and C, the master must send an address with bit 0 set, bit 1 clear, and bit 2 clear (e.g. 1111 0001b).

11.2.2. Broadcast Address

A broadcast address is formed from the logical OR of the SADDR and SADEN registers with zeros defined as don't-care bits, e.g.:

```
          SADDR            0101 0110b
          SADEN            1111 1100b
Broadcast =SADDR OR SADEN   1111 111Xb
```

The use of don't-care bits provides flexibility in defining the broadcast address, however in most applications, a broadcast address is FFh. The following is an example of using broadcast addresses:

```
Slave A:   SADDR      1111 0001b
           SADEN      1111 1010b
           Broadcast  1111 1X11b,

Slave B:   SADDR      1111 0011b
           SADEN      1111 1001b
           Broadcast  1111 1X11B,

Slave C:   SADDR=     1111 0010b
           SADEN      1111 1101b
           Broadcast  1111 1111b
```

For slaves A and B, bit 2 is a don't care bit; for slave C, bit 2 is set. To communicate with all of the slaves, the master must send an address FFh. To communicate with slaves A and B, but not slave C, the master can send and address FBh.

11.2.3. Reset Addresses

On reset, the SADDR and SADEN registers are initialized to 00h, i.e. the given and broadcast addresses are XXXX XXXXb (all don't-care bits). This ensures that the serial port will reply to any address, and so, that it is backwards compatible with the 80C51 microcontrollers that do not support automatic address recognition.

11.3. Baud Rate Selection for UART for mode 1 and 3

The Baud Rate Generator for transmit and receive clocks can be selected separately via the T2CON and BDRCON registers.

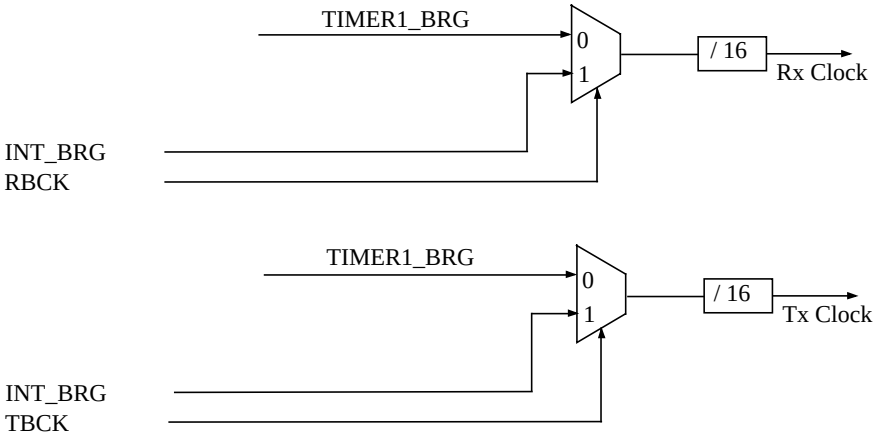


Figure 13. Baud Rate selection

11.3.1. Baud Rate selection table for UART

TBCK	RBCK	Clock Source for UART Tx	Clock Source UART Rx
0	0	Timer 1	Timer 1
1	0	INT_BRG	Timer 1
0	1	Timer 1	INT_BRG
1	1	INT_BRG	INT_BRG

11.3.2. Internal Baud Rate Generator (BRG)

When the internal Baud Rate Generator is used, the Baud Rates are determined by the BRG overflow depending on the BRL reload value, the X2 bit in CKON0 register, the value of SPD bit (Speed Mode) in BDRCON register and the value of the SMOD1 bit in PCON register (for UART). :

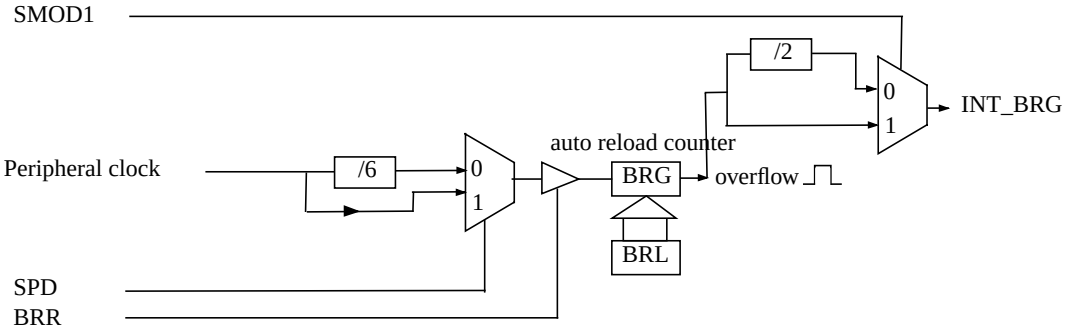


Figure 14. Internal Baud Rate Generator

- for UART

$$Baud\_Rate = \frac{2^{SMOD1} \times 2^{X2} \times F_{XTAL}}{2 \times 2 \times 6^{(1-SPD)} \times 16 \times [256 - (BRL)]}$$

$$(BRL) = 256 - \frac{2^{SMOD1} \times 2^{X2} \times F_{XTAL}}{2 \times 2 \times 6^{(1-SPD)} \times 16 \times Baud\_Rate}$$

Example of computed value when X2=1, SMOD1=1, SPD=1

Baud Rates	F_{XTAL} = 16.384 MHz		F_{XTAL} = 24MHz	
	BRL	Error (%)	BRL	Error (%)
115200	247	1.23	243	0.16
57600	238	1.23	230	0.16
38400	229	1.23	217	0.16
28800	220	1.23	204	0.16
19200	203	0.63	178	0.16
9600	149	0.31	100	0.16
4800	43	1.23	-	-

Example of computed value when X2=0, SMOD1=0, SPD=0

Baud Rates	F_{OSC} = 16.384 MHz		F_{OSC} = 24MHz	
	BRL	Error (%)	BRL	Error (%)
4800	247	1.23	243	0.16
2400	238	1.23	230	0.16
1200	220	1.23	202	3.55
600	185	0.16	152	0.16

The baud rate generator can be used for mode 1 or 3 (refer to figures 13), but also for mode 0 for both UARTs, thanks to the bit SRC located in BDRCON register (Table 20)

11.4. UARTs registers

SADEN - Slave Address Mask Register for UART (B9h)

7	6	5	4	3	2	1	0

Reset Value = 0000 0000b

SADDR - Slave Address Register for UART (A9h)

7	6	5	4	3	2	1	0

Reset Value = 0000 0000b

SBUF - Serial Buffer Register for UART (99h)

7	6	5	4	3	2	1	0

Reset Value = XXXX XXXXb

BRL - Baud Rate Reload Register for the internal baud rate generator, UART UART(9Ah)

7	6	5	4	3	2	1	0

Reset Value = 0000 0000b

Table 18. SCON Register

SCON - Serial Control Register for UART (98h)

7	6	5	4	3	2	1	0
FE/SM0	**SM1**	**SM2**	**REN**	**TB8**	**RB8**	**TI**	**RI**

Bit Number	Bit Mnemonic	Description
7	FE	**Framing Error bit (SMOD0=1) for UART** Clear to reset the error state, not cleared by a valid stop bit. Set by hardware when an invalid stop bit is detected. SMOD0 must be set to enable access to the FE bit
	SM0	**Serial port Mode bit 0 (SMOD0=0) for UART** Refer to SM1 for serial port mode selection. SMOD0 must be cleared to enable access to the SM0 bit
6	SM1	**Serial port Mode bit 1 for UART** SM0 SM1 ModeDescriptionBaud Rate 0 0 0Shift Register$F_{XTAL}/12$ ($F_{XTAL}/6$ X2 mode) 0 1 18-bit UARTVariable 1 0 29-bit UART$F_{XTAL}/64$ or $F_{XTAL}/32$ ($F_{XTAL}/32$ or $F_{XTAL}/16$ X2 mode) 1 1 39-bit UARTVariable
5	SM2	**Serial port Mode 2 bit / Multiprocessor Communication Enable bit for UART** Clear to disable multiprocessor communication feature. Set to enable multiprocessor communication feature in mode 2 and 3, and eventually mode 1. This bit should be cleared in mode 0.
4	REN	**Reception Enable bit for UART** Clear to disable serial reception. Set to enable serial reception.
3	TB8	**Transmitter Bit 8 / Ninth bit to transmit in modes 2 and 3 for UART**. Clear to transmit a logic 0 in the 9th bit. Set to transmit a logic 1 in the 9th bit.
2	RB8	**Receiver Bit 8 / Ninth bit received in modes 2 and 3 for UART** Cleared by hardware if 9th bit received is a logic 0. Set by hardware if 9th bit received is a logic 1. In mode 1, if SM2 = 0, RB8 is the received stop bit. In mode 0 RB8 is not used.
1	TI	**Transmit Interrupt flag for UART** Clear to acknowledge interrupt. Set by hardware at the end of the 8th bit time in mode 0 or at the beginning of the stop bit in the other modes.
0	RI	**Receive Interrupt flag for UART** Clear to acknowledge interrupt. Set by hardware at the end of the 8th bit time in mode 0, see Figure 11. and Figure 12. in the other modes.

Reset Value = 0000 0000b

Bit addressable

Table 19. PCON Register

PCON - Power Control Register (87h)

7	6	5	4	3	2	1	0
SMOD1	**SMOD0**	**RSTD**	**POF**	**GF1**	**GF0**	**PD**	**IDL**

Bit Number	Bit Mnemonic	Description
7	SMOD1	**Serial port Mode bit 1 for UART** Set to select double baud rate in mode 1, 2 or 3.
6	SMOD0	**Serial port Mode bit 0 for UART** Clear to select SM0 bit in SCON register. Set to to select FE bit in SCON register.
5	RSTD	**Reset Detector Disable Bit** Clear to disable PFD. Set to enable PFD.
4	POF	**Power-Off Flag** Clear to recognize next reset type. Set by hardware when VCC rises from 0 to its nominal voltage. Can also be set by software.
3	GF1	**General purpose Flag** Cleared by user for general purpose usage. Set by user for general purpose usage.
2	GF0	**General purpose Flag** Cleared by user for general purpose usage. Set by user for general purpose usage.
1	PD	**Power-Down mode bit** Cleared by hardware when reset occurs. Set to enter power-down mode.
0	IDL	**Idle mode bit** Clear by hardware when interrupt or reset occurs. Set to enter idle mode.

Reset Value = 0001 0000b
Not bit addressable

Power-off flag reset value will be 1 only after a power on (cold reset). A warm reset doesn't affect the value of this bit.

Table 20. BDRCON Register

BDRCON - Baud Rate Control Register (9Bh)

7	6	5	4	3	2	1	0
-	-	-	BRR	TBCK	RBCK	SPD	SRC

Bit Number	Bit Mnemonic	Description
7	-	**Reserved** The value read from this bit is indeterminate. Do not set this bit
6	-	**Reserved** The value read from this bit is indeterminate. Do not set this bit
5	-	**Reserved** The value read from this bit is indeterminate. Do not set this bit.
4	BRR	**Baud Rate Run Control bit** Clear to stop the internal Baud Rate Generator. Set to start the internal Baud Rate Generator.
3	TBCK	**Transmission Baud rate Generator Selection bit for UART** Clear to select Timer 1 or Timer 2 for the Baud Rate Generator. Set to select internal Baud Rate Generator.
2	RBCK	**Reception Baud Rate Generator Selection bit for UART** Clear to select Timer 1 or Timer 2 for the Baud Rate Generator. Set to select internal Baud Rate Generator.
1	SPD	**Baud Rate Speed Control bit for UART** Clear to select the SLOW Baud Rate Generator. Set to select the FAST Baud Rate Generator.
0	SRC	**Baud Rate Source select bit in Mode 0 for UART** Clear to select $F_{OSC}/12$ as the Baud Rate Generator ($F_{OSC}/6$ in X2 mode). Set to select the internal Baud Rate Generator for UARTs in mode 0.

Reset Value = XXX0 0000b

12. Serial Port Interface (SPI)

12.1. Introduction

The Serial Peripheral Interface module (SPI) which allows full-duplex, synchronous, serial communication between the MCU and peripheral devices, including other MCUs.

12.2. Features

Features of the SPI module include the following:

- Full-duplex, three-wire synchronous transfers
- Master or Slave operation
- Eight programmable Master clock rates
- Serial clock with programmable polarity and phase
- Master Mode fault error flag with MCU interrupt capability
- Write collision flag protection

12.3. Signal Description

Figure 15 shows a typical SPI bus configuration using one Master controller and many Slave peripherals. The bus is made of three wires connecting all the devices:

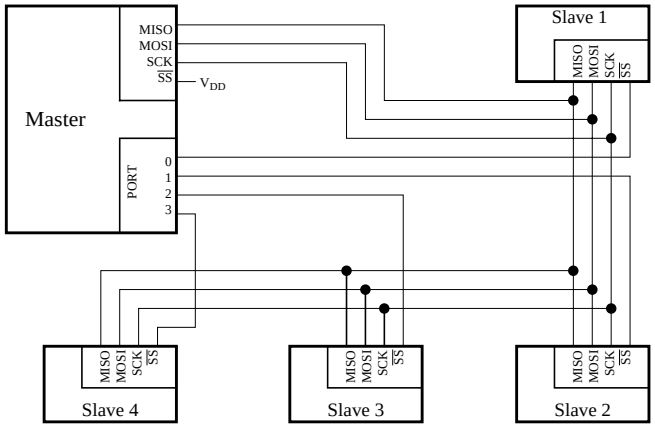


Figure 15. Typical SPI bus

The Master device selects the individual Slave devices by using four pins of a parallel port to control the four $\overline{SS}$ pins of the Slave devices.

12.3.1. Master Output Slave Input (MOSI)

This 1-bit signal is directly connected between the Master Device and a Slave Device. The MOSI line is used to transfer data in series from the Master to the Slave. Therefore, it is an output signal from the Master, and an input signal to a Slave. A byte (8-bit word) is transmitted most significant bit (MSB) first, least significant bit (LSB)last.

12.3.2. Master Input Slave Output (MISO)

This 1-bit signal is directly connected between the Slave Device and a Master Device. The MISO line is used to transfer data in series from the Slave to the Master. Therefore, it is an output signal from the Slave, and an input signal to the Master. A byte (8-bit word) is transmitted most significant bit (MSB) first, least significant bit (LSB) last.

12.3.3. SPI Serial Clock (SCK)

This signal is used to synchronize the data movement both in and out the devices through their MOSI and MISO lines. It is driven by the Master for eight clock cycles which allows to exchange one byte on the serial lines.

12.3.4. Slave Select ($\overline{SS}$)

Each Slave peripheral is selected by one Slave Select pin ($\overline{SS}$). This signal must stay low for any message for a Slave. It is obvious that only one Master ($\overline{SS}$ high level) can drive the network. The Master may select each Slave device by software through port pins (Figure 15). To prevent bus conflicts on the MISO line, only one slave should be selected at a time by the Master for a transmission.

In a Master configuration, the $\overline{SS}$ line can be used in conjunction with the MODF flag in the SPI Status register (SPSTA) to prevent multiple masters from driving MOSI and SCK (See Error conditions).

A high level on the $\overline{SS}$ pin puts the MISO line of a Slave SPI in a high-impedance state.

The $\overline{SS}$ pin could be used as a general purpose if the following conditions are met:

- The device is configured as a Master and the SSDIS control bit in SPCON is set. This kind of configuration can be found when only one Master is driving the network and there is no way that the $\overline{SS}$ pin will be pulled low. Therefore, the MODF flag in the SPSTA will never be set[1].
- The Device is configured as a Slave with CPHA and SSDIS control bits set[2]. This kind of configuration can happen when the system comprises one Master and one Slave only. Therefore, the device should always be selected and there is no raison that the Master uses the $\overline{SS}$ pin to select the communicating Slave device.

12.3.5. Baud rate

In Master mode, the baud rate can be selected from a baud rate generator which is controled by three bits in the SPCON register: SPR2, SPR1 and SPR0. The Master clock is chosen from one of seven clock rates resulting from the division of the internal clock by 2, 4, 8, 16, 32, 64 or 128, or an external clock.

Table 21 gives the different clock rates selected by SPR2:SPR1:SPR0:

Table 21. SPI Master baud rate selection

SPR2:SPR1:SPR0	Clock Rate	Baud rate divisor (BD)
000	F_{CkIdle} /2	2
001	F_{CkIdle} /4	4
010	F_{CkIdle} / 8	8
011	F_{CkIdle}/16	16
100	F_{CkIdle} /32	32
101	$F_{CkIdleH}$ /64	64
110	F_{CkIdle} /128	128
111	External clock	Output of BRG

1. Clearing SSDIS control bit does not clear MODF.
2. Special care should be taken not to set SSDIS control bit when CPHA = ’0’ because in this mode, the $\overline{SS}$ is used to start the transmission.

12.4. Functional Description

Figure 16 shows a detailed structure of the SPI module.

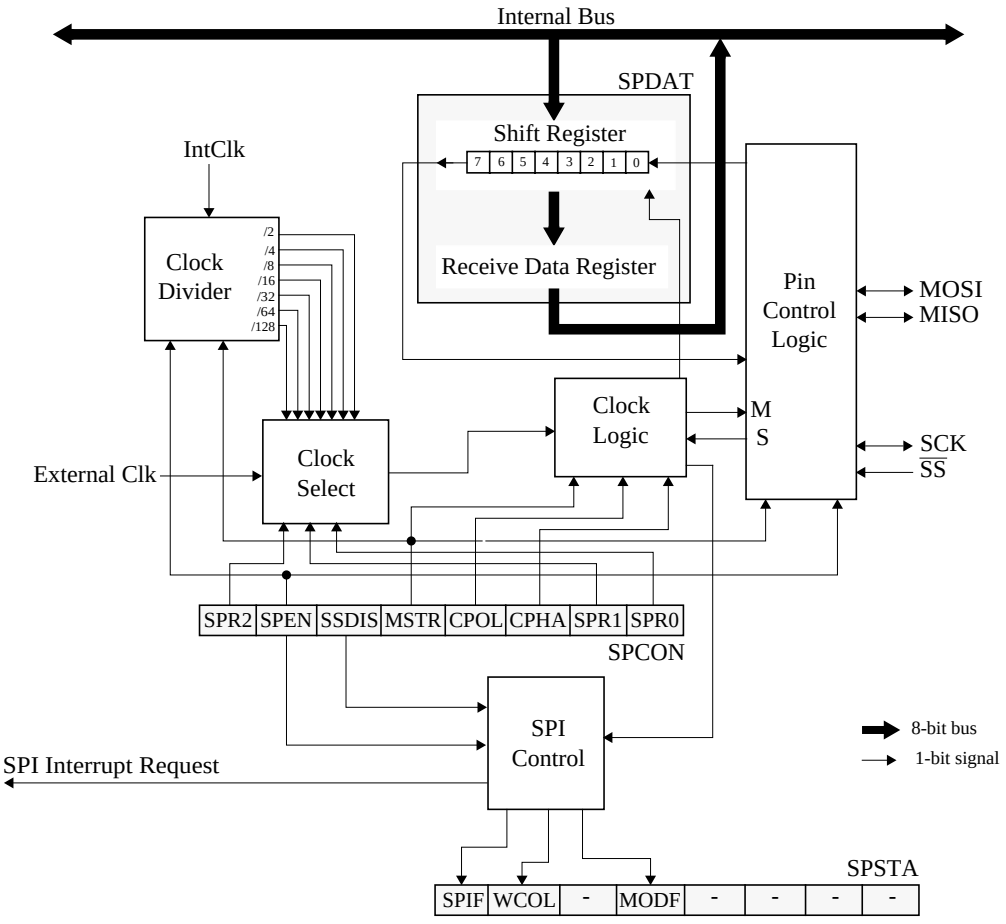


Figure 16. SPI Module Block Diagram

12.4.1. Operating Modes

The Serial Peripheral Interface can be configured as one of the two modes: Master mode or Salve mode. The configuration and initialization of the SPI module is made through one register:

- The Serial Peripheral CONtrol register (SPCON)

Once the SPI is configured, the data exchange is made using:

- SPCON
- The Serial Peripheral STAtus register (SPSTA)
- The Serial Peripheral DATa register (SPDAT)

During an SPI transmission, data is simultaneously transmitted (shifted out serially) and received (shifted in serially). A serial clock line (SCK) synchronizes shifting and sampling on the two serial data lines (MOSI and MISO). A Slave Select line ($\overline{SS}$) allows individual selection of a Slave SPI device; Slave devices that are not selected do not interfere with SPI bus activities.

When the Master device transmits data to the Slave device via the MOSI line, the Slave device responds by sending data to the Master device via the MISO line. This implies full-duplex transmission with both data out and data in synchronized with the same clock (Figure 17).

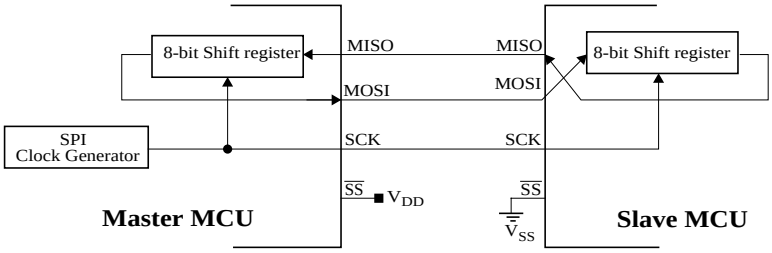


Figure 17. Full-Duplex Master-Slave Interconnection

12.4.1.1. Master mode

The SPI operates in Master mode when the Master bit, MSTR[1], in the SPCON register is set. Only one Master SPI device can initiate transmissions. Software begins the transmission from a Master SPI module by writing to the Serial Peripheral Data Register (SPDAT). If the shift register is empty, the byte is immediately transferred to the shift register. The byte begins shifting out on MOSI pin under the control of the serial clock, SCK. Simultaneously, another byte shifts in from the Slave on the Master's MISO pin. The transmission ends when the Serial Peripheral transfer data flag, SPIF, in SPSTA becomes set. At the same time that SPIF becomes set, the received byte from the Slave is transferred to the receive data register in SPDAT. Software clears SPIF by reading the Serial Peripheral Status register (SPSTA) with the SPIF bit set, and then reading the SPDAT.

When the pin SS is pulled down during a transmission, the data is interrupted and when the transmission is established again, the data present in the SPDAT is resent.

12.4.1.2. Slave mode

The SPI operates in Slave mode when the Master bit, MSTR[2], in the SPCON register is cleared. Before a data transmission occurs, the Slave Select pin, $\overline{SS}$, of the Slave device must be set to '0'. $\overline{SS}$ must remain low until the transmission is complete.

In a Slave SPI module, data enters the shift register under the control of the SCK from the Master SPI module. After a byte enters the shift register, it is immediately transferred to the receive data register in SPDAT, and the SPIF bit is set. To prevent an overflow condition, Slave software must then read the SPDAT before another byte enters the shift register[3]. A Slave SPI must complete the write to the SPDAT (shift register) at least one bus cycle before the Master SPI starts a transmission. If the write to the data register is late, the SPI transmits the data already in the shift register from the previous transmission.

12.4.2. Transmission Formats

Software can select any of four combinations of serial clock (SCK) phase and polarity using two bits in the SPCON: the Clock POLarity (CPOL[4]) and the Clock PHAse (CPHA[4]). CPOL defines the default SCK line level in idle state. It has no significant effect on the transmission format. CPHA defines the edges on which the input data are sampled and the edges on which the output data are shifted (Figure 18 and Figure 19). The clock phase and polarity should be identical for the Master SPI device and the communicating Slave device.

1. The SPI module should be configured as a Master before it is enabled (SPEN set). Also the Master SPI should be configured before the Slave SPI.
2. The SPI module should be configured as a Slave before it is enabled (SPEN set).
3. The maximum frequency of the SCK for an SPI configured as a Slave is the bus clock speed.
4. Before writing to the CPOL and CPHA bits, the SPI should be disabled (SPEN = '0').

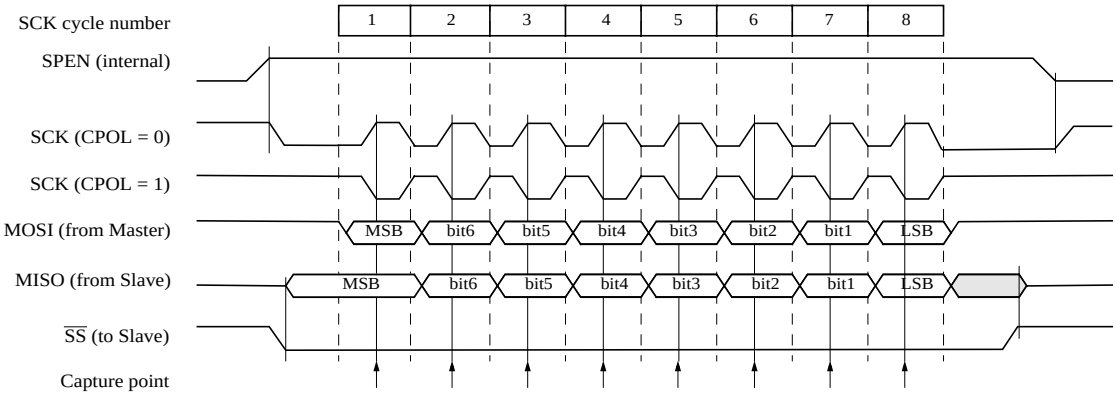


Figure 18. Data Transmission Format (CPHA = 0)

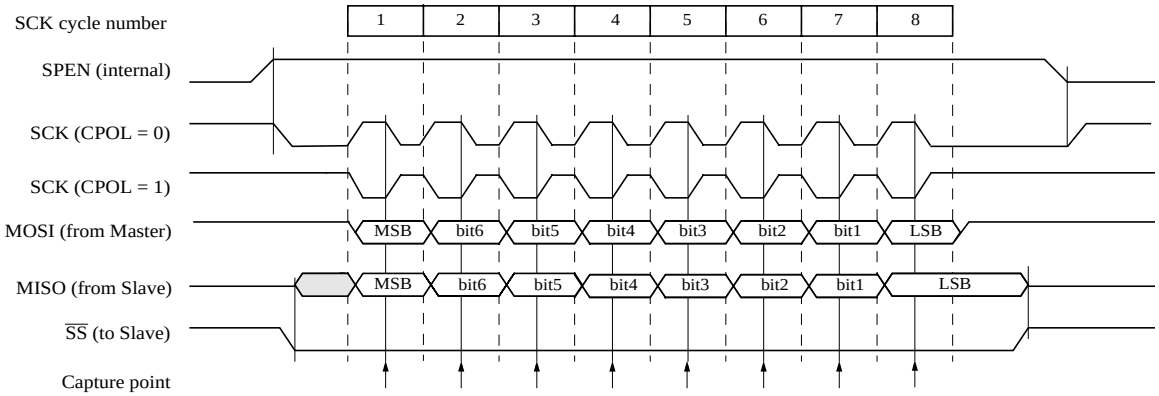


Figure 19. Data Transmission Format (CPHA = 1)

As shown in Figure 18, the first SCK edge is the MSB capture strobe. Therefore the Slave must begin driving its data before the first SCK edge, and a falling edge on the $\overline{SS}$ pin is used to start the transmission. The $\overline{SS}$ pin must be toggled high and then low between each byte transmitted (Figure 20).

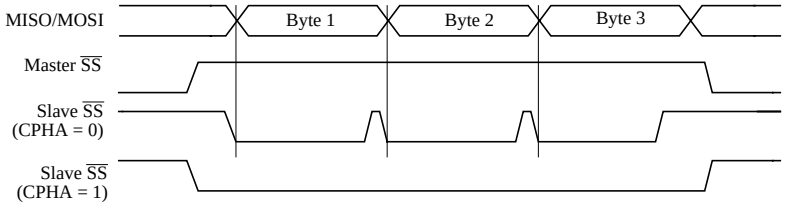


Figure 20. CPHA/$\overline{SS}$ timing

Figure 19 shows an SPI transmission in which CPHA is '1'. In this case, the Master begins driving its MOSI pin on the first SCK edge. Therefore the Slave uses the first SCK edge as a start transmission signal. The $\overline{SS}$ pin can remain low between transmissions (Figure 20). This format may be preferable in systems having only one Master and only one Slave driving the MISO data line.

12.4.3. Error conditions

The following flags in the SPSTA signal SPI error conditions:

12.4.3.1. Mode Fault (MODF)

MODe Fault error in Master mode SPI indicates that the level on the Slave Select ($\overline{SS}$) pin is inconsistent with the actual mode of the device. MODF is set to warn that there may have a multi-master conflict for system control. In this case, the SPI system is affected in the following ways:

- An SPI receiver/error CPU interrupt request is generated.
- The SPEN bit in SPCON is cleared. This disable the SPI.
- The MSTR bit in SPCON is cleared.

When $\overline{SS}$ DISable (SSDIS) bit in the SPCON register is cleared, the MODF flag is set when the $\overline{SS}$ signal becomes '0'.

However, as stated before, for a system with one Master, if the $\overline{SS}$ pin of the Master device is pulled low, there is no way that another Master is attempting to drive the network. In this case, to prevent the MODF flag from being set, software can set the SSDIS bit in the SPCON register and therefore making the $\overline{SS}$ pin as a general purpose I/O pin.

Clearing the MODF bit is accomplished by a read of SPSTA register with MODF bit set, followed by a write to the SPCON register. SPEN Control bit may be restored to its original set state after the MODF bit has been cleared.

12.4.3.2. Write Collision (WCOL)

A Write COLlision (WCOL) flag in the SPSTA is set when a write to the SPDAT register is done during a transmit sequence.

WCOL does not cause an interruption, and the transfer continues uninterrupted.

Clearing the WCOL bit is done through a software sequence of an access to SPSTA and an access to SPDAT.

12.4.3.3. Overrun Condition

An overrun condition occurs when the Master device tries to send several data bytes and the Slave devise has not cleared the SPIF bit issuing from the previous data byte transmitted. In this case, the receiver buffer contains the byte sent after the SPIF bit was last cleared. A read of the SPDAT returns this byte. All others bytes are lost.

This condition is not detected by the SPI peripheral.

12.4.4. Interrupts

Two SPI status flags can generate a CPU interrupt requests:

Flag	Request
SPIF (SP data transfer)	SPI Transmitter Interrupt request
MODF (Mode Fault)	SPI Receiver/Error Interrupt Request (if SSDIS = '0')

Table 22. SPI Interrupts

Serial Peripheral data transfer flag, SPIF: This bit is set by hardware when a transfer has been completed. SPIF bit generates transmitter CPU interrupt requests.

Mode Fault flag, MODF: This bit becomes set to indicate that the level on the $\overline{SS}$ is inconsistent with the mode of the SPI. MODF with SSDIS reset, generates receiver/error CPU interrupt requests.

Figure 21 gives a logical view of the above statements:

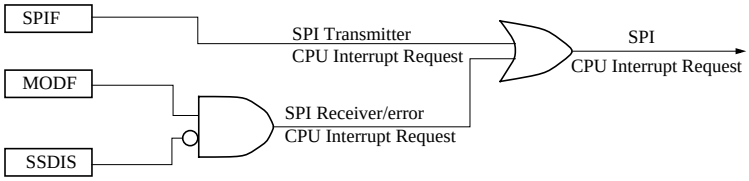


Figure 21. SPI Interrupt Requests Generation

12.4.5. Registers

There are three registers in the module that provide control, status and data storage functions. These registers are describes in the following paragraphs.

12.4.5.1. Serial Peripheral CONtrol register (SPCON)

The Serial Peripheral Control Register does the following:

- Selects one of the Master clock rates,
- Configure the SPI module as Master or Slave,
- Selects serial clock polarity and phase,
- Enables the SPI module,
- Frees the $\overline{SS}$ pin for a general purpose

Table 23 describes this register and explains the use of each bit:

Table 23. Serial Peripheral Control Register

7	6	5	4	3	2	1	0
SPR2	SPEN	SSDIS	MSTR	CPOL	CPHA	SPR1	SPR0

Bit Number	Bit Mnemonic	R/W Mode	Description
7	SPR2	RW	Serial Peripheral Rate 2 Bit with SPR1 and SPR0 define the clock rate
6	SPEN	RW	Serial Peripheral Enable Clear to disable the SPI interface Set to enable the SPI interface
5	SSDIS	RW	$\overline{SS}$ Disable Clear to enable SS# in both Master and Slave modes Set to disable SS# in both Master and Slave modes. In Slave mode, this bit has no effect if CPHA = '0'
4	MSTR	RW	Serial Peripheral Master Clear to configure the SPI as a Slave Set to configure the SPI as a Master
3	CPOL	RW	Clock Polarity Clear to have the SCK set to '0' in idle state Set to have the SCK set to '1' in idle low
2	CPHA	RW	Clock Phase Clear to have the data sampled when the SPSCK leaves the idle state (see CPOL) Set to have the data sampled when the SPSCK returns to idle state (see CPOL)

Bit Number	Bit Mnemonic	R/W Mode	Description
1	SPR1	RW	Serial Peripheral Rate (SPR2:SPR1:SPR0) 000 : $F_{CLK\ PERIPH}$ /2 001 : $F_{CLK\ PERIPH}$ /4 010 : $F_{CLK\ PERIPH}$ /8 011 : $F_{CLK\ PERIPH}$ /16
0	SPR0	RW	100 : $F_{CLK\ PERIPH}$ /32 101 : $F_{CLK\ PERIPH}$ /64 110 : $F_{CLK\ PERIPH}$ /128 111 : External clock, output of BRG

Reset Value= 00010100b

12.4.5.2. Serial Peripheral STAtus register (SPSTA)

The Serial Peripheral Status Register contains flags to signal the following conditions:

- Data transfer complete
- Write collision
- Inconsistent logic level on $\overline{SS}$ pin (mode fault error)

Table 24 describes the SPSTA register and explains the use of every bit in the register:

7	6	5	4	3	2	1	0
SPIF	WCOL	-	MODF	-	-	-	-

Bit Number	Bit Mnemonic	R/W Mode	Description
7	SPIF	R	Serial Peripheral data transfer flag Clear by hardware to indicate data transfer is in progress or has been approved by a clearing sequence. Set by hardware to indicate that the data transfer has been completed.
6	WCOL	R	Write Collision flag Cleared by hardware to indicate that no collision has occurred or has been approved by a clearing sequence. Set by hardware to indicate that a collision has been detected.
5	-	RW	Reserved The value read from this bit is indeterminate. Do not set this bit
4	MODF	R	Mode Fault Cleared by hardware to indicate that the $\overline{SS}$ pin is at appropriate logic level, or has been approved by a clearing sequence. Set by hardware to indicate that the $\overline{SS}$ pin is at inappropriate logic level
3	-	RW	Reserved The value read from this bit is indeterminate. Do not set this bit
2	-	RW	Reserved The value read from this bit is indeterminate. Do not set this bit
1	-	RW	Reserved The value read from this bit is indeterminate. Do not set this bit
0	-	RW	Reserved The value read from this bit is indeterminate. Do not set this bit

Reset Value= 00X0XXXXb

Table 24. Serial Peripheral Status and Control register

12.4.5.3. Serial Peripheral DATa register (SPDAT)

The Serial Peripheral Data Register (Table 25) is a read/write buffer for the receive data register. A write to SPDAT places data directly into the shift register. No transmit buffer is available in this model.

A Read of the SPDAT returns the value located in the receive buffer and not the content of the shift register.

Table 25. Serial Peripheral Data Register

7	6	5	4	3	2	1	0
R7	R6	R5	R4	R3	R2	R1	R0

Reset Value= XXXX XXXXb

R7:R0 : Receive data bits

SPCON, SPSTA and SPDAT registers may be read and written at any time while there is no on-going exchange. However, special care should be taken when writing to them while a transmission is on-going:

- Do not change SPR2, SPR1 and SPR0
- Do not change CPHA and CPOL
- Do not change MSTR
- Clearing SPEN would immediately disable the peripheral
- Writing to the SPDAT will cause an overflow

13. Programmable Counter Array PCA

The PCA provides more timing capabilities with less CPU intervention than the standard timer/counters. Its advantages include reduced software overhead and improved accuracy. The PCA consists of a dedicated timer/ counter which serves as the time base for an array of five compare/ capture modules. Its clock input can be programmed to count any one of the following signals:

- Oscillator frequency ÷ 12 (÷ 6 in X2 mode)
- Oscillator frequency ÷ 4 (÷ 2 in X2 mode)
- Timer 0 overflow
- External input on ECI (P1.2)

Each compare/capture modules can be programmed in any one of the following modes:

- rising and/or falling edge capture,
- software timer,
- high-speed output, or
- pulse width modulator.

Module 4 can also be programmed as a watchdog timer (See Section "PCA Watchdog Timer", page 58).

When the compare/capture modules are programmed in the capture mode, software timer, or high speed output mode, an interrupt can be generated when the module executes its function. All five modules plus the PCA timer overflow share one interrupt vector.

The PCA timer/counter and compare/capture modules share Port 1 for external I/O. These pins are listed below. If the port is not used for the PCA, it can still be used for standard I/O.

PCA component	External I/O Pin
16-bit Counter	P1.2 / ECI
16-bit Module 0	P1.3 / CEX0
16-bit Module 1	P1.4 / CEX1
16-bit Module 2	P1.5 / CEX2
16-bit Module 3	P1.6 / CEX3
16-bit Module 4	P1.7 / CEX4

The PCA timer is a common time base for all five modules (See Figure 22). The timer count source is determined from the CPS1 and CPS0 bits in the **CMOD SFR** (See Table 26) and can be programmed to run at:

- 1/12 the oscillator frequency. (Or 1/6 in X2 Mode)
- 1/4 the oscillator frequency. (Or 1/2 in X2 Mode)
- The Timer 0 overflow.
- The input on the ECI pin (P1.2).

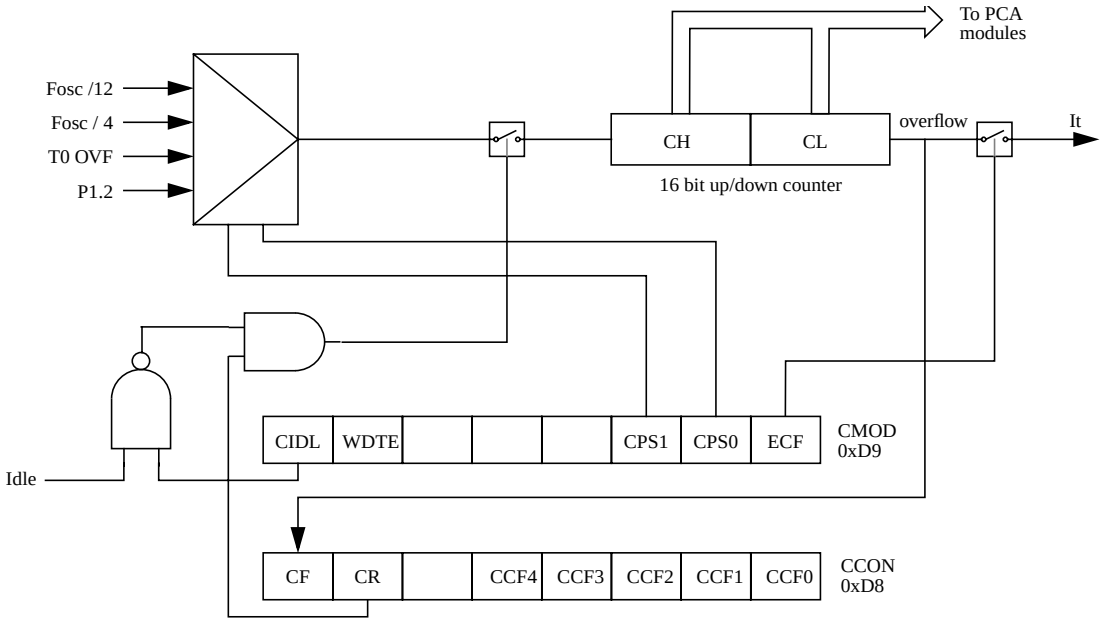


Figure 22. PCA Timer/Counter

Table 26. CMOD: PCA Counter Mode Register

CMOD Address 0D9H	CIDL	WDTE	-	-	-	CPS1	CPS0	ECF
Reset value	0	0	X	X	X	0	0	0

Symbol	Function		
CIDL	Counter Idle control: CIDL = 0 programs the PCA Counter to continue functioning during idle Mode. CIDL = 1 programs it to be gated off during idle.		
WDTE	Watchdog Timer Enable: WDTE = 0 disables Watchdog Timer function on PCA Module 4. WDTE = 1 enables it.		
-	Not implemented, reserved for future use.[a]		
CPS1	PCA Count Pulse Select bit 1.		
CPS0	PCA Count Pulse Select bit 0.		
	CPS1	CPS0	Selected PCA input.[b]
	0	0	Internal clock f_{osc}/12 (Or f_{osc}/6 in X2 Mode).
	0	1	Internal clock f_{osc}/4 (Or f_{osc}/2 in X2 Mode).
	1	0	Timer 0 Overflow
	1	1	External clock at ECI/P1.2 pin (max rate = f_{osc}/ 8)
ECF	PCA Enable Counter Overflow interrupt: ECF = 1 enables CF bit in CCON to generate an interrupt. ECF = 0 disables that function of CF.		

a. User software should not write 1s to reserved bits. These bits may be used in future 8051 family products to invoke new features. In that case, the reset or inactive value of the new bit will be 0, and its active value will be 1. The value read from a reserved bit is indeterminate.
b. f_{osc} = oscillator frequency

The CMOD SFR includes three additional bits associated with the PCA (See Figure 22 and Table 26).

- The CIDL bit which allows the PCA to stop during idle mode.
- The WDTE bit which enables or disables the watchdog function on module 4.
- The ECF bit which when set causes an interrupt and the PCA overflow flag CF (in the CCON SFR) to be set when the PCA timer overflows.

The CCON SFR contains the run control bit for the PCA and the flags for the PCA timer (CF) and each module (Refer to Table 27).

- Bit CR (CCON.6) must be set by software to run the PCA. The PCA is shut off by clearing this bit.
- Bit CF: The CF bit (CCON.7) is set when the PCA counter overflows and an interrupt will be generated if the ECF bit in the CMOD register is set. The CF bit can only be cleared by software.
- Bits 0 through 4 are the flags for the modules (bit 0 for module 0, bit 1 for module 1, etc.) and are set by hardware when either a match or a capture occurs. These flags also can only be cleared by software.

Table 27. CCON: PCA Counter Control Register

CCON Address 0D8H	CF	CR	-	CCF4	CCF3	CCF2	CCF1	CCF0
Reset value	0	0	X	0	0	0	0	0

Symbol	Function
CF	PCA Counter Overflow flag. Set by hardware when the counter rolls over. CF flags an interrupt if bit ECF in CMOD is set. CF may be set by either hardware or software but can only be cleared by software.
CR	PCA Counter Run control bit. Set by software to turn the PCA counter on. Must be cleared by software to turn the PCA counter off.
-	Not implemented, reserved for future use.[a]
CCF4	PCA Module 4 interrupt flag. Set by hardware when a match or capture occurs. Must be cleared by software.
CCF3	PCA Module 3 interrupt flag. Set by hardware when a match or capture occurs. Must be cleared by software.
CCF2	PCA Module 2 interrupt flag. Set by hardware when a match or capture occurs. Must be cleared by software.
CCF1	PCA Module 1 interrupt flag. Set by hardware when a match or capture occurs. Must be cleared by software.
CCF0	PCA Module 0 interrupt flag. Set by hardware when a match or capture occurs. Must be cleared by software.

a. User software should not write 1s to reserved bits. These bits may be used in future 8051 family products to invoke new features. In that case, the reset or inactive value of the new bit will be 0, and its active value will be 1. The value read from a reserved bit is indeterminate.

The watchdog timer function is implemented in module 4 (See Figure 25).

The PCA interrupt system is shown in Figure 23

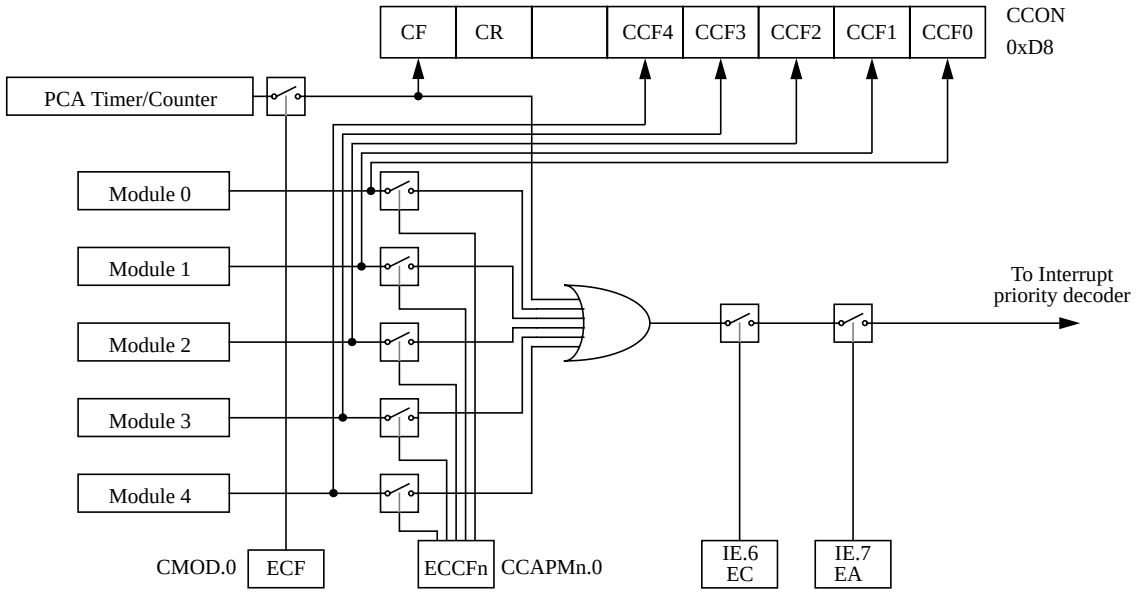


Figure 23. PCA Interrupt System

PCA Modules: each one of the five compare/capture modules has six possible functions. It can perform:

- 16-bit Capture, positive-edge triggered,
- 16-bit Capture, negative-edge triggered,
- 16-bit Capture, both positive and negative-edge triggered,
- 16-bit Software Timer,
- 16-bit High Speed Output,
- 8-bit Pulse Width Modulator.

In addition, module 4 can be used as a Watchdog Timer.

Each module in the PCA has a special function register associated with it. These registers are: CCAPM0 for module 0, CCAPM1 for module 1, etc. (See Table 28). The registers contain the bits that control the mode that each module will operate in.

- The ECCF bit (CCAPMn.0 where n=0, 1, 2, 3, or 4 depending on the module) enables the CCF flag in the CCON SFR to generate an interrupt when a match or compare occurs in the associated module.
- PWM (CCAPMn.1) enables the pulse width modulation mode.
- The TOG bit (CCAPMn.2) when set causes the CEX output associated with the module to toggle when there is a match between the PCA counter and the module's capture/compare register.
- The match bit MAT (CCAPMn.3) when set will cause the CCFn bit in the CCON register to be set when there is a match between the PCA counter and the module's capture/compare register.
- The next two bits CAPN (CCAPMn.4) and CAPP (CCAPMn.5) determine the edge that a capture input will be active on. The CAPN bit enables the negative edge, and the CAPP bit enables the positive edge. If both bits are set both edges will be enabled and a capture will occur for either transition.
- The last bit in the register ECOM (CCAPMn.6) when set enables the comparator function.

Table 29 shows the CCAPMn settings for the various PCA functions.

Table 28. CCAPMn: PCA Modules Compare/Capture Control Registers

CCAPMn Address n = 0 - 4	CCAPM0=0DAH CCAPM1=0DBH CCAPM2=0DCH CCAPM3=0DDH CCAPM4=0DEH							
	-	ECOMn	CAPPn	CAPNn	MATn	TOGn	PWMm	ECCFn
Reset value	X	0	0	0	0	0	0	0

Symbol	Function
-	Not implemented, reserved for future use.[a]
ECOMn	Enable Comparator. ECOMn = 1 enables the comparator function.
CAPPn	Capture Positive, CAPPn = 1 enables positive edge capture.
CAPNn	Capture Negative, CAPNn = 1 enables negative edge capture.
MATn	Match. When MATn = 1, a match of the PCA counter with this module's compare/capture register causes the CCFn bit in CCON to be set, flagging an interrupt.
TOGn	Toggle. When TOGn = 1, a match of the PCA counter with this module's compare/capture register causes the CEXn pin to toggle.
PWMn	Pulse Width Modulation Mode. PWMn = 1 enables the CEXn pin to be used as a pulse width modulated output.
ECCFn	Enable CCF interrupt. Enables compare/capture flag CCFn in the CCON register to generate an interrupt.

a. User software should not write 1s to reserved bits. These bits may be used in future 8051 family products to invoke new features. In that case, the reset or inactive value of the new bit will be 0, and its active value will be 1. The value read from a reserved bit is indeterminate.

Table 29. PCA Module Modes (CCAPMn Registers)

ECOMn	CAPPn	CAPNn	MATn	TOGn	PWMm	ECCFn	Module Function
0	0	0	0	0	0	0	No Operation
X	1	0	0	0	0	X	16-bit capture by a positive-edge trigger on CEXn
X	0	1	0	0	0	X	16-bit capture by a negative trigger on CEXn
X	1	1	0	0	0	X	16-bit capture by a transition on CEXn
1	0	0	1	0	0	X	16-bit Software Timer / Compare mode.
1	0	0	1	1	0	X	16-bit High Speed Output
1	0	0	0	0	1	0	8-bit PWM
1	0	0	1	X	0	X	Watchdog Timer (module 4 only)

There are two additional registers associated with each of the PCA modules. They are CCAPnH and CCAPnL and these are the registers that store the 16-bit count when a capture occurs or a compare should occur. When a module is used in the PWM mode these registers are used to control the duty cycle of the output (See Table 30 & Table 31)

Table 30. CCAPnH: PCA Modules Capture/Compare Registers High

CCAPnH Address n = 0 - 4	CCAP0H=0FAH CCAP1H=0FBH CCAP2H=0FCH CCAP3H=0FDH CCAP4H=0FEH							
	7	6	5	4	3	2	1	0
Reset value	0	0	0	0	0	0	0	0

Table 31. CCAPnL: PCA Modules Capture/Compare Registers Low

CCAPnL Address n = 0 - 4	CCAP0L=0EAH CCAP1L=0EBH CCAP2L=0ECH CCAP3L=0EDH CCAP4L=0EEH							
	7	6	5	4	3	2	1	0
Reset value	0	0	0	0	0	0	0	0

Table 32. CH: PCA Counter High

CH Address 0F9H								
	7	6	5	4	3	2	1	0
Reset value	0	0	0	0	0	0	0	0

Table 33. CL: PCA Counter Low

CL Address 0E9H								
	7	6	5	4	3	2	1	0
Reset value	0	0	0	0	0	0	0	0

13.1. PCA Capture Mode

To use one of the PCA modules in the capture mode either one or both of the CCAPM bits CAPN and CAPP for that module must be set. The external CEX input for the module (on port 1) is sampled for a transition. When a valid transition occurs the PCA hardware loads the value of the PCA counter registers (CH and CL) into the module's capture registers (CCAPnL and CCAPnH). If the CCFn bit for the module in the CCON SFR and the ECCFn bit in the CCAPMn SFR are set then an interrupt will be generated (Refer to Figure 24).

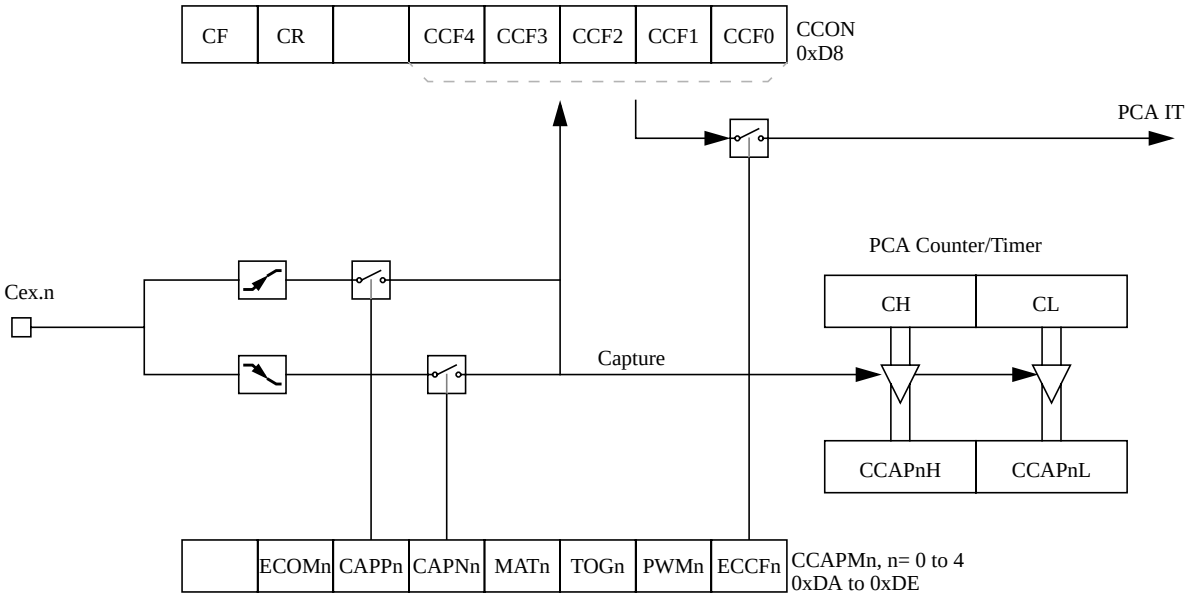
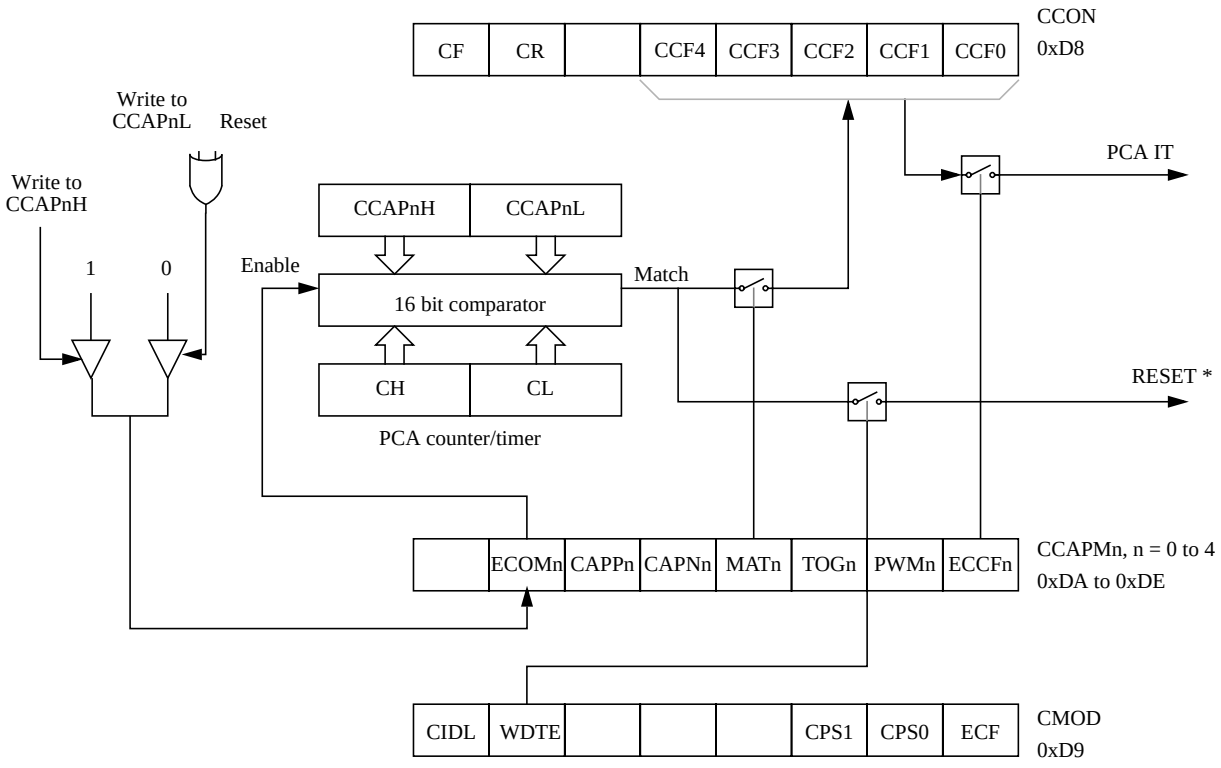


Figure 24. PCA Capture Mode

13.2. 16-bit Software Timer / Compare Mode

The PCA modules can be used as software timers by setting both the ECOM and MAT bits in the modules CCAPMn register. The PCA timer will be compared to the module's capture registers and when a match occurs an interrupt will occur if the CCFn (CCON SFR) and the ECCFn (CCAPMn SFR) bits for the module are both set (See Figure 25).



* Only for Module 4

Figure 25. PCA Compare Mode and PCA Watchdog Timer

Before enabling ECOM bit, CCAPnL and CCAPnH should be set with a non zero value, otherwise an unwanted match could happen. Writing to CCAPnH will set the ECOM bit.

Once ECOM set, writing CCAPnL will clear ECOM so that an unwanted match doesn't occur while modifying the compare value. Writing to CCAPnH will set ECOM. For this reason, user software should write CCAPnL first, and then CCAPnH. Of course, the ECOM bit can still be controlled by accessing to CCAPMn register.

13.3. High Speed Output Mode

In this mode the CEX output (on port 1) associated with the PCA module will toggle each time a match occurs between the PCA counter and the module's capture registers. To activate this mode the TOG, MAT, and ECOM bits in the module's CCAPMn SFR must be set (See Figure 26).

A prior write must be done to CCAPnL and CCAPnH before writing the ECOMn bit.

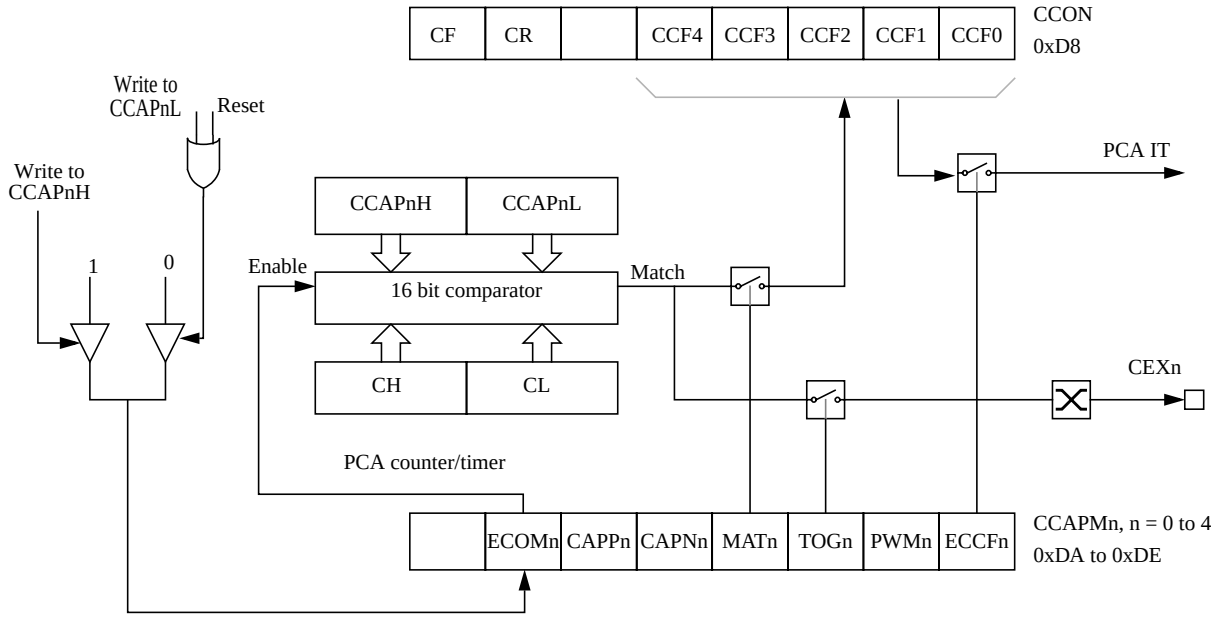


Figure 26. PCA High Speed Output Mode

Before enabling ECOM bit, CCAPnL and CCAPnH should be set with a non zero value, otherwise an unwanted match could happen.

Once ECOM set, writing CCAPnL will clear ECOM so that an unwanted match doesn't occur while modifying the compare value. Writing to CCAPnH will set ECOM. For this reason, user software should write CCAPnL first, and then CCAPnH. Of course, the ECOM bit can still be controlled by accessing to CCAPMn register.

13.4. Pulse Width Modulator Mode

All of the PCA modules can be used as PWM outputs. Figure 27 shows the PWM function. The frequency of the output depends on the source for the PCA timer. All of the modules will have the same frequency of output because they all share the PCA timer. The duty cycle of each module is independently variable using the module's capture register CCAPLn. When the value of the PCA CL SFR is less than the value in the module's CCAPLn

SFR the output will be low, when it is equal to or greater than the output will be high. When CL overflows from FF to 00, CCAPLn is reloaded with the value in CCAPHn. This allows updating the PWM without glitches. The PWM and ECOM bits in the module's CCAPMn register must be set to enable the PWM mode.

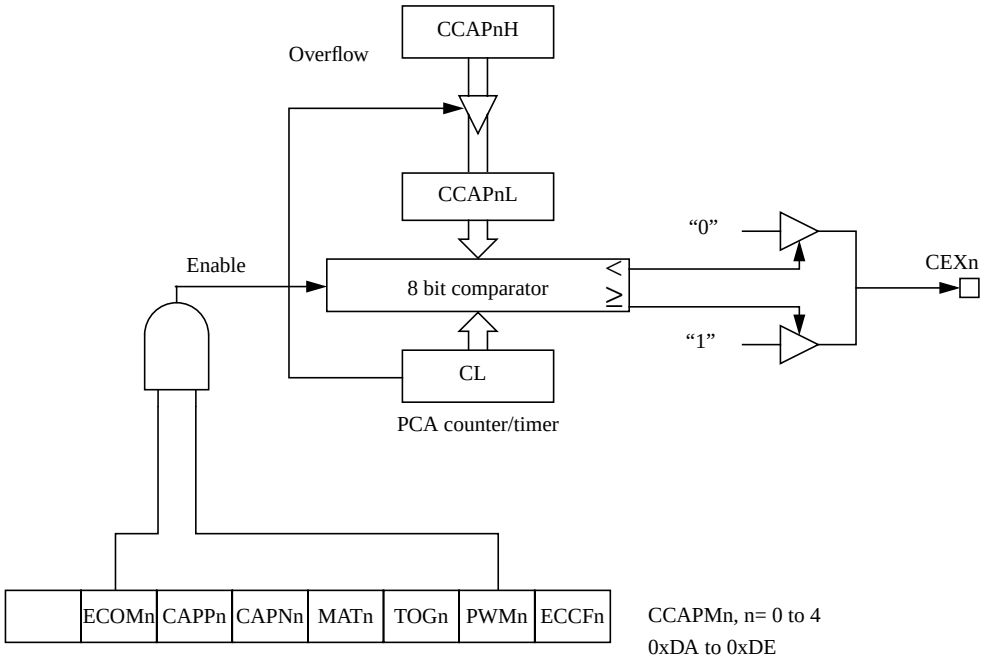


Figure 27. PCA PWM Mode

13.5. PCA Watchdog Timer

An on-board watchdog timer is available with the PCA to improve the reliability of the system without increasing chip count. Watchdog timers are useful for systems that are susceptible to noise, power glitches, or electrostatic discharge. Module 4 is the only PCA module that can be programmed as a watchdog. However, this module can still be used for other modes if the watchdog is not needed. Figure 25 shows a diagram of how the watchdog works. The user pre-loads a 16-bit value in the compare registers. Just like the other compare modes, this 16-bit value is compared to the PCA timer value. If a match is allowed to occur, an internal reset will be generated. This will not cause the RST pin to be driven high.

In order to hold off the reset, the user has three options:

- 1. periodically change the compare value so it will never match the PCA timer,
- 2. periodically change the PCA timer value so it will never match the compare values, or
- 3. disable the watchdog by clearing the WDTE bit before a match occurs and then re-enable it.

The first two options are more reliable because the watchdog timer is never disabled as in option #3. If the program counter ever goes astray, a match will eventually occur and cause an internal reset. The second option is also not recommended if other PCA modules are being used. Remember, the PCA timer is the time base for all modules; changing the time base for other modules would not be a good idea. Thus, in most applications the first solution is the best option.

This watchdog timer won't generate a reset out on the reset pin.

14. Analog-to-Digital Converter (ADC)

14.1. Introduction

This section describes the on-chip 10 bit analog-to-digital converter of the T80C5112. Eight ADC channels are available for sampling of the external sources AN0 to AN7. An analog multiplexer allows the single ADC converter to select one from the 8 ADC channels as ADC input voltage (ADCIN). ADCIN is converted by the 10 bit-cascaded potentiometric ADC.

Three kind of conversion are available:

- Standard conversion (7-8 bits).
- Precision conversion (8-9 bits).
- Accurate conversion (10 bits).

For the precision conversion, set bits PSIDLE and ADSST in ADCON register to start the conversion. The chip is in a idle mode, the CPU doesn't run but the peripherals are always running. This mode allows digital noise to be lower, to ensure precise conversion.

For the accurate conversion, set bits QUIETM and ADSST in ADCON register to start the conversion. The chip is in a pseudo-idle mode, the AD is the only peripheral running. This mode allows digital noise to be as low as possible, to ensure high precision conversion.

For these modes it is necessary to work with end of conversion interrupt, which is the only way to wake up the chip.

If another interrupt occurs during the precision conversion, it will be treated only after this conversion is ended.

14.2. Features

- 8 channels with multiplexed inputs
- 10-bit cascaded potentiometric ADC
- Conversion time 40 micro-seconds
- Zero Error (offset) +/- 2 LSB max
- External Positive Reference Voltage Range 2.4 to Vcc
- Internal Positive Reference Voltage 2.4 Volt. If Vref is used as output, the load must be higher than 18 kOhm.
- ADCIN Range 0 to Vcc
- Integral non-linearity typical 1 LSB, max. 2 LSB
- Differential non-linearity typical 0.5 LSB, max. 1 LSB
- Conversion Complete Flag or Conversion Complete Interrupt
- Selected ADC Clock

14.3. ADC I/O Functions

AINx are general I/O that are shared with the ADC channels. The channel select bit in ADCF register define which ADC channel pin will be used as ADCIN. The remaining ADC channels pins can be used as general purpose I/O or as the alternate function that is available. Writes to the port register which aren't selected by the ADCF will not have any effect.

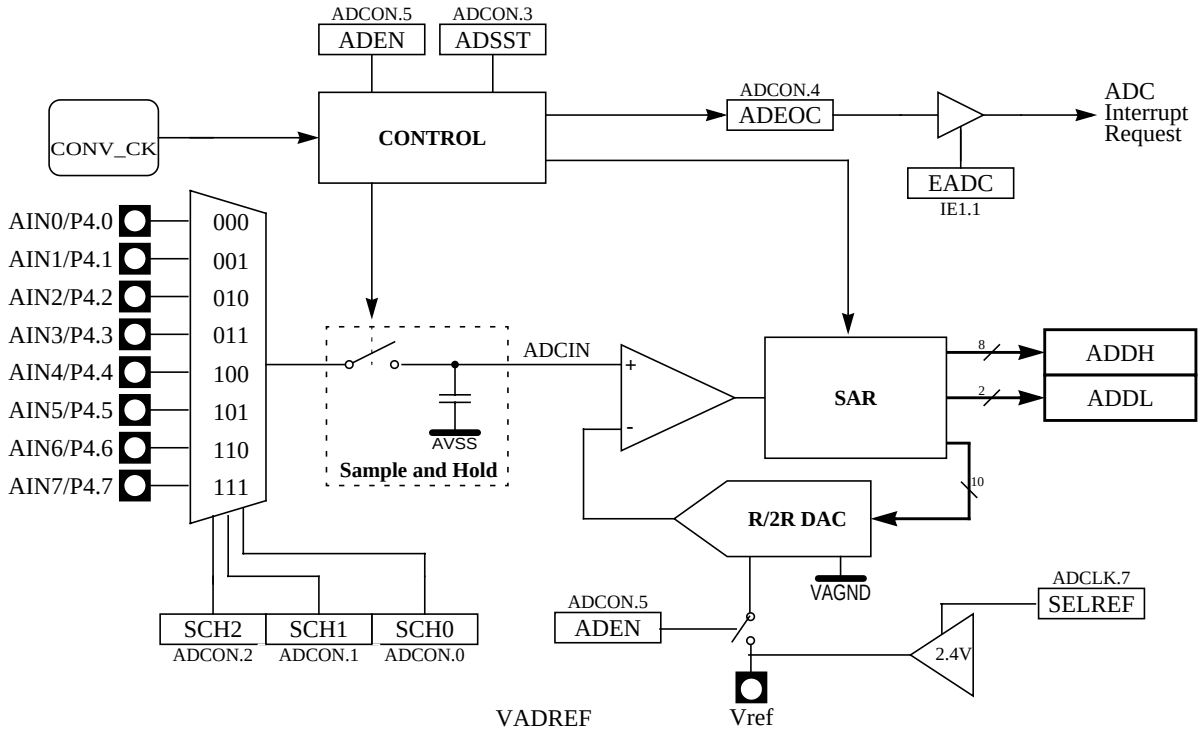


Figure 28. ADC Description

Figure 29 shows the timing diagram of a complete conversion. For simplicity, the figure depicts the waveforms in idealized form and do not provide precise timing information. For ADC characteristics and timing parameters refer to the Section “AC Characteristics” of the T80C5112 datasheet.

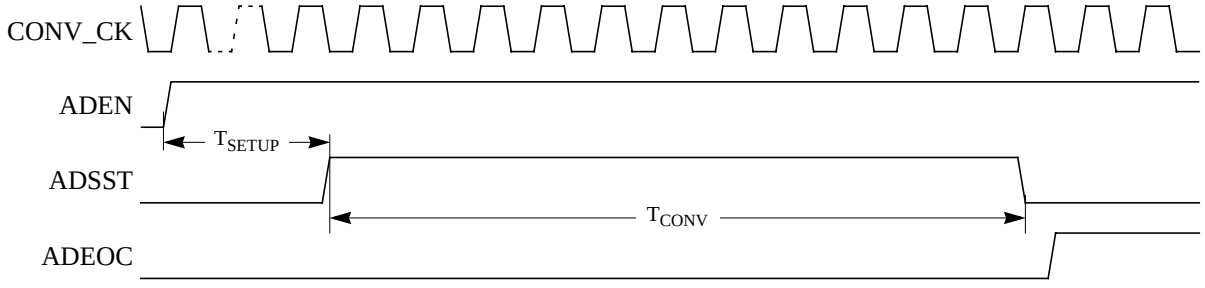


Figure 29. Timing Diagram

NOTE:
Tsetup = 4 us

14.4. ADC Converter Operation

A start of single A/D conversion is triggered by setting bit ADSST (ADCON.3).

The busy flag ADSST(ADCON.3) remains set as long as an A/D conversion is running. After completion of the A/D conversion, it is cleared by hardware. When a conversion is running, this flag can be read only, a write has no effect.

The end-of-conversion flag ADEOC (ADCON.4) is set when the value of conversion is available in ADDH and ADDL, it is cleared by software. If the bit EADC (IE1.1) is set, an interrupt occur when flag ADEOC is set (see Figure 31). Clear this flag for re-arming the interrupt.

The bits SCH0 to SCH2 in ADCON register are used for the analog input channel selection.

Before starting normal power reduction modes the ADC conversion has to be completed.

Table 34. Selected Analog input

SCH2	SCH1	SCH0	Selected Analog input
0	0	0	AN0
0	0	1	AN1
0	1	0	AN2
0	1	1	AN3
1	0	0	AN4
1	0	1	AN5
1	1	0	AN6
1	1	1	AN7

14.5. Voltage Conversion

When the ADCIN is equals to VAREF the ADC converts the signal to 3FFh (full scale). If the input voltage equals VAGND, the ADC converts it to 000h. Input voltage between VAREF and VAGND are a straight-line linear conversion. All other voltages will result in 3FFh if greater than VAREF and 000h if less than VAGND.

Note that ADCIN should not exceed VAREF absolute maximum range.

14.6. Clock Selection

The maximum clock frequency for ADC (CONV_CK for Conversion Clock) is defined in the AC characteristics section. A prescaler is featured (ADCCLK) to generate the CONV_CK clock from the oscillator frequency.

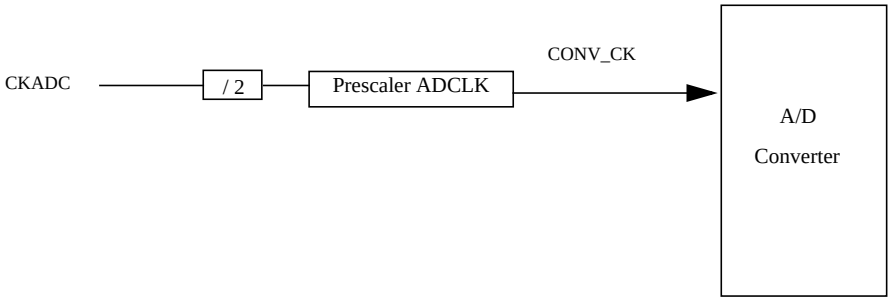


Figure 30. A/D Converter clock

14.7. ADC Standby Mode

When the ADC is not used, it is possible to set it in standby mode by clearing bit ADEN in ADCON register.

In this mode the power dissipation is about 1uW.

14.8. Voltage referencee

The voltage reference can be either internal or external.

As input, the Vref pin is used to enter the voltage reference for the A/D conversion.

When the voltage reference is active, the Vref pin is an output. This voltage can be used for the A/D and for any other application requiring a voltage independant from the power supply. Voltage typical value is 2.4 volt and the load must greater than 18 kOms.

14.9. IT ADC management

An interrupt end-of-conversion will occurs when the bit ADEOC is actived and the bit EADC is set. For re-arming the interrupt the bit ADEOC must be cleared by software.

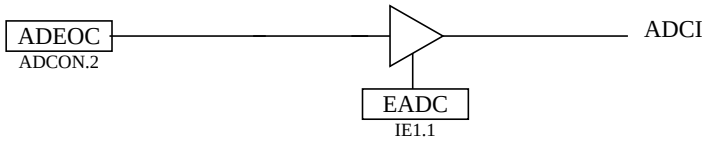


Figure 31. ADC interrupt structure

14.10. Registers

Table 35. ADCON Register

ADCON (S:F3h)
ADC Control Register

7	6	5	4	3	2	1	0
QUIETM	**PSIDLE**	**ADEN**	**ADEOC**	**ADSST**	**SCH2**	**SCH1**	**SCH0**

Bit Number	Bit Mnemonic	Description
7	QUIETM	**Pseudo Idle mode (best precision)** Set to put in quiet mode during conversion. Cleared by hardware after completion of the conversion.
6	PSIDLE	**Pseudo Idle mode (good precision)** Set to put in idle mode during conversion. Cleared by hardware after completion of the conversion.

Bit Number	Bit Mnemonic	Description
5	ADEN	**Enable/Standby Mode** Set to enable ADC. Clear for Standby mode (power dissipation 1 uW).
4	ADEOC	**End Of Conversion** Set by hardware when ADC result is ready to be read. This flag can generate an interrupt. Must be cleared by software.
3	ADSST	**Start and Status** Set to start an A/D conversion. Cleared by hardware after completion of the conversion.
2-0	SCH2:0	**Selection of channel to convert** see Table 34.

Reset Value=X000 0000b

Table 36. ADCLK Register

ADCLK (S:F2h)
ADC Clock Prescaler

7	6	5	4	3	2	1	0
SELREF	**PRS 6**	**PRS 5**	**PRS 4**	**PRS 3**	**PRS 2**	**PRS 1**	**PRS 0**

Bit Number	Bit Mnemonic	Description
7	SELREF	**Selection and activation of the internal 2.4V voltage reference** Set to enable the internal voltage reference. Clear to disable the internal voltage reference.
6-0	PRS6:0	**Clock Prescaler** $f_{CONV\_CK} = \mathbf{f}_{CkADC} / (2 * PRS)$ if PRS=0, $f_{CONV\_CK} = \mathbf{f}_{CkADC} / 256$

Reset Value: 0000 0000b

Table 37. ADDH Register

ADDH (S:F5h Read Only)
ADC Data High byte register

7	6	5	4	3	2	1	0
ADAT 9	**ADAT 8**	**ADAT 7**	**ADAT 6**	**ADAT 5**	**ADAT 4**	**ADAT 3**	**ADAT 2**

Bit Number	Bit Mnemonic	Description
7-0	ADAT9:2	**ADC result** bits 9-2

Read only register

Reset Value: 00h

Table 38. ADDL Register

ADDL (S:F4h Read Only)
ADC Data Low byte register

7	6	5	4	3	2	1	0
-	-	-	-	-	-	**ADAT 1**	**ADAT 0**

Bit Number	Bit Mnemonic	Description
7-6	-	**Reserved** The value read from these bits are indeterminate. Do not set these bits.
1-0	ADAT1:0	**ADC result** bits 1-0

Read only register

Reset Value: xxxx xx00b

Table 39. ADCF Register

ADCF (S:F6h)
ADC Input Select Register

7	6	5	4	3	2	1	0
SEL7	**SEL6**	**SEL5**	**SEL4**	**SEL3**	**SEL2**	**SEL1**	**SEL0**

Bit Number	Bit Mnemonic	Description
7-0	SEL7-0	**Select Input 7-0** Set to select bit 7-0 as possible input for A/D Cleared to leave this bit free for other function

Reset Value=0000 0000b

15. Interrupt System

The T80C5112 has a total of 8 interrupt vectors: two external interrupts ($\overline{INT0}$ and $\overline{INT1}$), two timer interrupts (timers 0, 1), serial port interrupt, PCA, SPI and A/D. These interrupts are shown in Figure 32..

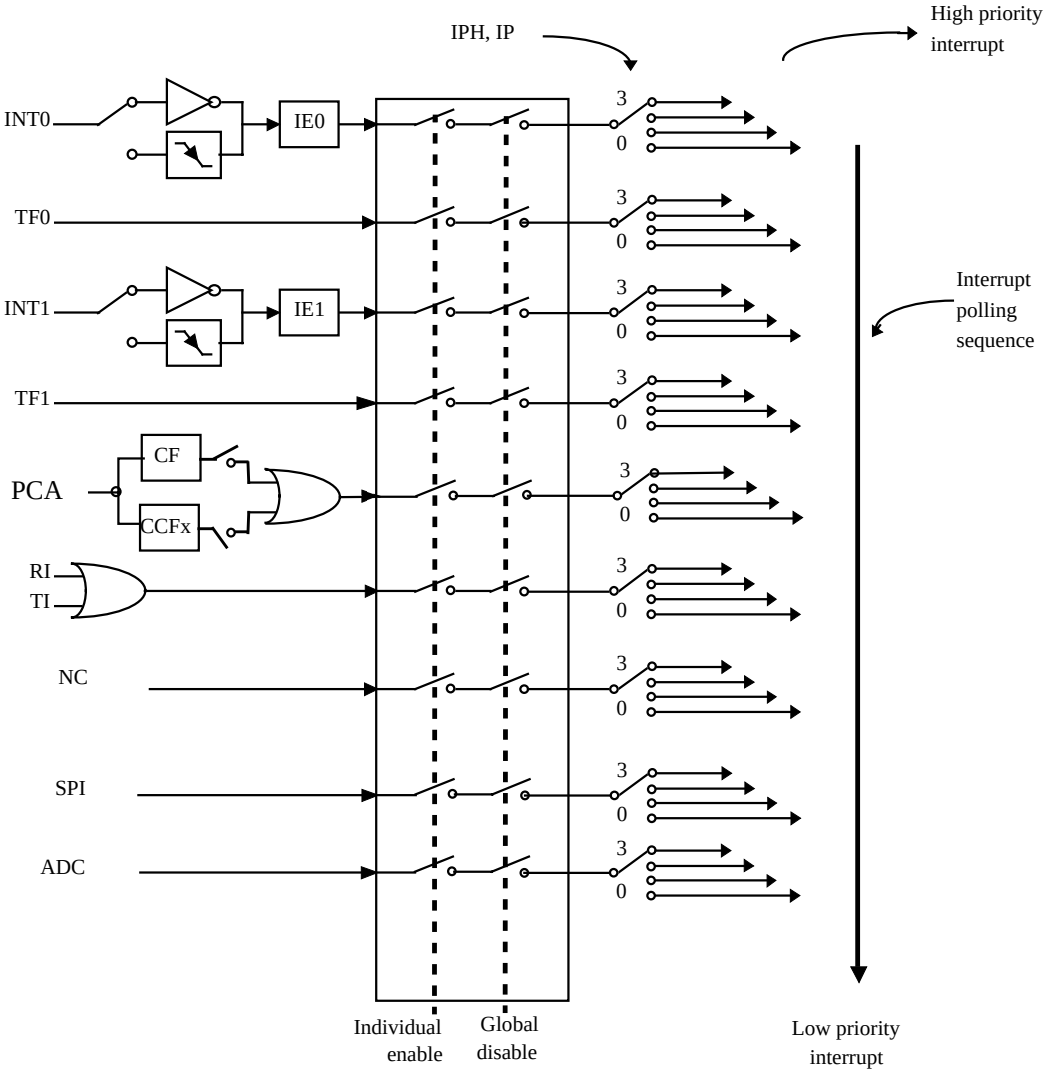


Figure 32. Interrupt Control System

Each of the interrupt sources can be individually enabled or disabled by setting or clearing a bit in the Interrupt Enable register (See Table 42.). This register also contains a global disable bit, which must be cleared to disable all interrupts at once.

Each interrupt source can also be individually programmed to one of four priority levels by setting or clearing a bit in the Interrupt Priority register (See Table 44.) and in the Interrupt Priority High register (See Table 46.). Table 40. shows the bit values and priority levels associated with each combination.

Table 40. Priority bit level values

IPH.x	IP.x	Interrupt Level Priority
0	0	0 (Lowest)
0	1	1
1	0	2
1	1	3 (Highest)

A low-priority interrupt can be interrupted by a high priority interrupt, but not by another low-priority interrupt. A high-priority interrupt can't be interrupted by any other interrupt source.

If two interrupt requests of different priority levels are received simultaneously, the request of higher priority level is serviced. If interrupt requests of the same priority level are received simultaneously, an internal polling sequence determines which request is serviced. Thus within each priority level there is a second priority structure determined by the polling sequence.

Table 41. Address vectors

Interrupt Name	Interrupt Address Vector	Priority Number
external interrupt (INT0)	0003h	1
Timer0 (TF0)	000Bh	2
external interrupt (INT1)	0013h	3
Timer1 (TF1)	001Bh	4
PCA (CF or CCFn)	0033h	5
UART (RI or TI)	0023h	6
SPI	004Bh	8
ADC	0043h	9

Table 42. IE Register

IE - Interrupt Enable Register (A8h)

7	6	5	4	3	2	1	0
EA	EC	-	ES	ET1	EX1	ET0	EX0

Bit Number	Bit Mnemonic	Description
7	EA	**Enable All interrupt bit** Clear to disable all interrupts. Set to enable all interrupts. If EA=1, each interrupt source is individually enabled or disabled by setting or clearing its interrupt enable bit.
6	EC	**PCA Interrupt Enable** Clear to disable the the PCA interrupt. Set to enable the the PCA interrupt.
5	-	**Reserved** The value read from this bit is indeterminate. Do not set this bit.
4	ES	**Serial port Enable bit** Clear to disable serial port interrupt. Set to enable serial port interrupt.
3	ET1	**Timer 1 overflow interrupt Enable bit** Clear to disable timer 1 overflow interrupt. Set to enable timer 1 overflow interrupt.
2	EX1	**External interrupt 1 Enable bit** Clear to disable external interrupt 1. Set to enable external interrupt 1.
1	ET0	**Timer 0 overflow interrupt Enable bit** Clear to disable timer 0 overflow interrupt. Set to enable timer 0 overflow interrupt.
0	EX0	**External interrupt 0 Enable bit** Clear to disable external interrupt 0. Set to enable external interrupt 0.

Reset Value = 00X0 0000b
Bit addressable

Table 43. IE1 Register

IE1 (S:C0h)
Interrupt Enable Register

7	6	5	4	3	2	1	0
-	-	-	-	-	**ESPI**	**EADC**	-

Bit Number	Bit Mnemonic	Description
7	-	**Reserved** The value read from this bit is indeterminate. Do not set this bit.
6	-	**Reserved** The value read from this bit is indeterminate. Do not set this bit.
5	-	**Reserved** The value read from this bit is indeterminate. Do not set this bit.
4	-	**Reserved** The value read from this bit is indeterminate. Do not set this bit.
3	-	**Reserved** The value read from this bit is indeterminate. Do not set this bit.
2	ESPI	**SPI Interrupt Enable bit** Clear to disable the SPI interrupt. Set to enable the SPI interrupt.
1	EADC	**A/D Interrupt Enable bit** Clear to disable the ADC interrupt. Set to enable the ADC interrupt.
0	-	**Reserved** The value read from this bit is indeterminate. Do not set this bit.

Reset Value = XXXX X00Xb
No Bit addressable

Table 44. IPL0 Register

IPL0 - Interrupt Priority Register (B8h)

7	6	5	4	3	2	1	0
-	PPC	-	PS	PT1	PX1	PT0	PX0

Bit Number	Bit Mnemonic	Description
7	-	**Reserved** The value read from this bit is indeterminate. Do not set this bit.
6	PPCL	**PCA Counter Interrupt Priority bit** Refer to PPCH for priority level
5	-	**Reserved** The value read from this bit is indeterminate. Do not set this bit.
4	PSL	**Serial port Priority bit** Refer to PSH for priority level.
3	PT1L	**Timer 1 overflow interrupt Priority bit** Refer to PT1H for priority level.
2	PX1L	**External interrupt 1 Priority bit** Refer to PX1H for priority level.
1	PT0L	**Timer 0 overflow interrupt Priority bit** Refer to PT0H for priority level.
0	PX0L	**External interrupt 0 Priority bit** Refer to PX0H for priority level.

Reset Value = X0X0 0000b
Bit addressable.

Table 45. IPL1 Register

IPL1 - Interrupt Priority Low Register 1 (S:B2h)

7	6	5	4	3	2	1	0
-	-	-	-	-	PSPI	PADC	-

Bit Number	Bit Mnemonic	Description
7		
6	-	**Reserved** The value read from this bit is indeterminate. Do not set this bit.
5	-	**Reserved** The value read from this bit is indeterminate. Do not set this bit.
4	-	**Reserved** The value read from this bit is indeterminate. Do not set this bit.
3	-	**Reserved** The value read from this bit is indeterminate. Do not set this bit.
2	PSPI	**SPI Interrupt Priority level less significant bit.** Refer to PSPIH for priority level.
1	PADC	**ADC Interrupt Priority level less significant bit.** Refer to PADCH for priority level.
0	-	**Reserved** The value read from this bit is indeterminate. Do not set this bit.

Reset Value = XXXX X00Xb
Not Bit addressable.

Table 46. IPH0 Register

IPH0 - Interrupt Priority High Register (B7h)

7	6	5	4	3	2	1	0
-	PPCH	-	PSH	PT1H	PX1H	PT0H	PX0H

Bit Number	Bit Mnemonic	Description
7	-	**Reserved** The value read from this bit is indeterminate. Do not set this bit.
6	PPCH	**PCA Counter Interrupt Priority level most significant bit** PPCH PPC Priority level 0 0 Lowest 0 1 1 0 1 1 Highest priority
5	-	**Reserved** The value read from this bit is indeterminate. Do not set this bit.
4	PSH	**Serial port Priority High bit** PSH PS Priority Level 0 0 Lowest 0 1 1 0 1 1 Highest
3	PT1H	**Timer 1 overflow interrupt Priority High bit** PT1H PT1 Priority Level 0 0 Lowest 0 1 1 0 1 1 Highest
2	PX1H	**External interrupt 1 Priority High bit** PX1H PX1 Priority Level 0 0 Lowest 0 1 1 0 1 1 Highest
1	PT0H	**Timer 0 overflow interrupt Priority High bit** PT0H PT0 Priority Level 0 0 Lowest 0 1 1 0 1 1 Highest
0	PX0H	**External interrupt 0 Priority High bit** PX0H PX0 Priority Level 0 0 Lowest 0 1 1 0 1 1 Highest

Reset Value = X0X0 0000b
Not bit addressable

Table 47. IPH1 Register

IPH1 - Interrupt Priority High Register 1 (B3h)

7	6	5	4	3	2	1	0
-	-	-	-	-	PSPIH	PADCH	-

Bit Number	Bit Mnemonic	Description
7		
6	-	**Reserved** The value read from this bit is indeterminate. Do not set this bit.
5	-	**Reserved** The value read from this bit is indeterminate. Do not set this bit.
4	-	**Reserved** The value read from this bit is indeterminate. Do not set this bit.
3	-	**Reserved** The value read from this bit is indeterminate. Do not set this bit.
2	PSPIH	**SPI Interrupt Priority level most significant bit** PSPIH PSPI Priority level 0 0Lowest 0 1 1 0 1 1Highest
1	PADCH	**ADC Interrupt Priority level most significant bit** PADCH PADC Priority level 0 0Lowest 0 1 1 0 1 1Highest
0	-	**Reserved** The value read from this bit is indeterminate. Do not set this bit.

Reset Value = XXXX X00Xb
Not bit addressable

16. ROM

16.1. ROM Structure

The T80C5112 ROM memory is divided in three different arrays:

- the code array: . . . . . .8Kbytes.
- the encryption array:. . . . . 64 bytes.
- the signature array:. . . . . 4 bytes.

16.2. ROM Lock System

The program Lock system, when programmed, protects the on-chip program against software piracy.

16.2.1. Encryption Array

Within the ROM array are 64 bytes of encryption array. Every time a byte is addressed during program verify, 6 address lines are used to select a byte of the encryption array. This byte is then exclusive-NOR'ed (XNOR) with the code byte, creating an encrypted verify byte. The algorithm, with the encryption array in the unprogrammed state, will return the code in its original, unmodified form.

When using the encryption array, one important factor needs to be considered. If a byte has the value FFh, verifying the byte will produce the encryption byte value. If a large block (>64 bytes) of code is left unprogrammed, a verification routine will display the content of the encryption array. For this reason all the unused code bytes should be programmed with random values.

16.2.2. Program Lock Bits

The lock bits when programmed according to Table 41. will provide different level of protection for the on-chip code and data.

Table 48. Program Lock bits

Program Lock Bits			Protection description
Security level	LB1	LB2	
1	U	U	No program lock features enabled. Code verify will still be encrypted by the encryption array if programmed. MOVC instruction executed from external program memory returns non encrypted data.
2	P	U	MOVC instruction executed from external program memory are disabled from fetching code bytes from internal memory, $\overline{EA}$ is sampled and latched on reset.
3	U	P	Same as 2, also verify is disabled This security level is available because ROM integrity will be verified thanks to another method.

U: unprogrammed
P: programmed

16.2.3. Signature bytes

The T80C5112 contains 4 factory programmed signatures bytes. To read these bytes, perform the process described in Section "Signature bytes", page 75.

16.2.4. Verify Algorithm

Refer to Section "Verify algorithm", page 76.

17. EPROM

17.1. EPROM Structure

The T80C5112 EPROM is divided into two different arrays:

- the code array: . . . . . 8Kbytes.
- the encryption array: . . . . . 64 bytes.

In addition a third non programmable array is implemented:

- the signature array: . . . . . 4 bytes.

17.2. EPROM Lock System

The program Lock system, when programmed, protects the on-chip program against software piracy.

17.2.1. Encryption Array

Within the EPROM array are 64 bytes of encryption array that are initially unprogrammed (all FF's). Every time a byte is addressed during program verify, 6 address lines are used to select a byte of the encryption array. This byte is then exclusive-NOR'ed (XNOR) with the code byte, creating an encrypted verify byte. The algorithm, with the encryption array in the unprogrammed state, will return the code in its original, unmodified form.

When using the encryption array, one important factor needs to be considered. If a byte has the value FFh, verifying the byte will produce the encryption byte value. If a large block (>64 bytes) of code is left unprogrammed, a verification routine will display the content of the encryption array. For this reason all the unused code bytes should be programmed with random values.

17.2.2. Program Lock Bits

The three lock bits, when programmed according to Table 49., will provide different level of protection for the on-chip code and data.

Table 49. Program Lock bits

Program Lock Bits				Protection description
Security level	LB1	LB2	LB3	
1	U	U	U	No program lock features enabled. Code verify will still be encrypted by the encryption array if programmed. MOVC instruction executed from external program memory returns non encrypted data.
2	P	U	U	MOVC instruction executed from external program memory are disabled from fetching code bytes from internal memory, $\overline{EA}$ is sampled and latched on reset , and further programming of the EPROM is disabled..
3	U	P	U	Same as 2, also verify is disabled This security level is available because ROM integrity will be verified thanks to another method..
4	U	U	P	Same as 3, also external execution is disabled.

U: unprogrammed,
P: programmed

WARNING: Security level 2 and higher should only be programmed after EPROM verification.

17.2.3. Signature bytes

The T80C5112 contains 4 factory programmed signatures bytes. To read these bytes, perform the process described in Section 17.5.1.

17.3. EPROM Programming

17.3.1. Set-up modes

In order to program and verify the EPROM or to read the signature bytes, the T80C5112 is placed in specific set-up modes (See Figure 33.).

Control and program signals must be held at the levels indicated in Table 50.

17.3.2. Definition of terms

Address Lines: P1.0-P1.7, P2.0-P2.5, P3.4, P3.5 respectively for A0-A15 (P2.5 (A13) for RB, P3.4 (A14) for RC, P3.5 (A15) for RD)

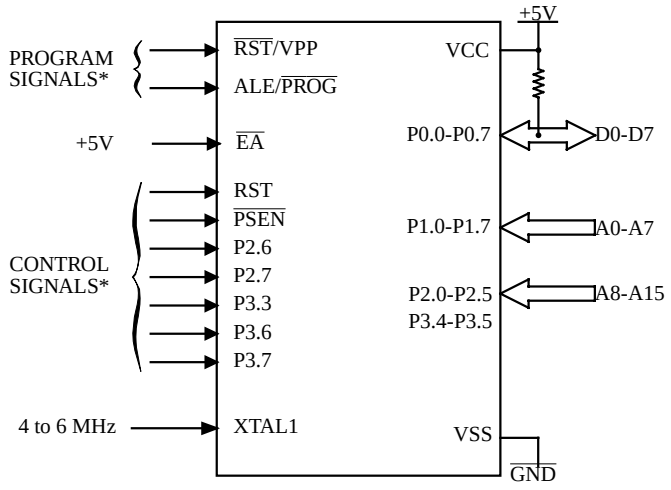
Data Lines: P0.0-P0.7 for D0-D7

Control Signals: RST, $\overline{\text{PSEN}}$, P2.6, P2.7, P3.3, P3.6, P3.7.

Program Signals: ALE/$\overline{\text{PROG}}$, $\overline{\text{RST}}$/VPP.

Table 50. EPROM Set-Up Modes

Mode	RST	$\overline{\text{PSEN}}$	ALE/$\overline{\text{PROG}}$	$\overline{\text{RST}}$/VPP	P2.6	P2.7	P3.3	P3.6	P3.7
Program Code data	1	0	⎍	12.75V	0	1	1	1	1
Verify Code data	1	0	1	1	0	⎍	0	1	1
Program Encryption Array Address 0-3Fh	1	0	⎍	12.75V	0	1	1	0	1
Read Signature Bytes	1	0	1	1	0	⎍	0	0	0
Program Lock bit 1	1	0	⎍	12.75V	1	1	1	1	1
Program Lock bit 2	1	0	⎍	12.75V	1	1	1	0	0
Program Lock bit 3	1	0	⎍	12.75V	1	0	1	1	0



* See Table 49. for proper value on these inputs

Figure 33. Set-Up Modes Configuration

17.3.3. Programming Algorithm

The Improved Quick Pulse algorithm is based on the Quick Pulse algorithm and decreases the number of pulses applied during byte programming from 25 to 1.

To program the T80C5112 the following sequence must be exercised:

- Step 1: Activate the combination of control signals.
- Step 2: Input the valid address on the address lines.
- Step 3: Input the appropriate data on the data lines.
- Step 4: Raise RST/VPP from VCC to VPP (typical 12.75V).
- Step 5: Pulse ALE/PROG once.
- Step 6: Lower RST/VPP from VPP to VCC

Repeat step 2 through 6 changing the address and data for the entire array or until the end of the object file is reached (See Figure 34).

17.3.4. Verify algorithm

Code array verify must be done after each byte or block of bytes is programmed. In either case, a complete verify of the programmed array will ensure reliable programming of the T80C5112.

P 2.7 is used to enable data output.

To verify the T80C5112 code the following sequence must be exercised:

- Step 1: Activate the combination of program and control signals.
- Step 2: Input the valid address on the address lines.
- Step 3: Read data on the data lines.

Repeat step 2 through 3 changing the address for the entire array verification (See Figure 34).

The encryption array cannot be directly verified. Verification of the encryption array is done by observing that the code array is well encrypted.

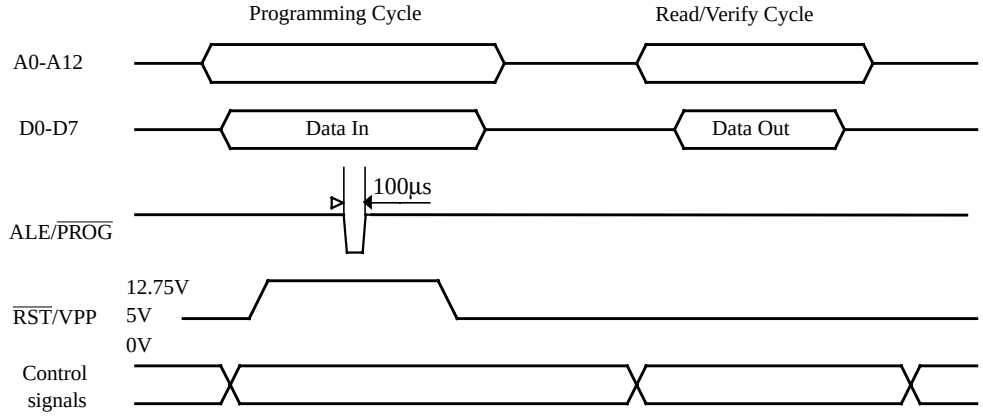


Figure 34. Programming and Verification Signal's Waveform

17.4. EPROM Erasure (Windowed Packages Only)

Erasing the EPROM erases the code array, the encryption array and the lock bits returning the parts to full functionality.

Erasure leaves all the EPROM cells in a 1's state (FF).

17.4.1. Erasure Characteristics

The recommended erasure procedure is exposure to ultraviolet light (at 2537 Å) to an integrated dose at least 15 W-sec/cm^2. Exposing the EPROM to an ultraviolet lamp of 12,000 µW/cm^2 rating for 30 minutes, at a distance of about 25 mm, should be sufficient. An exposure of 1 hour is recommended with most of standard erasers.

Erasure of the EPROM begins to occur when the chip is exposed to light with wavelength shorter than approximately 4,000 Å. Since sunlight and fluorescent lighting have wavelengths in this range, exposure to these light sources over an extended time (about 1 week in sunlight, or 3 years in room-level fluorescent lighting) could cause inadvertent erasure. If an application subjects the device to this type of exposure, it is suggested that an opaque label be placed over the window.

17.5. Signature Bytes

17.5.1. Signature bytes content

The T80C5112 has four signature bytes in location 30h, 31h, 60h and 61h. To read these bytes follow the procedure for EPROM verify but activate the control lines provided in xxxx for Read Signature Bytes. Table 51. shows the content of the signature byte for the T80C5112.

Table 51. Signature Bytes Content

Location	Contents	Comment
30h	58h	Manufacturer Code: Atmel Wireless & Microcontrollers
31h	57h	Family Code: C51 X2
60h	2Dh	Product name: T80C5112 8K ROM version
60h	ADh	Product name: T80C5112 8K OTP version
61h	EFh	Product revision number : T80C5112 Rev.0

18. Electrical Characteristics

18.1. Absolute Maximum Ratings (1)

Ambiant Temperature Under Bias:
C = commercial 0°C to 70°C
I = industrial -40°C to 85°C
Storage Temperature -65°C to + 150°C
Voltage on V_{CC} to V_{SS}-0.5 V to + 7 V
Voltage on V_{PP} to V_{SS}-0.5 V to + 13 V
Voltage on Any Pin to V_{SS}-0.5 V to V_{CC} + 0.5 V
Power Dissipation1 W(2)

NOTES

1. Stresses at or above those listed under " Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions may affect device reliability.

2. This value is based on the maximum allowable die temperature and the thermal resistance of the package.

18.2. Power consumption measurement

Since the introduction of the first C51 devices, every manufacturer made operating Icc measurements under reset, which made sense for the designs were the CPU was running under reset. In our new devices, the CPU is no more active during reset, so the power consumption is very low but is not really representative of what will happen in the customer system. That's why, while keeping measurements under Reset, we present a new way to measure the operating Icc:

Using an internal test ROM, the following code is executed:

Label: SJMP Label (80 FE)

Ports 1, 3, 4 are disconnected, RST = Vcc, XTAL2 is not connected and XTAL1 is driven by the clock.

This is much more representative of the real operating Icc.

18.3. DC Parameters for Standard Voltage

T_A = 0°C to +70°C; V_{SS} = 0 V; V_{CC} = 5 V ± 10%; F = 0 to 40 MHz.
T_A = -40°C to +85°C; V_{SS} = 0 V; V_{CC} = 5 V ± 10%; F = 0 to 40 MHz.

Table 52. DC Parameters in Standard Voltage

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
V_{IL}	Input Low Voltage	-0.5		0.2 V_{CC} - 0.1	V	
V_{IH}	Input High Voltage except XTAL1, RST	0.2 V_{CC} + 0.9		V_{CC} + 0.5	V	
V_{IH1}	Input High Voltage, XTAL1, RST	0.7 V_{CC}		V_{CC} + 0.5	V	
V_{OL}	Output Low Voltage, ports 1, 2, 3, 4.			0.3 0.45 1.0	V V V	I_{OL} = 100 µA I_{OL} = 1.6 mA I_{OL} = 3.5 mA
V_{OL1}	Output Low Voltage, port 0, ALE, PSEN(6)			0.3 0.45 1.0	V V V	I_{OL} = 200 µA I_{OL} = 3.2 mA I_{OL} =7.0 mA
V_{OH}	Output High Voltage, ports 1, 2, 3, 4.(6)	V_{CC} - 0.3 V_{CC} - 0.7 V_{CC} - 1.5			V V V	I_{OH} = -10 µA I_{OH} = -30 µA I_{OH} = -60 µA V_{CC} = 5 V ± 10%
V_{OH2}	Output High Voltage, ports 1, 3, 4.(6) mode Push pull	V_{CC} - 0.3 V_{CC} - 0.7 V_{CC} - 1.5			V V V	I_{OH} = -100 µA I_{OH} = -1.6 mA I_{OH} = -3.2 mA V_{CC} = 5 V ± 10%
V_{OH1}	Output High Voltage, ports 0, ALE, PSEN(6)	V_{CC} - 0.3 V_{CC} - 0.7 V_{CC} - 1.5			V V V	I_{OH} = -200 µA I_{OH} = -3.2 mA I_{OH} = -7.0 mA V_{CC} = 5 V ± 10%
R_{RST}	RST Pulldown Resistor	50	90 (5)	200	kΩ	
I_{IL}	Logical 0 Input Current ports 1, 2, 3 and 4			-50	µA	Vin = 0.45 V,
I_{LI}	Input Leakage Current			±10	µA	0.45 V < Vin < V_{CC}
I_{TL}	Logical 1 to 0 Transition Current, ports 1, 2, 3, 4			-650	µA	Vin = 2.0 V
C_{IO}	Capacitance of I/O Buffer			10	pF	Fc = 1 MHz T_A = 25°C
I_{PD}	Power Down Current	to be confirmed	20 (5)	50	µA	2.0 V < V_{CC} < 5.5 V(3)
I_{CC} under RESET	Power Supply Current Maximum values, X1 mode: (7)		to be confirmed	3+ 0.4 Freq (MHz) @12MHz 5.8 @16MHz 7.4	mA	*V_{CC} = 5.5 V(1)*
I_{CC} operating	Power Supply Current Maximum values, X1 mode: (7)		to be confirmed	3 + 0.6 Freq (MHz) @12MHz 10.2 @16MHz 12.6	mA	V_{CC} = 5.5 V(8)
I_{CC} idle	Power Supply Current Maximum values, X1 mode: (7)		to be confirmed	3+0.3 Freq (MHz) @12MHz 3.9 @16MHz 5.1	mA	V_{CC} = 5.5 V(2)
V_{RET}	Supply voltage during power down mode	2			V	
V_{RST+}	High threshold of Power Fail Detect			2.54	V	
V_{RST}	Low threshold of Power Fail Detect	2.19			V	

18.4. DC Parameters for Low Voltage

TA = 0°C to +70°C; V_{SS} = 0 V; V_{CC} = 2.7 V to 5.5 V; F = 0 to 30 MHz.
TA = -40°C to +85°C; V_{SS} = 0 V; V_{CC} = 2.7 V to 5.5 V; F = 0 to 30 MHz.

Table 53. DC Parameters for Low Voltage

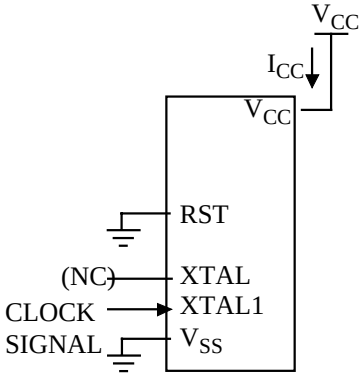
Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
V_{IL}	Input Low Voltage	-0.5		0.2 V_{CC} - 0.1	V	
V_{IH}	Input High Voltage except XTAL1, RST	0.2 V_{CC} + 0.9		V_{CC} + 0.5	V	
V_{IH1}	Input High Voltage, XTAL1, RST	0.7 V_{CC}		V_{CC} + 0.5	V	
V_{OL}	Output Low Voltage, ports 1, 2, 3, 4.			0.3 0.45 1.0	V V V	I_{OL} = I_{OL} = 0.8 mA I_{OL} =
V_{OL1}	Output Low Voltage, port 0, ALE, PSEN(6)			0.3 0.45 1.0	V V V	I_{OL} = 100 µA I_{OL} = 1.6 mA I_{OL} = 3.2 mA
V_{OH}	Output High Voltage, ports 1, 2, 3, 4.(6)	0.9 V_{CC} V_{CC} - 0.7 V_{CC} - 1.5			V V V	I_{OH} = -10 µA I_{OH} = I_{OH} =
V_{OH2}	Output High Voltage, ports 1, 3, 4.(6) mode Push pull	0.9V_{CC} V_{CC} - 0.7 V_{CC} - 1.5			V V V	I_{OH} = -100 µA I_{OH} = - mA I_{OH} =
V_{OH1}	Output High Voltage, ports 0, ALE, PSEN(6)	V_{CC} - 0.3 V_{CC} - 0.7 V_{CC} - 1.5			V V V	I_{OH} = -100 µA I_{OH} = -1.6 mA I_{OH} = -3.2 mA V_{CC} = 3V ± 10%
I_{IL}	Logical 0 Input Current ports 1, 2,3 and 4			-50	µA	Vin = 0.45 V
I_{LI}	Input Leakage Current			±10	µA	0.45 V < Vin < V_{CC}
I_{TL}	Logical 1 to 0 Transition Current, ports 1, 2, 3, 4			-650	µA	Vin = 2.0 V
R_{RST}	RST Pulldown Resistor	50	90 (5)	200	kΩ	
CIO	Capacitance of I/O Buffer			10	pF	Fc = 1 MHz TA = 25°C
I_{PD}	Power Down Current	to be confirmed	20 (5) 10 (5)	50 30	µA	V_{CC} = 2.0 V to 5.5 V(3) V_{CC} = 2.0 V to 3.3 V(3)
I_{CC} under RESET	Power Supply Current Maximum values, X1 mode: (7)		to be confirmed	1.5 + 0.2 Freq (MHz) @12MHz 3.4 @16MHz 4.2	mA	V_{CC} = 3.3 V(1)
I_{CC} operating	Power Supply Current Maximum values, X1 mode: (7)		to be confirmed	1.5 + 0.3 Freq (MHz) @12MHz 4.6 @16MHz 5.8	mA	V_{CC} = 3.3 V(8)
I_{CC} idle	Power Supply Current Maximum values, X1 mode: (7)		to be confirmed	1.5+0.15 Freq (MHz) @12MHz 2 @16MHz 2.6	mA	V_{CC} = 3.3 V(2)
V_{RET}	Supply voltage during power down mode	2			V	
V_{RST+}	High threshold of Power Fail Detect			2.54	V	
V_{RST}	Low threshold of Power Fail Detect	2.19			V	

NOTES

1. I_{CC} under reset is measured with all output pins disconnected; XTAL1 driven with T_{CLCH}, T_{CHCL} = 5 ns (see Figure 39.), V_{IL} = V_{SS} + 0.5 V, V_{IH} = V_{CC} - 0.5V; XTAL2 N.C.; Vpp = RST = V_{CC}. I_{CC} would be slightly higher if a crystal oscillator used.

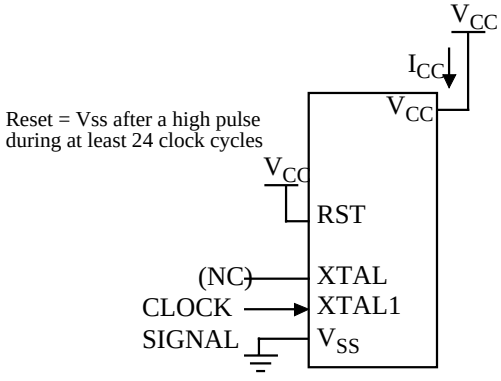
2. Idle I_{CC} is measured with all output pins disconnected; XTAL1 driven with T_{CLCH}, T_{CHCL} = 5 ns, V_{IL} = V_{SS} + 0.5 V, V_{IH} = V_{CC} - 0.5 V; XTAL2 N.C; Vpp = RST = V_{SS} (see Figure 37.).

3. *Power Down I_{CC} is measured with all output pins disconnected; Vpp = V_{SS}; XTAL2 NC.; RST = V_{SS} (see Figure 38.).*
4. *Not Applicable*
5. *Typicals are based on a limited number of samples and are not guaranteed. The values listed are at room temperature and 5V.*
6. *If I_{OL} exceeds the test condition, V_{OL} may exceed the related specification. Pins are not guaranteed to sink current greater than the listed test conditions.*
7. *For other values, please contact your sales office.*
8. *Operating I_{CC} is measured with all output pins disconnected; XTAL1 driven with T_{CLCH}, T_{CHCL} = 5 ns (see Figure 39.), V_{IL} = V_{SS} + 0.5 V, V_{IH} = V_{CC} - 0.5V; XTAL2 N.C.; $\overline{RST}$/Vpp= V_{CC};. The internal ROM runs the code 80 FE (label: SJMP label). I_{CC} would be slightly higher if a crystal oscillator is used. Measurements are made with OTP products when possible, which is the worst case.*



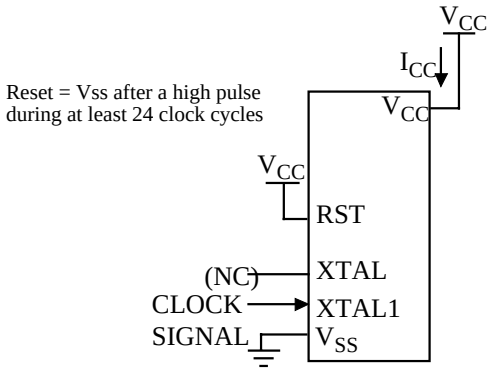
All other pins are disconnected.

Figure 35. I_{CC} Test Condition, under reset



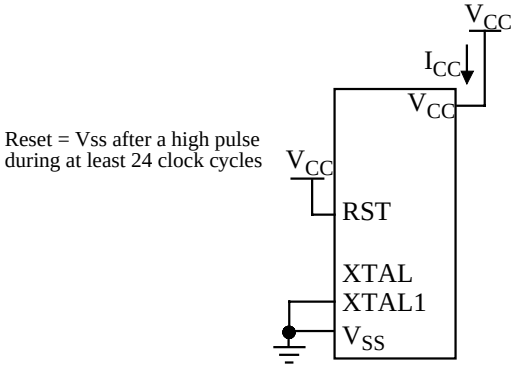
All other pins are disconnected.

Figure 36. Operating I_{CC} Test Condition



All other pins are disconnected.

Figure 37. I_{CC} Test Condition, Idle Mode



All other pins are disconnected.

Figure 38. I_{CC} Test Condition, Power-Down Mode

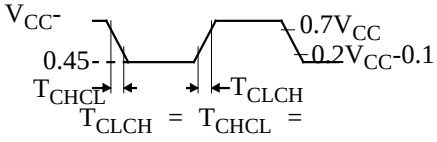


Figure 39. Clock Signal Waveform for I_{CC} Tests in Active and Idle Modes

18.5. DC Parameters for A/D Converter

T_A = 0°C to +70°C; V_{SS} = 0 V; V_{CC} = 2.7 V to 5.5 V; F = 0 to 30 MHz.
T_A = -40°C to +85°C; V_{SS} = 0 V; V_{CC} = 2.7 V to 5.5 V; F = 0 to 30 MHz.

Table 54. DC Parameters for Low Voltage

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
	Resolution		10		bit	

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
AVin	Analog input voltage	Vss- 0.2		Vcc + 0.2	V	
Rref	Resistance between Vref and Vss	13	18	24	KOhm	
Vref	Value of integrated voltage source	2.43		2.49	V	Small variation with Vcc and Temperature (1)
Lref	Load on integrated voltage source	10			KOhm	
Cai	Analog input Capacitance		60		pF	During sampling
	Integral non linearity		1	2	lsb	
	Differential non linearity		0.5	1	lsb	
	Offset error	-2		2	lsb	
	Input source impedance			1	KOhm	For 10 bit resolution at maximum speed

(1) Total drift on one part over full Voltage and Temperature range is below 20 mV

18.6. AC Parameters

18.6.1. Explanation of the AC Symbols

Each timing symbol has 5 characters. The first character is always a “T” (stands for time). The other characters, depending on their positions, stand for the name of a signal or the logical status of that signal. The following is a list of all the characters and what they stand for.

Example:T_{AVLL} = Time for Address Valid to ALE Low.
T_{LLPL} = Time for ALE Low to $\overline{PSEN}$ Low.

T_A = 0 to +70°C (commercial temperature range); V_{SS} = 0 V; V_{CC} = 5 V ± 10%; -V ranges.
T_A = -40°C to +85°C (industrial temperature range); V_{SS} = 0 V; V_{CC} = 5 V ± 10%; -V ranges.
T_A = 0 to +70°C (commercial temperature range); V_{SS} = 0 V; 2.7 V < V_{CC} < 5.5 V; -L range.
T_A = -40°C to +85°C (industrial temperature range); V_{SS} = 0 V; 2.7 V < V_{CC} < 5.5 V; -L range.

Table 55. gives the maximum applicable load capacitance for Port 0, Port 1, 2 and 3, and ALE and $\overline{PSEN}$ signals. Timings will be guaranteed if these capacitances are respected. Higher capacitance values can be used, but timings will then be degraded.

Table 55. Load Capacitance versus speed range, in pF

	-V	-L
Port 0	50	100
Port 1, 2, 3	50	80
ALE / $\overline{PSEN}$	30	100

Table 57., Table 60. and Table 61. give the description of each AC symbols.

Table 57., Table 59. and Table 62. give for each range the AC parameter.

Table 58., Table 60. and Table 63. give the frequency derating formula of the AC parameter. To calculate each AC symbols, take the x value corresponding to the speed grade you need (-V or -L) and replace this value in the formula. Values of the frequency must be limited to the corresponding speed grade:

Table 56. Max frequency for derating formula regarding the speed grade

	-V X1 mode	-V X2 mode	-L X1 mode	-L X2 mode
Freq (MHz)	40	30	30	20
T (ns)	25	33.3	33.3	50

Example:

T_{LLIV} in X2 mode for a -V part at 20 MHz (T = $1/20^{E6}$ = 50 ns):

x= 25 (Table 58.)

T= 50ns

T_{LLIV}= 2T - x = 2 x 50 - 25 = 75ns

18.6.2. External Program Memory Characteristics

Symbol	Parameter
T	Oscillator clock period
T_{LHLL}	ALE pulse width
T_{AVLL}	Address Valid to ALE
T_{LLAX}	Address Hold After ALE
T_{LLIV}	ALE to Valid Instruction In
T_{LLPL}	ALE to $\overline{PSEN}$
T_{PLPH}	$\overline{PSEN}$ Pulse Width
T_{PLIV}	$\overline{PSEN}$ to Valid Instruction In
T_{PXIX}	Input Instruction Hold After $\overline{PSEN}$
T_{PXIZ}	Input Instruction FloatAfter $\overline{PSEN}$
T_{PXAV}	$\overline{PSEN}$ to Address Valid
T_{AVIV}	Address to Valid Instruction In
T_{PLAZ}	$\overline{PSEN}$ Low to Address Float

Table 57. AC Parameters for Fix Clock

Speed	-V X2 mode 30 MHz 60 MHz equiv.		-V standard mode 40 MHz		-L X2 mode 20 MHz 40 MHz equiv.		-L standard mode 30 MHz		Units
Symbol	Min	Max	Min	Max	Min	Max	Min	Max	
T	33		25		50		33		ns
T_{LHLL}	25		42		35		52		ns
T_{AVLL}	4		12		5		13		ns
T_{LLAX}	4		12		5		13		ns
T_{LLIV}		45		78		65		98	ns
T_{LLPL}	9		17		10		18		ns
T_{PLPH}	35		60		50		75		ns
T_{PLIV}		25		50		30		55	ns
T_{PXIX}	0		0		0		0		ns
T_{PXIZ}		12		20		10		18	ns
T_{AVIV}		53		95		80		122	ns
T_{PLAZ}		10		10		10		10	ns

Table 58. AC Parameters for a Variable Clock: derating formula

Symbol	Type	Standard Clock	X2 Clock	-V	-L	Units
T_{LHLL}	Min	2 T - x	T - x	8	15	ns
T_{AVLL}	Min	T - x	0.5 T - x	13	20	ns
T_{LLAX}	Min	T - x	0.5 T - x	13	20	ns
T_{LLIV}	Max	4 T - x	2 T - x	22	35	ns
T_{LLPL}	Min	T - x	0.5 T - x	8	15	ns
T_{PLPH}	Min	3 T - x	1.5 T - x	15	25	ns
T_{PLIV}	Max	3 T - x	1.5 T - x	25	45	ns
T_{PXIX}	Min	x	x	0	0	ns
T_{PXIZ}	Max	T - x	0.5 T - x	5	15	ns
T_{AVIV}	Max	5 T - x	2.5 T - x	30	45	ns
T_{PLAZ}	Max	x	x	10	10	ns

18.6.3. External Program Memory Read Cycle

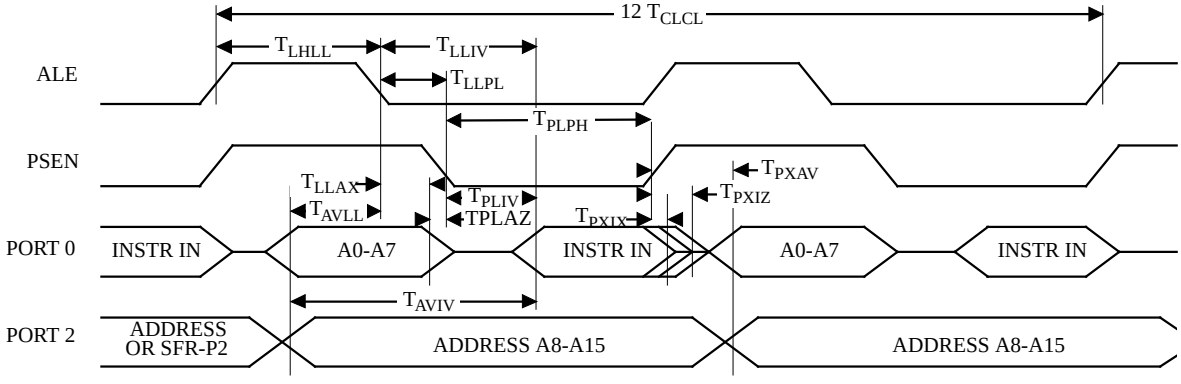


Figure 40. External Program Memory Read Cycle

18.6.4. External Data Memory Characteristics

Symbol	Parameter
T_{RLRH}	$\overline{RD}$ Pulse Width
T_{WLWH}	$\overline{WR}$ Pulse Width
T_{RLDV}	$\overline{RD}$ to Valid Data In
T_{RHDX}	Data Hold After $\overline{RD}$
T_{RHDZ}	Data Float After $\overline{RD}$
T_{LLDV}	ALE to Valid Data In
T_{AVDV}	Address to Valid Data In
T_{LLWL}	ALE to $\overline{WR}$ or $\overline{RD}$
T_{AVWL}	Address to $\overline{WR}$ or $\overline{RD}$
T_{QVWX}	Data Valid to $\overline{WR}$ Transition
T_{QVWH}	Data set-up to $\overline{WR}$ High
T_{WHQX}	Data Hold After $\overline{WR}$
T_{RLAZ}	$\overline{RD}$ Low to Address Float
T_{WHLH}	$\overline{RD}$ or $\overline{WR}$ High to ALE high

Table 59. AC Parameters for a Fix Clock

Speed	-V X2 mode 30 MHz 60 MHz equiv.		-V standard mode 40 MHz		-L X2 mode 20 MHz 40 MHz equiv.		-L standard mode 30 MHz		Units
Symbol	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	
T_{RLRH}	85		135		125		175		ns
T_{WLWH}	85		135		125		175		ns
T_{RLDV}		60		102		95		137	ns
T_{RHDX}	0		0		0		0		ns
T_{RHDZ}		18		35		25		42	ns
T_{LLDV}		98		165		155		222	ns
T_{AVDV}		100		175		160		235	ns
T_{LLWL}	30	70	55	95	45	105	70	130	ns
T_{AVWL}	47		80		70		103		ns
T_{QVWX}	7		15		5		13		ns
T_{QVWH}	107		165		155		213		ns
T_{WHQX}	9		17		10		18		ns
T_{RLAZ}		0		0		0		0	ns
T_{WHLH}	7	27	15	35	5	45	13	53	ns

Table 60. AC Parameters for a Variable Clock: derating formula

Symbol	Type	Standard Clock	X2 Clock	-V	-L	Units
T_{RLRH}	Min	6 T - x	3 T - x	15	25	ns
T_{WLWH}	Min	6 T - x	3 T - x	15	25	ns
T_{RLDV}	Max	5 T - x	2.5 T - x	23	30	ns
T_{RHDX}	Min	x	x	0	0	ns
T_{RHDZ}	Max	2 T - x	T - x	15	25	ns
T_{LLDV}	Max	8 T - x	4T -x	35	45	ns
T_{AVDV}	Max	9 T - x	4.5 T - x	50	65	ns
T_{LLWL}	Min	3 T - x	1.5 T - x	20	30	ns
T_{LLWL}	Max	3 T + x	1.5 T + x	20	30	ns
T_{AVWL}	Min	4 T - x	2 T - x	20	30	ns
T_{QVWX}	Min	T - x	0.5 T - x	10	20	ns
T_{QVWH}	Min	7 T - x	3.5 T - x	10	20	ns
T_{WHQX}	Min	T - x	0.5 T - x	8	15	ns
T_{RLAZ}	Max	x	x	0	0	ns
T_{WHLH}	Min	T - x	0.5 T - x	10	20	ns
T_{WHLH}	Max	T + x	0.5 T + x	10	20	ns

18.6.5. External Data Memory Write Cycle

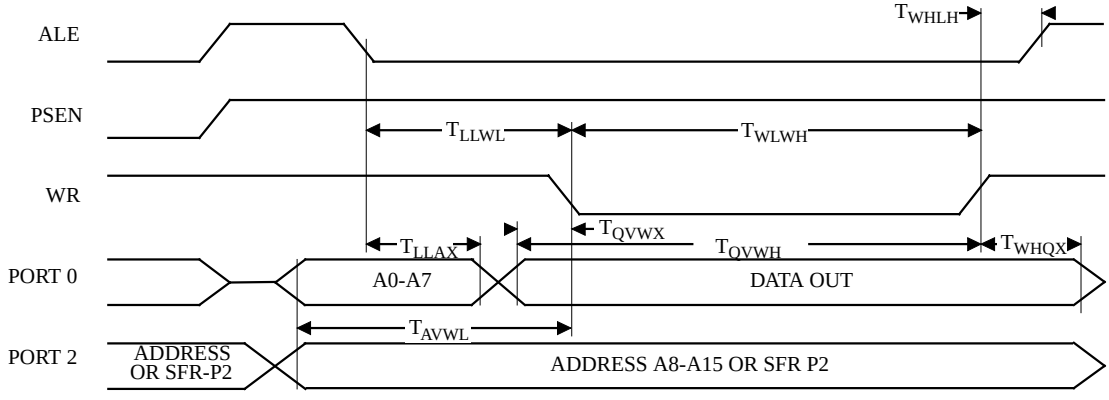


Figure 41. External Data Memory Write Cycle

18.6.6. External Data Memory Read Cycle

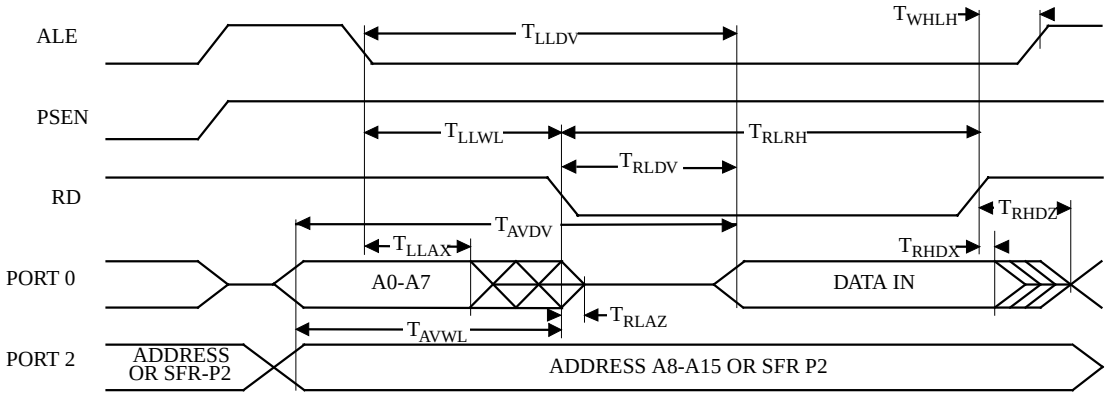


Figure 42. External Data Memory Read Cycle

18.6.7. Serial Port Timing - Shift Register Mode

Table 61. Symbol Description

Symbol	Parameter
T_{XLXL}	Serial port clock cycle time
T_{QVHX}	Output data set-up to clock rising edge
T_{XHQX}	Output data hold after clock rising edge
T_{XHDX}	Input data hold after clock rising edge
T_{XHDV}	Clock rising edge to input data valid

Table 62. AC Parameters for a Fix Clock

Speed	-V X2 mode 30 MHz 60 MHz equiv.		-V standard mode 40 MHz		-L X2 mode 20 MHz 40 MHz equiv.		-L standard mode 30 MHz		Units
Symbol	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	
T_{XLXL}	200		300		300		400		ns
T_{QVHX}	117		200		200		283		ns
T_{XHQX}	13		30		30		47		ns
T_{XHDX}	0		0		0		0		ns
T_{XHDV}		34		117		117		200	ns

Table 63. AC Parameters for a Variable Clock: derating formula

Symbol	Type	Standard Clock	X2 Clock	-V	-L	Units
T_{XLXL}	Min	12 T	6 T			ns
T_{QVHX}	Min	10 T - x	5 T - x	50	50	ns
T_{XHQX}	Min	2 T - x	T - x	20	20	ns
T_{XHDX}	Min	x	x	0	0	ns
T_{XHDV}	Max	10 T - x	5 T- x	133	133	ns

18.6.8. Shift Register Timing Waveforms

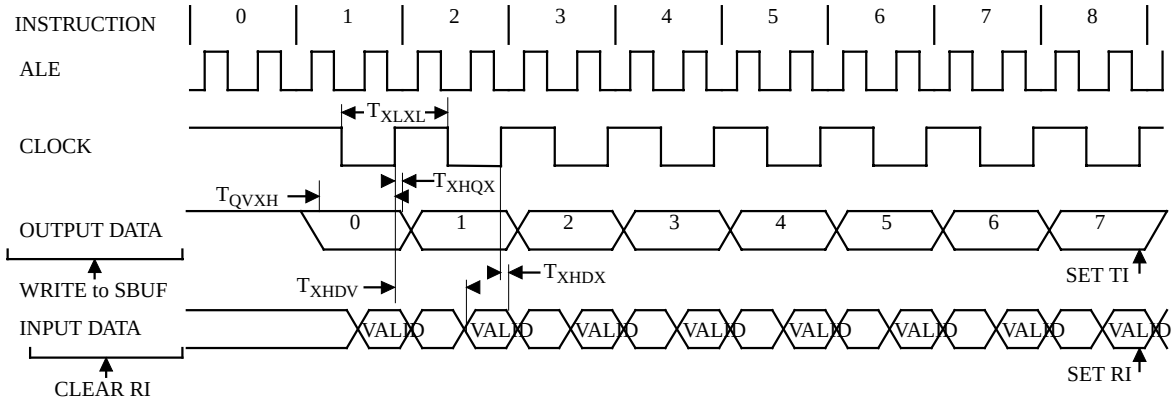


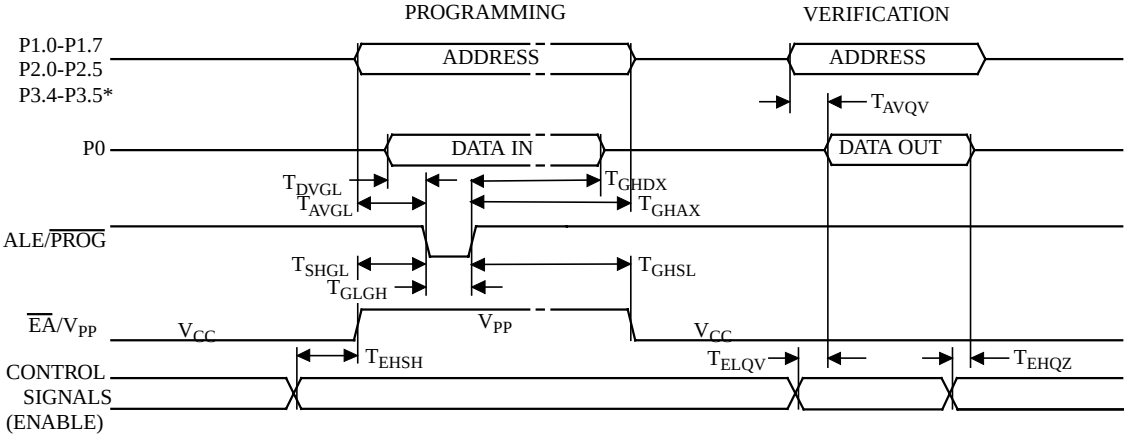
Figure 43. Shift Register Timing Waveforms

18.6.9. EPROM Programming and Verification Characteristics

T_A = 21°C to 27°C; V_{SS} = 0V; V_{CC} = 5V ± 10% while programming. V_{CC} = operating range while verifying

Symbol	Parameter	Min	Max	Units
V_{PP}	Programming Supply Voltage	12.5	13	V
I_{PP}	Programming Supply Current		75	mA
$1/T_{CLCL}$	Oscillator Frquency	4	6	MHz
T_{AVGL}	Address Setup to $\overline{PROG}$ Low	48 T_{CLCL}		
T_{GHAX}	Adress Hold after $\overline{PROG}$	48 T_{CLCL}		
T_{DVGL}	Data Setup to $\overline{PROG}$ Low	48 T_{CLCL}		
T_{GHDX}	Data Hold after $\overline{PROG}$	48 T_{CLCL}		
T_{EHSH}	(Enable) High to V_{PP}	48 T_{CLCL}		
T_{SHGL}	V_{PP} Setup to $\overline{PROG}$ Low	10		µs
T_{GHSL}	V_{PP} Hold after $\overline{PROG}$	10		µs
T_{GLGH}	$\overline{PROG}$ Width	90	110	µs
T_{AVQV}	Address to Valid Data		48 T_{CLCL}	
T_{ELQV}	ENABLE Low to Data Valid		48 T_{CLCL}	
T_{EHQZ}	Data Float after ENABLE	0	48 T_{CLCL}	

18.6.10. EPROM Programming and Verification Waveforms



* 8KB: up to P2.4, 16KB: up to P2.5, 32KB: up to P3.4, 64KB: up to P3.5

Figure 44. EPROM Programming and Verification Waveforms

18.6.11. External Clock Drive Characteristics (XTAL1)

Symbol	Parameter	Min	Max	Units
T_{CLCL}	Oscillator Period	25		ns
T_{CHCX}	High Time	5		ns
T_{CLCX}	Low Time	5		ns
T_{CLCH}	Rise Time		5	ns
T_{CHCL}	Fall Time		5	ns
T_{CHCX}/T_{CLCX}	Cyclic ratio in X2 mode	40	60	%

18.6.12. External Clock Drive Waveforms

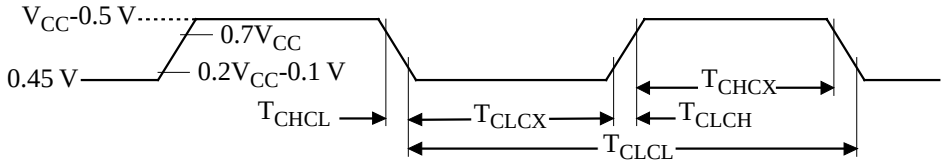


Figure 45. External Clock Drive Waveforms

18.6.13. A/D comverter

Symbol	Parameter	Min	Typ	Max	Units
	Conversion time		11		Clock periods (1 for sampling, 10 for conversion)
Fconv_ck	Clock Conversion frequency			350 (1)	kHz
	Sampling frequency	8		32	kHz

Notes: (1)For 10 bits resolution

18.6.14. AC Testing Input/Output Waveforms

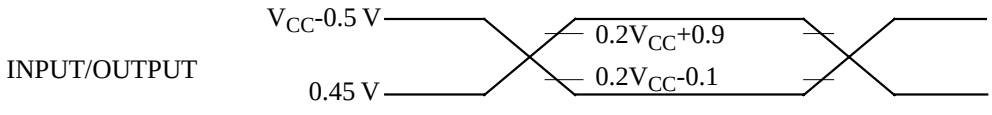


Figure 46. AC Testing Input/Output Waveforms

AC inputs during testing are driven at V_{CC} - 0.5 for a logic “1” and 0.45V for a logic “0”. Timing measurement are made at V_{IH} min for a logic “1” and V_{IL} max for a logic “0”.

18.6.15. Float Waveforms

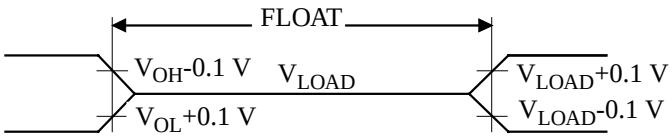


Figure 47. Float Waveforms

For timing purposes a port pin is no longer floating when a 100 mV change from load voltage occurs and begins to float when a 100 mV change from the loaded V_{OH}/V_{OL} level occurs. $I_{OL}/I_{OH} \geq \pm$ 20mA.

18.6.16. Clock Waveforms

Valid in normal clock mode. In X2 mode XTAL2 signal must be changed to XTAL2 divided by two.

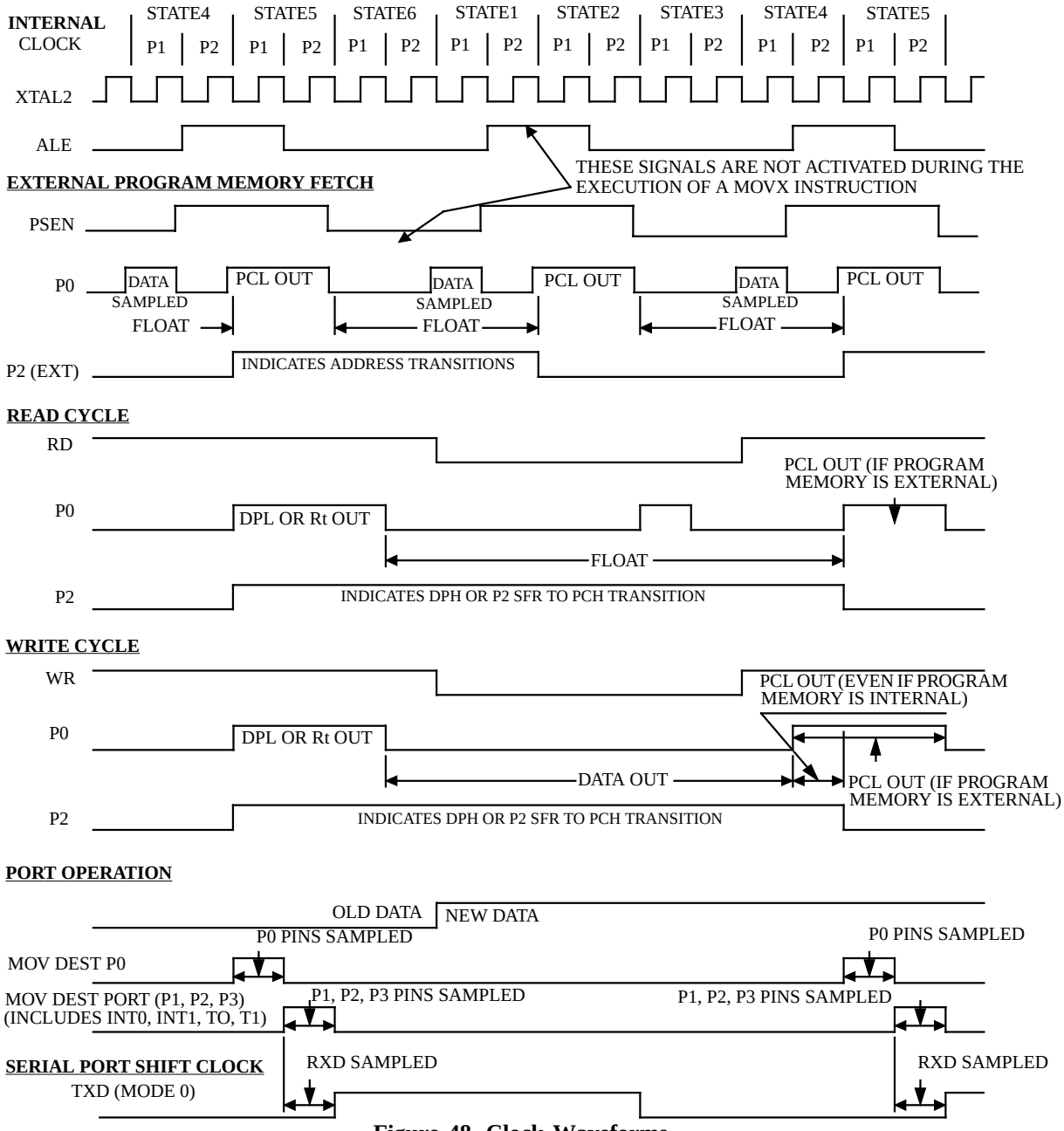


Figure 48. Clock Waveforms

This diagram indicates when signals are clocked internally. The time it takes the signals to propagate to the pins, however, ranges from 25 to 125 ns. This propagation delay is dependent on variables such as temperature and pin loading. Propagation also varies from output to output and component. Typically though (T_A=25°C fully loaded) $\overline{RD}$ and $\overline{WR}$ propagation delays are approximately 50ns. The other signals are typically 85 ns. Propagation delays are incorporated in the AC specifications.

19. Ordering Information

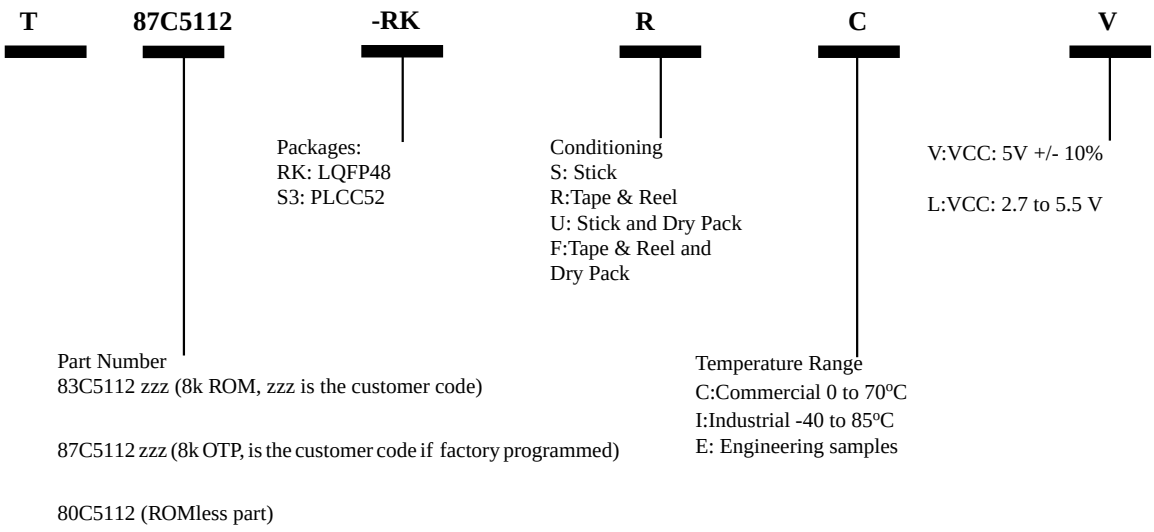


Table 64. Maximum Clock Frequency

Code	-V	-L	Unit
Standard Mode, oscillator frequency Standard Mode, internal frequency	40 40	40 40	MHz
X2 Mode, oscillator frequency X2 Mode, internal equivalent frequency	33 **66**	20 **40**	MHz

Notes: -L parts supplied with 5V +-10% have same speed as -V parts

Table 65. Possible order entries

Extension	Type	T83C5112 Mask ROM	T87C5112 OTP	T80C5112 ROMless
-S3SCL	PLCC52, Stick, Comm. 2.7-5.5V, 40 MHz			
-S3SCV	PLCC52, Stick, Comm. 5V, 66MHz			
-S3SIL	PLCC52, Stick, Ind. 2.7-5.5V, 40 MHz	X	X	X
-S3RCL	PLCC52, Tape & Reel, Comm. 2.7-5.5V, 40 MHz			
-S3RCV	PLCC52, Tape & Reel, Comm. 5V, 66MHz			
-S3RIL	PLCC52, Tape & Reel, Ind. 2.7-5.5V, 40 MHz	X	X	X
-RKUCL	LQFP48, Stick & Dry Pack, Comm. 2.7-5.5V, 40 MHz			
-RKUCV	LQFP48, Stick & Dry Pack, Comm. 5V, 66MHz			
-RKUIL	LQFP48, Stick & Dry Pack, Ind. 2.7-5.5V, 40 MHz	X	X	X
-RKFCL	LQFP48, Tape & Reel & Dry Pack, Comm. 2.7-5.5V, 40 MHz			
-RKFCV	LQFP48, Tape & Reel & Dry Pack, Comm. 5V, 66MHz			
-RKFIL	LQFP48, Tape & Reel & Dry Pack, Ind. 2.7-5.5V, 40 MHz	X	X	X
-RKSEL	Engineering sample, LQFP48, Stick, 2.7-5.5V, 40MHz		X	
-TDSEL	Engineering sample, PLCC52, Stick, 2.7-5.5V, 40MHz		X	