CMOS single-chip 8-bit MCU with 12-bit ADC and LDO

Main features

8-bit Microcontroller with high performance M8051 CPU

Basic MCU Function

- 6 Kbytes Flash Code Memory
- Code Area Protection
- 256 bytes SRAM Data Memory

Built-in Analog Function

- Power-On Reset and Low Voltage Indicator Reset
- Internal 32 MHz RC Oscillator

Peripheral features

- 12-bit Analog to Digital Converter with 2.5V LDO

I/O and packages

- Up to 18 programmable I/O lines with 20pin package
- Package types 20QFN, 20TSSOP, 16SOPN

Operating conditions

- -40°C to 85°C temperature range
- 2.2V to 5.5V wide operation range

Application

- Battery charge & discharge control
- Small home appliance

MC96F1206

User's Manual

V 1.5

Revised 18 Sept, 2018

Revision history

Version	Date	Revision list
1.0	2016.01.18	Initial Release
1.1	2016.04.20	Delete ‘ENBODST’ in BODR register Update MCU stabilization time Update table format and contents in 7 Electrical Characteristics Add 7.11 Operating Voltage Range and 7.12 Typical Characteristics Change ‘VREF2P3EN’ to ‘VREF2P3SEL‘ in LDOCR Change BOD to LVI (name change)
1.2	2016.06.29	Correct ‘24QFN’ to ‘20QFN’ in Figure 3.1 Correct PIN Number in Figure 3.3 Update 20QFN package diagram in Figure 4.1 Delete 20SOP package
1.3	2017.03.16	Correct symbol discrepancies in 7 Electrical characteristics. Correct WDT block diagram in Figure 10.2.
1.4	2017.04.25	Update 20TSSOP package diagram in Figure 4.2 Update 16SOPN package diagram in Figure 4.3 Correct ordering information in Table 1.1
1.5	2018.09.18	Revised this book. Added Nomenclature Figure 1.1 Update Figure 1.4 OCD Interface Circuit Added Chapter 1.3.3 OCD Port Operation. Updated Chapter 7.5 Power-On Reset VDD Voltage Rising Time. Added Chapter 7.13 Recommended Application Circuit. Updated POD (20-QFN_3x3)

Version 1.5

Published by AE team

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1 Overview

1.1. Description

The MC96F1206 is an advanced CMOS 8-bit microcontroller with 6 Kbytes of FLASH. This is powerful microcontroller which provides a highly flexible and cost effective solution to many embedded control applications. This provides the following features : 6 Kbytes of FLASH, 256 bytes of SRAM, 16-bit timer/counter/PWM, Watchdog timer with WDTOSC, 12-bit ADC with LDO, On-chip POR, LVI and LVR, Internal RC-Oscillator, Internal WDT-Oscillator and clock circuitry. The MC96F1206 also supports Power saving modes to reduce Power Consumption.

Device Name	FLASH	IRAM	XRAM	ADC	I/O PORT	Package
MC96F1206USBN	6 Kbytes	256 bytes	-	15 inputs	18	20-QFN
MC96F1206RBN	6 Kbytes	256 bytes	-	15 inputs	18	20-TSSOP
MC96F1206MBN	6 Kbytes	256 bytes	-	12 inputs	14	16-SOPN

Table 1.1 Ordering Information of MC96F1206

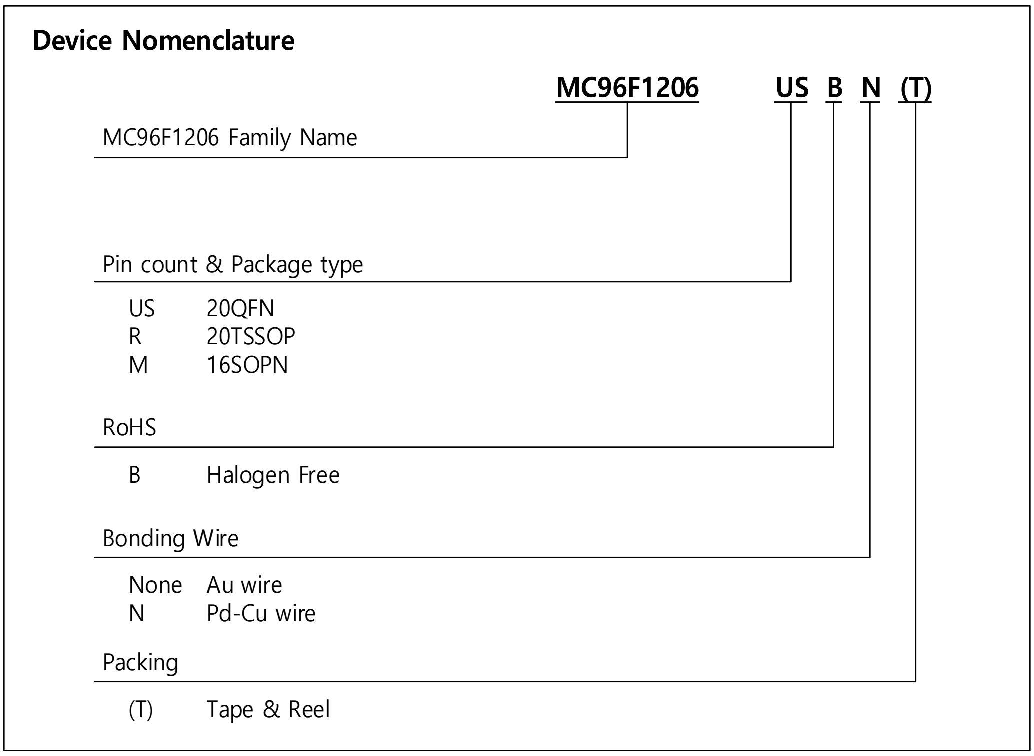


Figure 1.1 Device Nomenclature

1.2 Features

- **CPU**
  - M8051 (8051 Compatible, 2 clock per cycle)
- **6 Kbytes On-Chip FLASH**
  - Endurance : 10,000 times at room temperature
  - Retention : 10 years
  - Self-Writing (Code protect option)
- 256 bytes IRAM
- **Input Output Ports**
  - GPIO 18
- **Timer/Counter**
  - 16-bit × 2-ch (Timer0, Timer1)
  - Basic Interval Timer
- **PWM** (16-bit 2-ch, Using Timer0,1)
- **Watch Dog Timer**
- **12-bit A/D Converter**
  - 15-Input channels
  - Internal 2.5V LDO reference (option)
- **Interrupt Sources**
  - External Interrupts (3, with PCI)
  - Timer (2)
  - ADC (1)
  - BIT (1)
  - WDT (1)
  - LVI (1)
- **On-Chip RC-Oscillator**
  - 32MHz (±5%) Oscillator
- **On-Chip WDT-Oscillator**
  - 8kHz (±50%) Oscillator
- **Power On Reset**
  - 1.1 V
- **Low Voltage Reset**
  - 1-Level (1.75 V)
- **Low Voltage Indicator**
  - 3-Level (2.1 V, 2.5 V, 3.5 V)
- **Minimum Instruction Execution Time**
  - 125ns (@16MHz, NOP Instruction)
- **Power Down Mode**
  - IDLE, STOP1, STOP2 mode
- **Operating Frequency**
  - 16 MHz
- **Operating Voltage**
  - 2.2V~5.5V
- **Operating Temperature :** –40 ~ +85℃
- **Package Type**
  - 20 QFN/TSSOP, 16 SOPN
  - Pb free package

1.3 Development tools

1.3.1 Compiler

ABOV semiconductor does not provide any compiler for the MC96F1206. But the CPU core of MC96F1206 is M8051 core, you can use all kinds of third party's standard 8051 compiler like Keil C Compiler, Open Source SDCC (Small Device C Compiler). These compilers' output debug information can be integrated with our OCD2 emulator and debugger. Refer to OCD2 manual for more details.

1.3.2 OCD2 emulator and debugger

The OCD2 emulator supports ABOV Semiconductor’s 8051 series MCU emulation.

The OCD2 interface uses two wires interfacing between PC and MCU which is attached to user’s system. The OCD2 can read or change the value of MCU internal memory and I/O peripherals. And also the OCD2 controls MCU internal debugging logic, it means OCD2 controls emulation, step run, monitoring etc.

The OCD2 Debugger program works on Microsoft-Windows NT, 2000, XP, Vista (32-bit), 7, 8, 8.1 operating system.

If you want to see more details, please refer OCD2 debugger manual. You can download debugger S/W and manual from our web-site.

1.3.3 OCD Port Operation

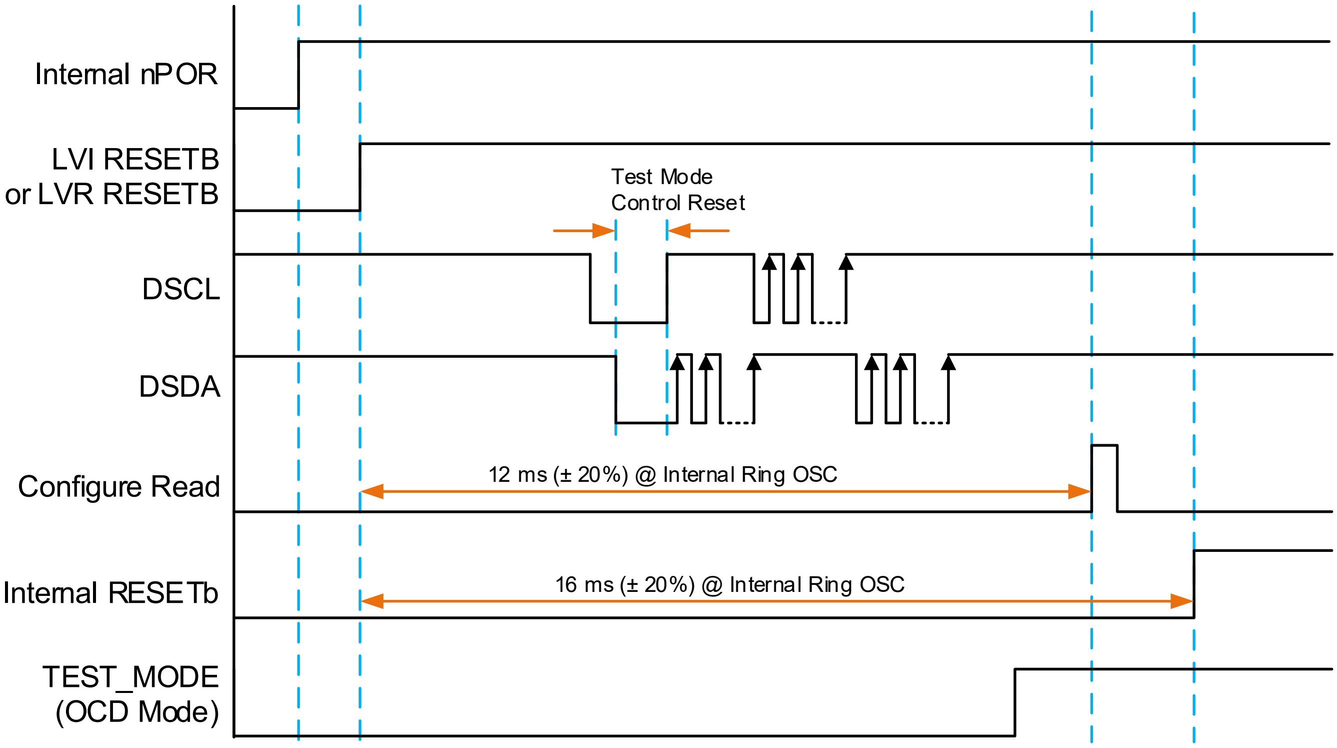


Figure 1.2 OCD Mode Sequence

The OCD port is used for flash program writing and device debugging. The device has a section that determines whether to use it in that mode of POR. This is done when the internal reset is cleared and waiting to clear Configure Read and Internal Reset. If the internal reset is cleared and DSCL and DSDA wait for a period of time from internal pull-up 'high' to 'low', the internal controller for entering test mode is initialized. Then, when DSCA and DSCA appointed communication, the test mode is entered.

As described above, OCD port is a port for special purpose. Even if it is used as Normal GPIO in User Program, it is necessary to limit the state to prevent malfunction during POR. Therefore, it is recommended to connect Pull-up Resistor to the outside of OCD Port and to fix OCD Port input to VDD / GND at POR. If it is difficult to apply pull-up on the circuit, install at least 0.1uf bypass capacitor to prevent Floating state at POR. However, if you install a bypass cap, you can not use on board writing and OCD Debugger.

There are OCD2 mode connection

- P01 (MC96F1206 DSCL pin)
- P00 (MC96F1206 DSDA pin)

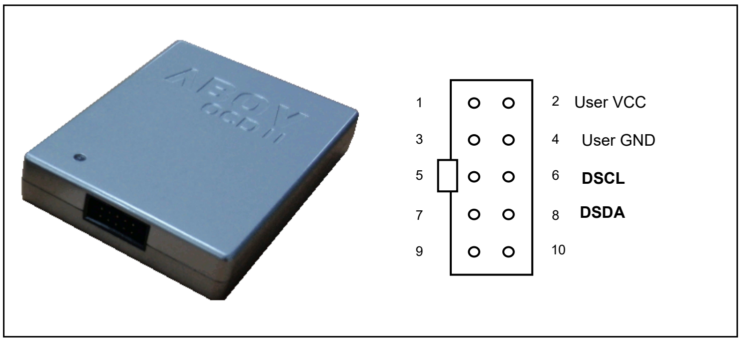


Figure 1.3 On Chip Debugger 2 and Pin description

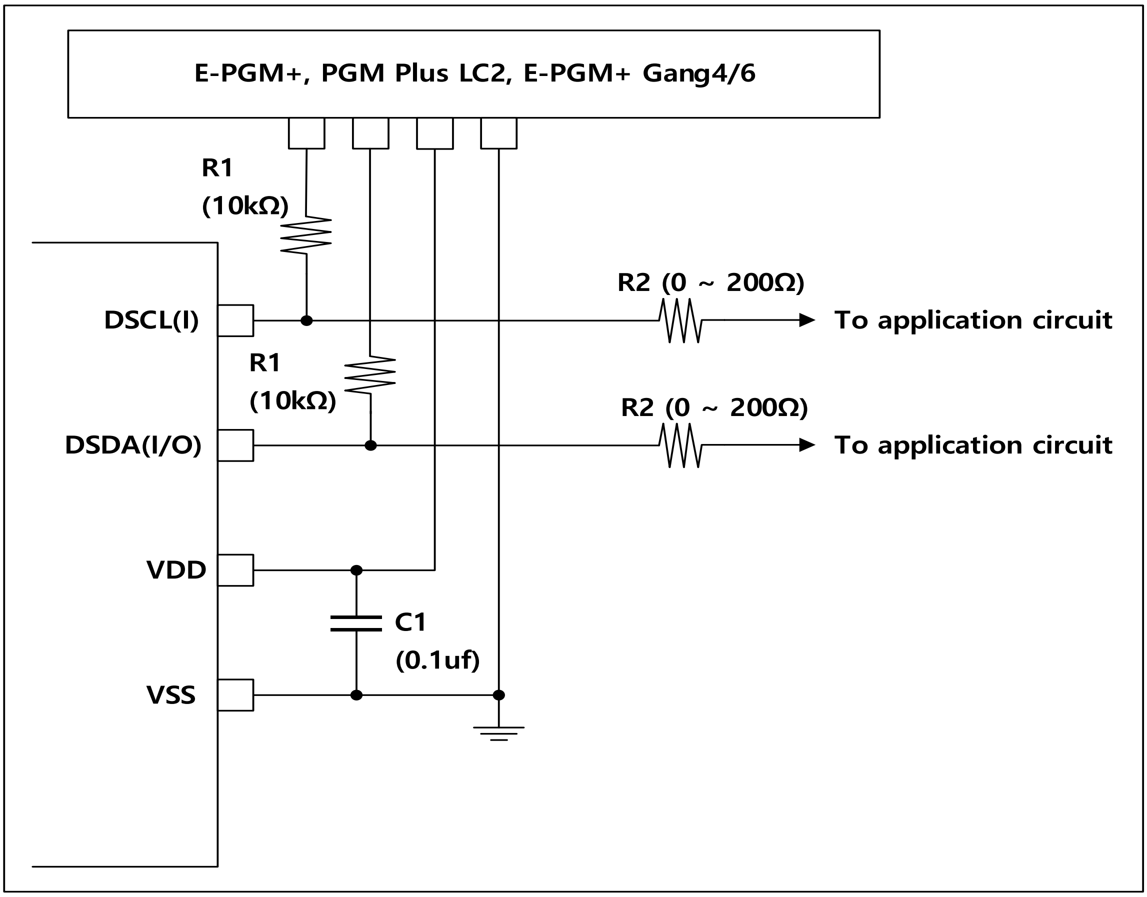


Figure 1.4 OCD Interface Circuit

NOTE)

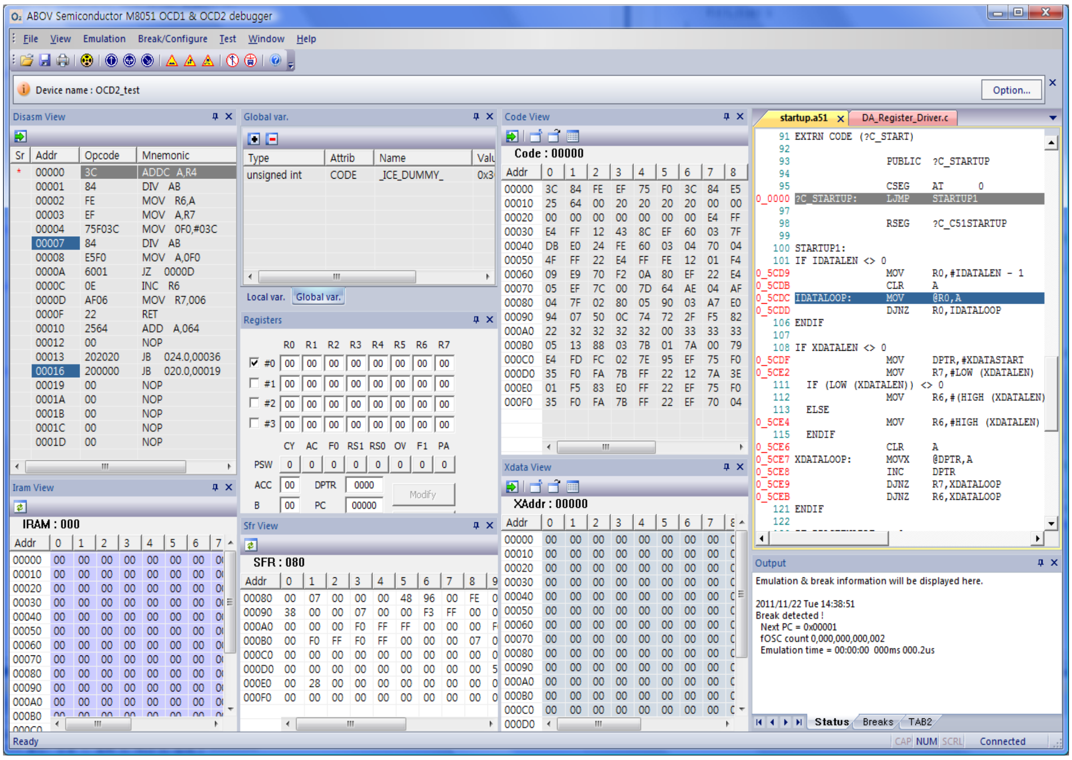
1. In on-board programming mode, very high-speed signal will be provided to pin DSCL and DSDA. And it will cause some damages to the application circuits connected to DSCL or DSDA port if the application circuit is designed as high speed response such as relay control circuit. If possible, the I/O configuration of DSDA, DSCL pins had better be set to input mode.
2. The value of R1, R2 and C1 is recommended value. It varies with circuit of system.

OCD2 (On Chip Debug) Emulator

- MCU emulation control via 2pin or 3pin OCD interface.
- 2pin interface : OCD2 clock & data.
- 1pin option interface
  - Support device OCD2 mode entry during user S/W is running.
  - Support exact emulation time measurement.
- Higher interface speed than OCD dongle.
- Support newly added debugging specifications.
  - Data access break (1, 2, 4bytes),
  - internal OSC Frequency measurement and trimming, etc.
- Compact size.
- Cost effective emulator.
- Emulation & debugging on the target system directly.
- Real time emulation.
- PC interface : USB.

Debugger

- Operates with OCD2 emulator H/W.
- Integrated Development Environment (IDE).
  Support docking windows and menus.
- Support Free run, Step run, auto step run.
- Support Symbolic debugging.
- Support Source level debugging.



Device name : OCD2_test

Sr	Addr	Opcode	Mnemonic
*	00000	3C	ADDC A,R4
	00001	84	DIV AB
	00002	FE	MOV R6,A
	00003	EF	MOV A,R7
	00004	75F03C	MOV 0F0,#03C
	00007	84	DIV AB
	00008	E5F0	MOV A,0F0
	0000A	6001	JZ 0000D
	0000C	0E	INC R6
	0000D	AF06	MOV R7,006
	0000F	22	RET
	00010	2564	ADD A,064
	00012	00	NOP
	00013	202020	JB 024.0,00036
	00016	200000	JB 020.0,00019
	00019	00	NOP
	0001A	00	NOP
	0001B	00	NOP
	0001C	00	NOP
	0001D	00	NOP

Type	Attrib	Name	Valu
unsigned int	CODE	_ICE_DUMMY_	0x3

	R0	R1	R2	R3	R4	R5	R6	R7
☑ #0	00	00	00	00	00	00	00	00
□ #1	00	00	00	00	00	00	00	00
□ #2	00	00	00	00	00	00	00	00
□ #3	00	00	00	00	00	00	00	00

	CY	AC	F0	RS1	RS0	OV	F1	PA
PSW	0	0	0	0	0	0	0	0

ACC 00 DPTR 0000
B 00 PC 00000

Code : 00000

Addr	0	1	2	3	4	5	6	7	8
00000	3C	84	FE	EF	75	F0	3C	84	E5
00010	25	64	00	20	20	20	20	00	00
00020	00	00	00	00	00	00	00	E4	FF
00030	E4	FF	12	43	8C	EF	60	03	7F
00040	DB	E0	24	FE	60	03	04	70	04
00050	4F	FF	22	E4	FF	FE	12	01	F4
00060	09	E9	70	F2	0A	80	EF	22	E4
00070	05	EF	7C	00	7D	64	AE	04	AF
00080	04	7F	02	80	05	90	03	A7	E0
00090	94	07	50	0C	74	72	2F	F5	82
000A0	22	32	32	32	32	00	33	33	33
000B0	05	13	88	03	7B	01	7A	00	79
000C0	E4	FD	FC	02	7E	95	EF	75	F0
000D0	35	F0	FA	7B	FF	22	12	7A	3E
000E0	01	F5	83	E0	FF	22	EF	75	F0
000F0	35	F0	FA	7B	FF	22	EF	70	04

```
     91 EXTRN CODE (?C_START)
     92
     93                 PUBLIC  ?C_STARTUP
     94
     95                 CSEG    AT      0
 0_0000 ?C_STARTUP:     LJMP    STARTUP1
     97
     98                 RSEG    ?C_C51STARTUP
     99
    100 STARTUP1:
    101 IF IDATALEN <> 0
 0_5CD9                 MOV     R0,#IDATALEN - 1
 0_5CDB                 CLR     A
 0_5CDC IDATALOOP:      MOV     @R0,A
 0_5CDD                 DJNZ    R0,IDATALOOP
    106 ENDIF
    107
    108 IF XDATALEN <> 0
 0_5CDF                 MOV     DPTR,#XDATASTART
 0_5CE2                 MOV     R7,#LOW (XDATALEN)
    111   IF (LOW (XDATALEN)) <> 0
    112                 MOV     R6,#(HIGH (XDATALEN)
    113   ELSE
 0_5CE4                 MOV     R6,#HIGH (XDATALEN)
    115   ENDIF
 0_5CE6                 CLR     A
 0_5CE7 XDATALOOP:      MOVX    @DPTR,A
 0_5CE8                 INC     DPTR
 0_5CE9                 DJNZ    R7,XDATALOOP
 0_5CEB                 DJNZ    R6,XDATALOOP
    121 ENDIF
    122
```

IRAM : 000

Addr	0	1	2	3	4	5	6	7
00000	00	00	00	00	00	00	00	00
00010	00	00	00	00	00	00	00	00
00020	00	00	00	00	00	00	00	00
00030	00	00	00	00	00	00	00	00
00040	00	00	00	00	00	00	00	00
00050	00	00	00	00	00	00	00	00
00060	00	00	00	00	00	00	00	00
00070	00	00	00	00	00	00	00	00
00080	00	00	00	00	00	00	00	00
00090	00	00	00	00	00	00	00	00
000A0	00	00	00	00	00	00	00	00

SFR : 080

Addr	0	1	2	3	4	5	6	7	8
00080	00	07	00	00	00	48	96	00	FE
00090	38	00	00	07	00	00	F3	FF	00
000A0	00	00	00	F0	FF	FF	00	00	00
000B0	00	F0	FF	F0	FF	00	00	00	07
000C0	00	00	00	00	00	00	00	00	00
000D0	00	00	00	00	00	00	00	00	00
000E0	00	28	00	00	00	00	00	00	00
000F0	00	00	00	00	00	00	00	00	00

XAddr : 00000

Addr	0	1	2	3	4	5	6	7
00000	00	00	00	00	00	00	00	00
00010	00	00	00	00	00	00	00	00
00020	00	00	00	00	00	00	00	00
00030	00	00	00	00	00	00	00	00
00040	00	00	00	00	00	00	00	00
00050	00	00	00	00	00	00	00	00
00060	00	00	00	00	00	00	00	00
00070	00	00	00	00	00	00	00	00
00080	00	00	00	00	00	00	00	00
00090	00	00	00	00	00	00	00	00
000A0	00	00	00	00	00	00	00	00
000B0	00	00	00	00	00	00	00	00
000C0	00	00	00	00	00	00	00	00

```
Emulation & break information will be displayed here.

2011/11/22 Tue 14:38:51
Break detected !
  Next PC = 0x00001
  fOSC count 0,000,000,000,002
  Emulation time = 00:00:00  000ms 000.2us
```

Figure 1.5 OCD Debugger

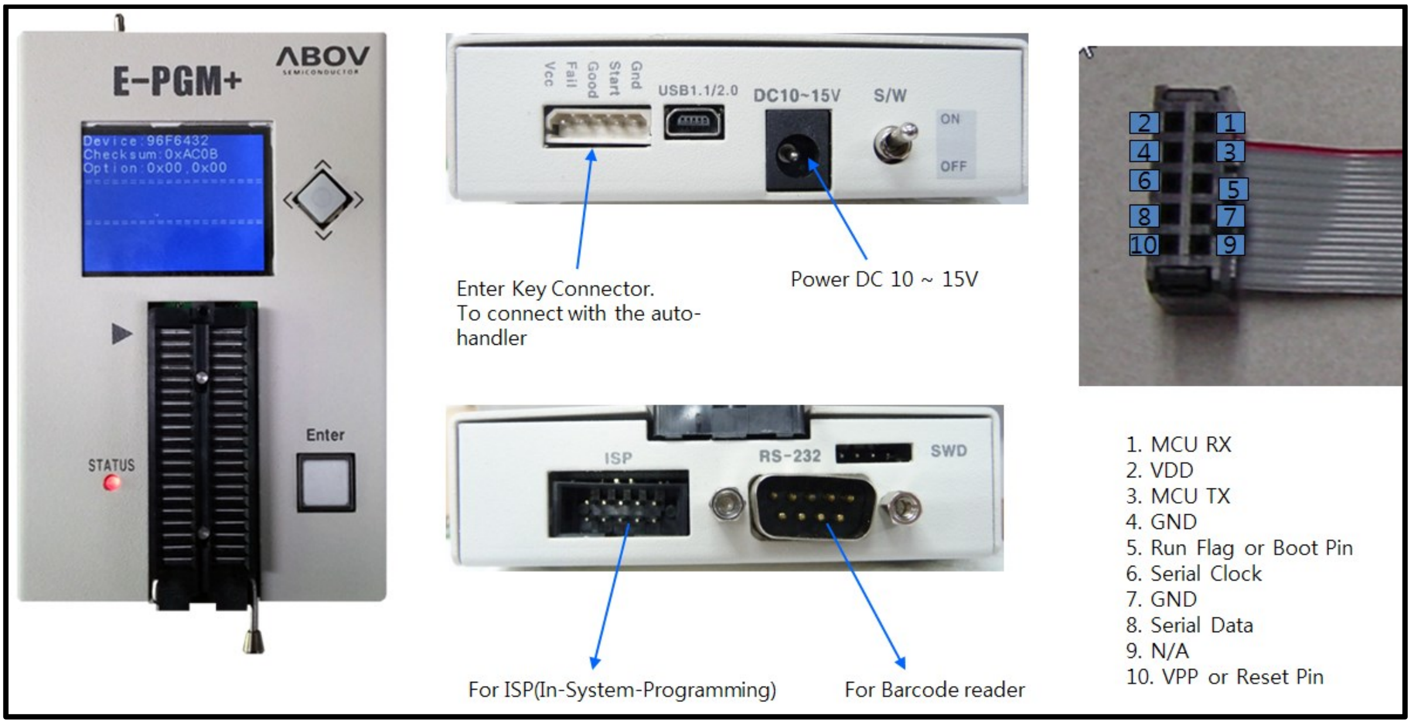
Support Devices

- MC95xxxx
- MC96xxxx
- MC97xxxx

1.3.4 Programmer

E-PGM +

- Support ABOV / ADAM devices
- 2~5 times faster than S-PGM+
- Main controller : 32 bit MCU @ 72MHz
- Buffer memory : 1 MByte



Enter Key Connector.
To connect with the auto-handler

Power DC 10 ~ 15V

For ISP(In-System-Programming)

For Barcode reader

1. MCU RX
2. VDD
3. MCU TX
4. GND
5. Run Flag or Boot Pin
6. Serial Clock
7. GND
8. Serial Data
9. N/A
10. VPP or Reset Pin

Figure 1.6 PGMplus USB

PGMPlusLC 2

Description

PGMPlusLC2 is for ISP (In System Programming). It is used to write into the MCU Which is already mounted on target board using 10pin cable.

Features

- PGMplusLC2 is low cost writing Tool.
- USB interface is supported.
- Not need USB driver installation.
- Connect the external power adaptor (5v@2A).
- Fast 32-bit Cortex-M3 MCU is used.
- Supported high voltage Max 18V.
- PGMplusLC2 is based on PC environment.
- PGMplusLC2 is faster than PGMplusLC.
- Transmission speed is 64Kbyte/s

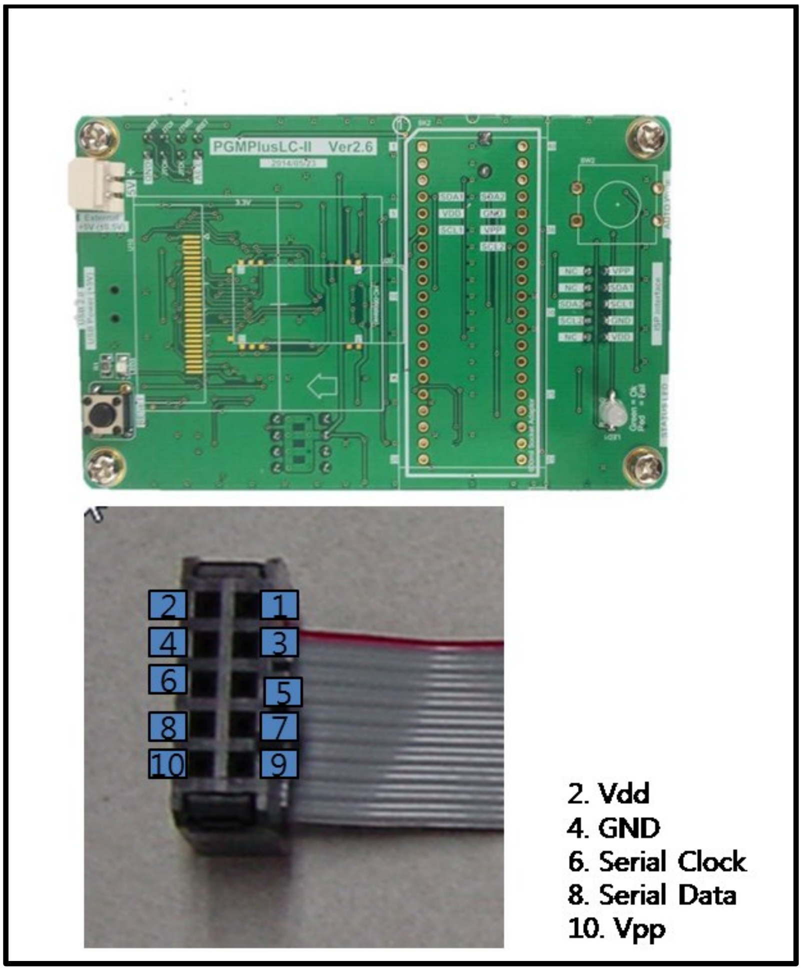


Figure 1.7 PGMplusLC Writer

E-PGM+ Gang4/6

- Product name : **E-PGM+ GANG 4**
- Dimension(x , y, h) : 33.5 x 22.5 x35mm
- Weight : 2.0kg
- Input Voltage : DC Adaptor 15V/2A
- Power Consumption :
- Operating Temp : -10 ~ 40℃
- Storage Temp : -30 ~ 80℃
- Water Proof : No

- Product name : **E-PGM+ GANG 6**
- Dimension(x , y, h) : 148.2 x 22.5 x35mm
- Weight : 2.8kg

- Input Voltage : DC Adaptor 15V/2A
- Power Consumption :
- Operating Temp : -10 ~ 40℃
- Storage Temp : -30 ~ 80℃
- Water Proof : No

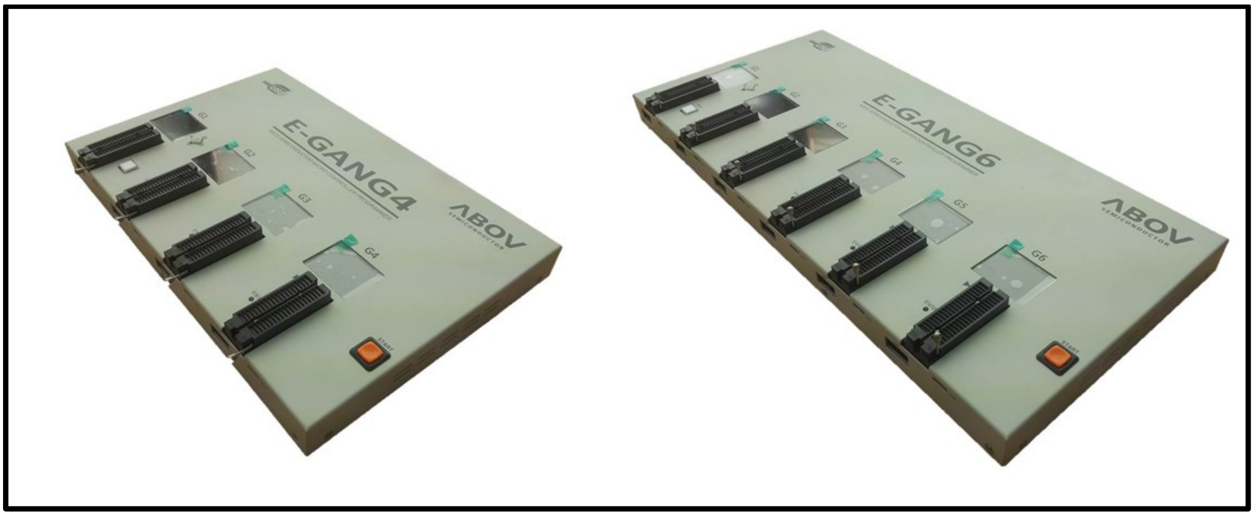


Figure 1.8 Gang Programmer

2 Block diagram

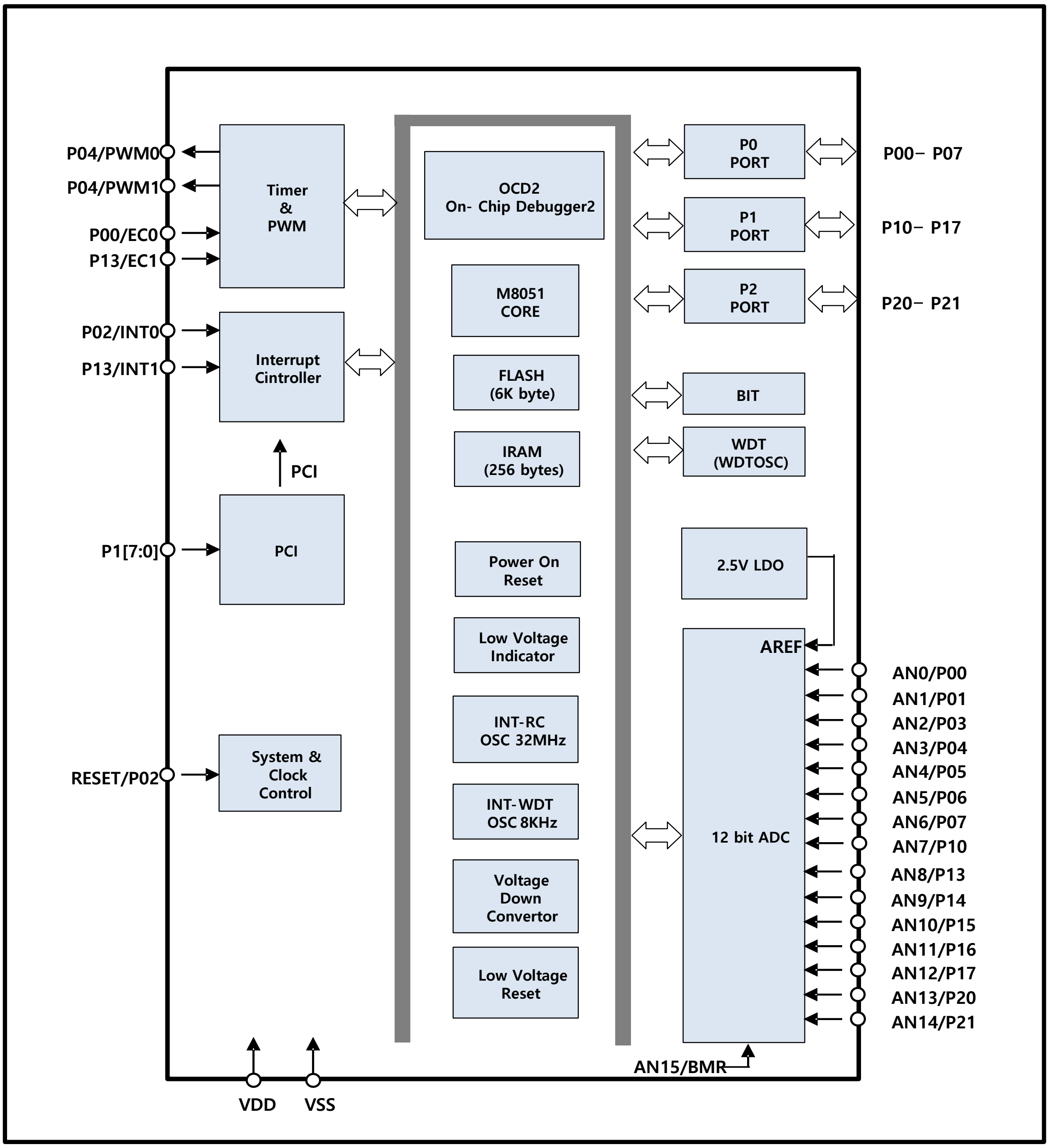


Figure 2.1 Block diagram of MC96F1206

3 Pin assignment

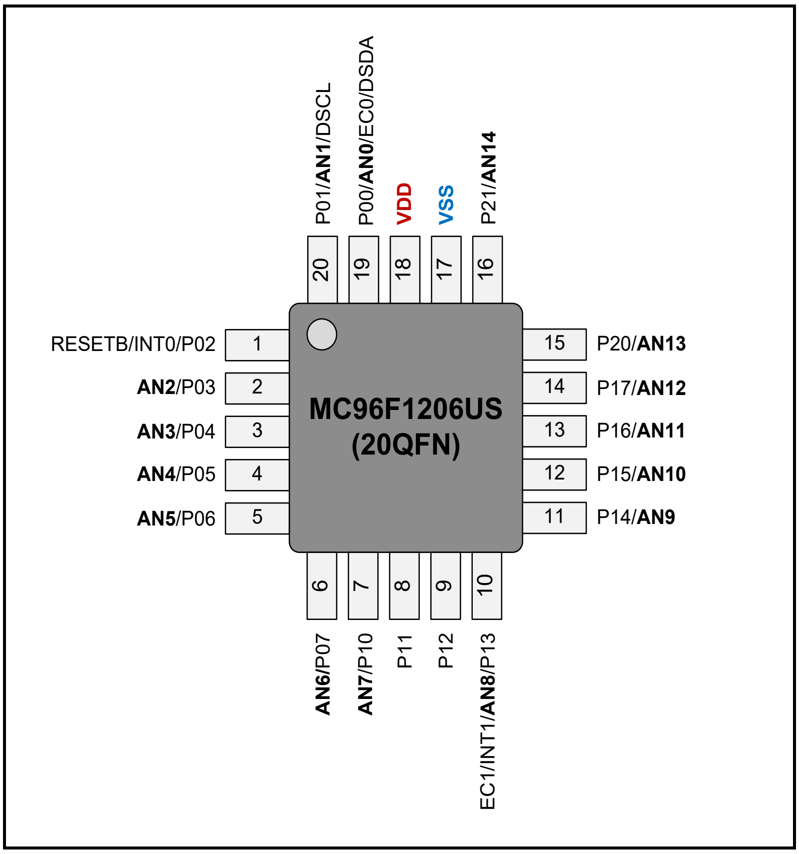


Figure 3.1 MC96F1206 20QFN assignment

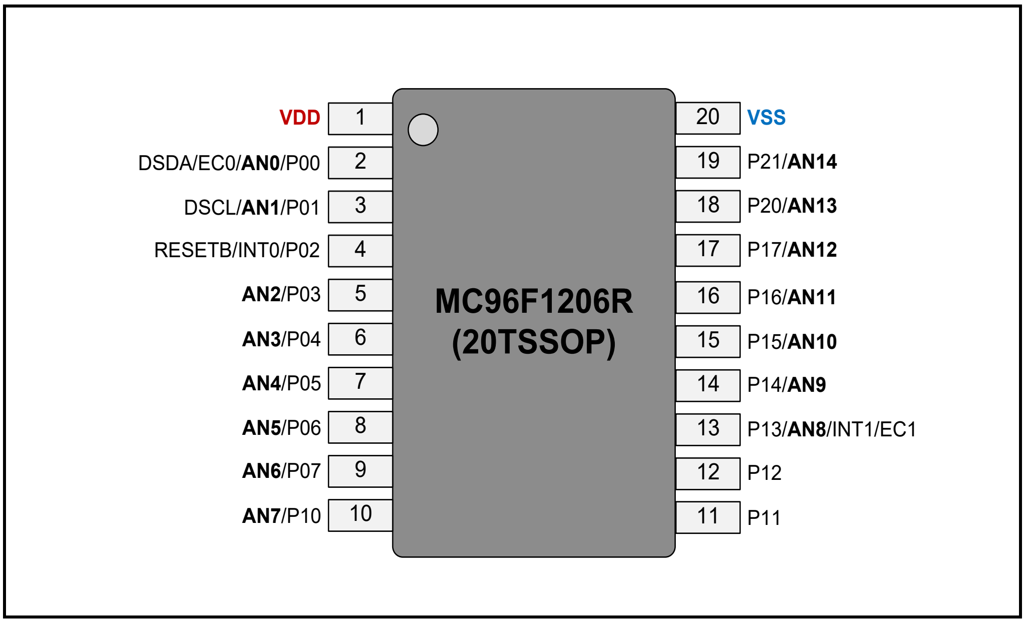


Figure 3.2 MC96F1206 20TSSOP assignment

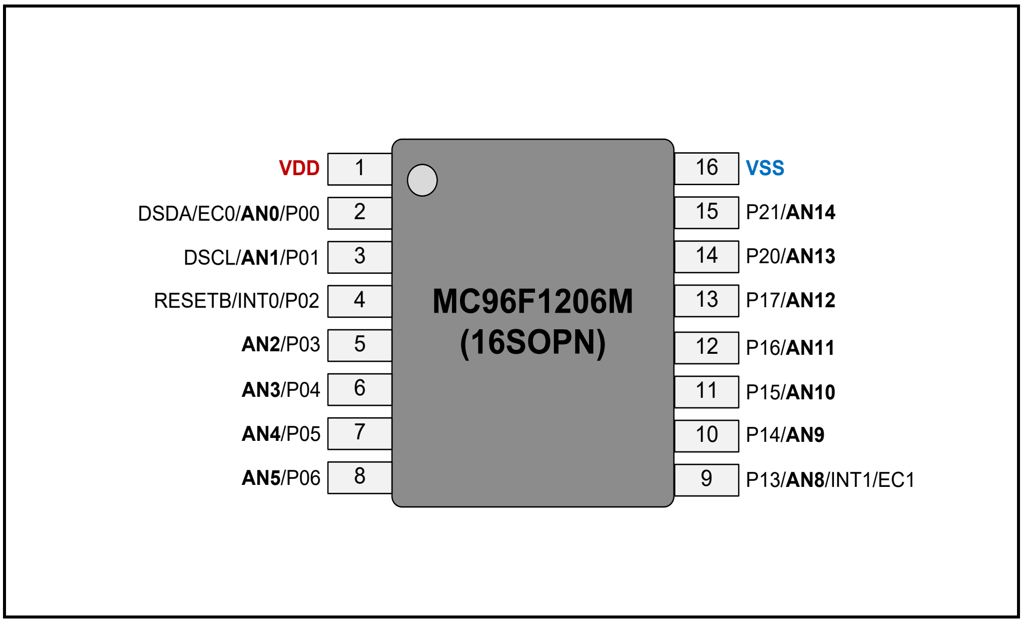
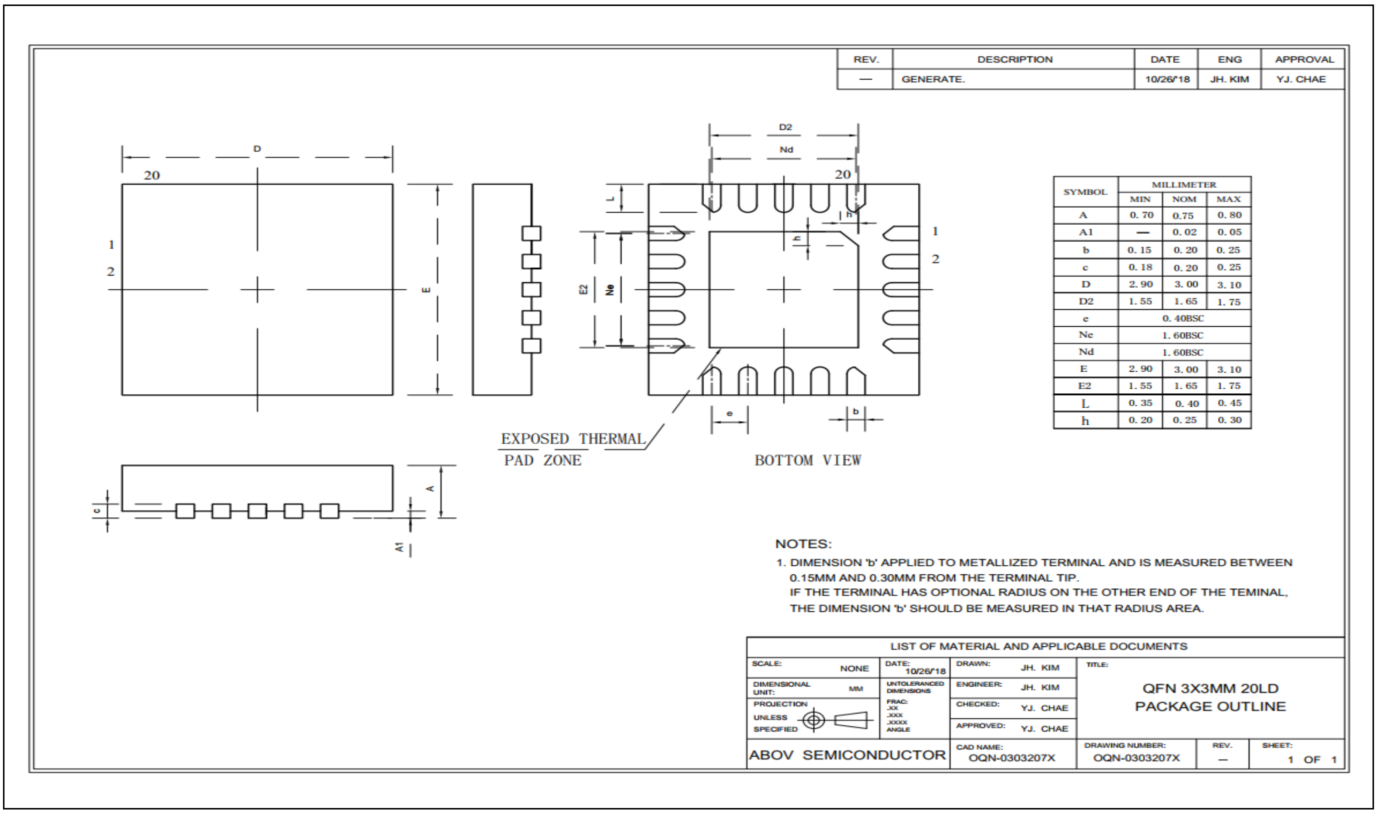


Figure 3.3 MC96F1206 16SOPN assignment

NOTE)

1. The P07, P10-P12 pins should be selected as a push-pull output or an input with pull-up resistor by software control when the 16SOPN package is used.

4 Package Diagram



REV.	DESCRIPTION	DATE	ENG	APPROVAL
—	GENERATE.	10/26/'18	JH. KIM	YJ. CHAE

SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	0. 70	0.75	0. 80
A1	—	0. 02	0. 05
b	0. 15	0. 20	0. 25
c	0. 18	0. 20	0. 25
D	2. 90	3. 00	3. 10
D2	1. 55	1. 65	1. 75
e	0. 40BSC		
Ne	1. 60BSC		
Nd	1. 60BSC		
E	2. 90	3. 00	3. 10
E2	1. 55	1. 65	1. 75
L	0. 35	0. 40	0. 45
h	0. 20	0. 25	0. 30

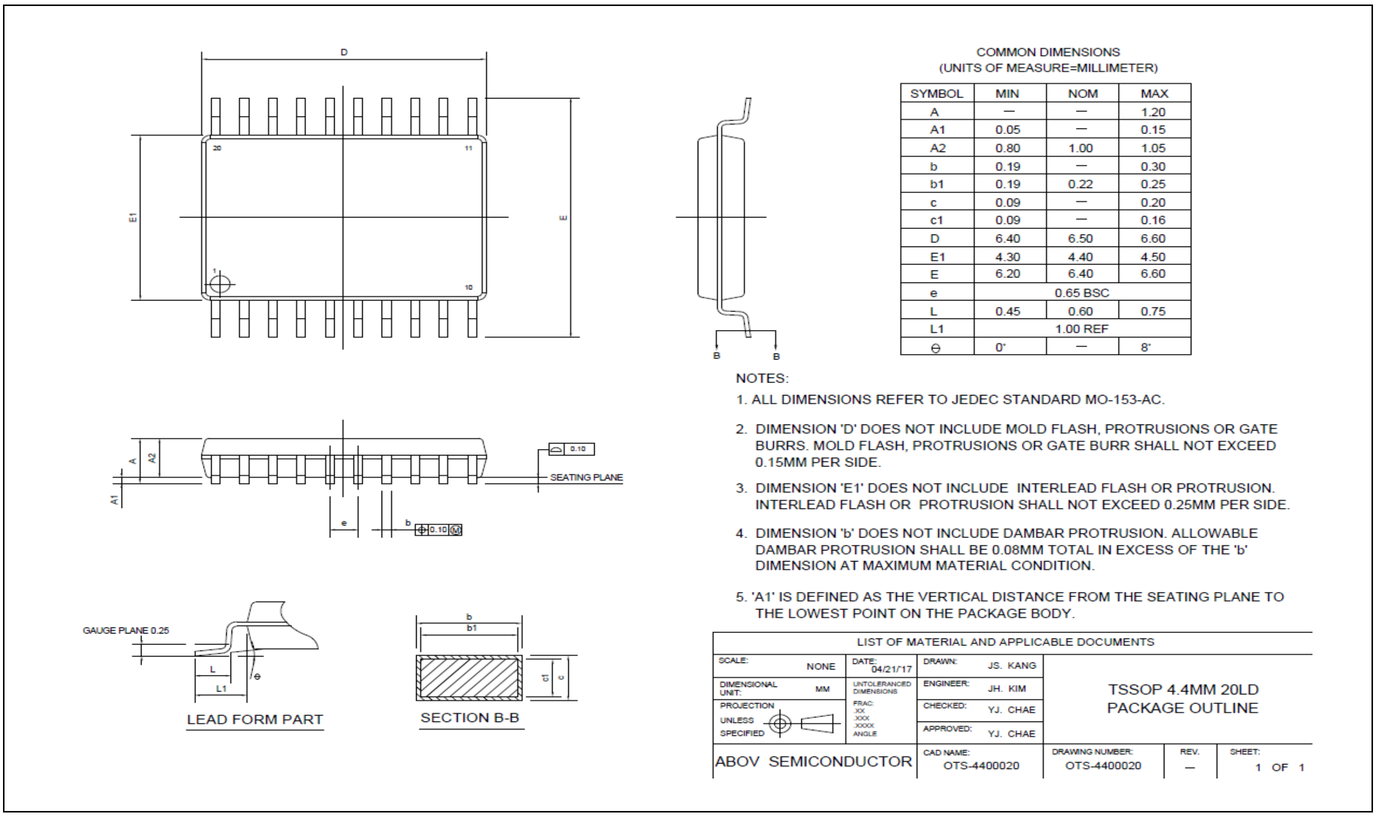
NOTES:

1. DIMENSION 'b' APPLIED TO METALLIZED TERMINAL AND IS MEASURED BETWEEN 0.15MM AND 0.30MM FROM THE TERMINAL TIP.
IF THE TERMINAL HAS OPTIONAL RADIUS ON THE OTHER END OF THE TEMINAL, THE DIMENSION 'b' SHOULD BE MEASURED IN THAT RADIUS AREA.

LIST OF MATERIAL AND APPLICABLE DOCUMENTS

SCALE: NONE	DATE: 10/26/'18	DRAWN: JH. KIM	TITLE: QFN 3X3MM 20LD PACKAGE OUTLINE
DIMENSIONAL UNIT: MM	UNTOLERANCED DIMENSIONS	ENGINEER: JH. KIM	
PROJECTION UNLESS SPECIFIED	FRAC: .XX .XXX .XXXX ANGLE	CHECKED: YJ. CHAE APPROVED: YJ. CHAE	
ABOV SEMICONDUCTOR		CAD NAME: OQN-0303207X	DRAWING NUMBER: OQN-0303207X / REV. — / SHEET: 1 OF 1

Figure 4.1 20 QFN Package



COMMON DIMENSIONS
(UNITS OF MEASURE=MILLIMETER)

SYMBOL	MIN	NOM	MAX
A	—	—	1.20
A1	0.05	—	0.15
A2	0.80	1.00	1.05
b	0.19	—	0.30
b1	0.19	0.22	0.25
c	0.09	—	0.20
c1	0.09	—	0.16
D	6.40	6.50	6.60
E1	4.30	4.40	4.50
E	6.20	6.40	6.60
e	0.65 BSC		
L	0.45	0.60	0.75
L1	1.00 REF		
ϴ	0˚	—	8˚

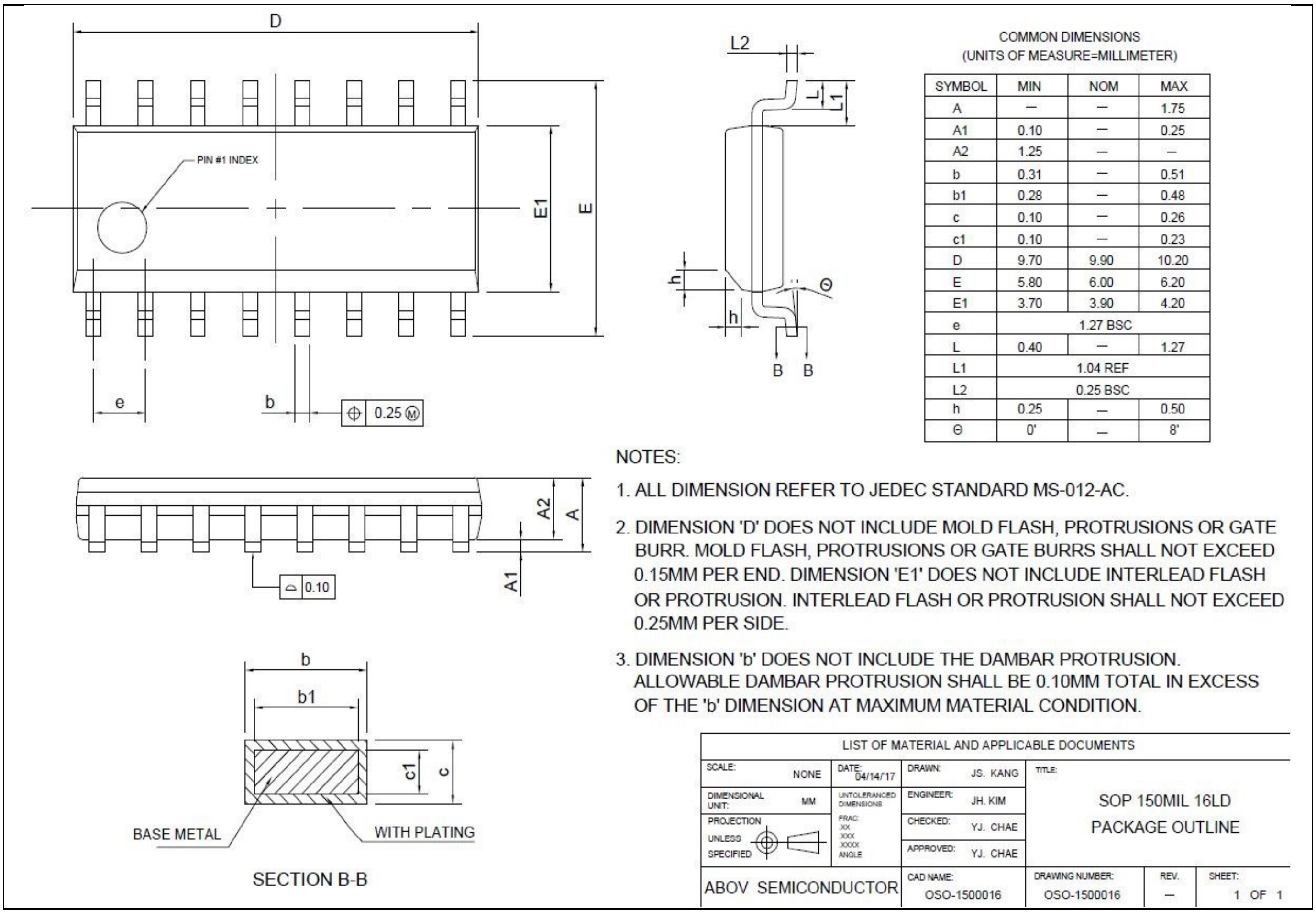
NOTES:

1. ALL DIMENSIONS REFER TO JEDEC STANDARD MO-153-AC.
2. DIMENSION 'D' DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH, PROTRUSIONS OR GATE BURR SHALL NOT EXCEED 0.15MM PER SIDE.
3. DIMENSION 'E1' DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25MM PER SIDE.
4. DIMENSION 'b' DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08MM TOTAL IN EXCESS OF THE 'b' DIMENSION AT MAXIMUM MATERIAL CONDITION.
5. 'A1' IS DEFINED AS THE VERTICAL DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT ON THE PACKAGE BODY.

LIST OF MATERIAL AND APPLICABLE DOCUMENTS

SCALE: NONE	DATE: 04/21/'17	DRAWN: JS. KANG	TSSOP 4.4MM 20LD PACKAGE OUTLINE
DIMENSIONAL UNIT: MM	UNTOLERANCED DIMENSIONS	ENGINEER: JH. KIM	
PROJECTION UNLESS SPECIFIED	FRAC: .XX .XXX .XXXX ANGLE	CHECKED: YJ. CHAE APPROVED: YJ. CHAE	
ABOV SEMICONDUCTOR		CAD NAME: OTS-4400020	DRAWING NUMBER: OTS-4400020 / REV. — / SHEET: 1 OF 1

Figure 4.2 20 TSSOP Package



COMMON DIMENSIONS
(UNITS OF MEASURE=MILLIMETER)

SYMBOL	MIN	NOM	MAX
A	–	–	1.75
A1	0.10	–	0.25
A2	1.25	–	–
b	0.31	–	0.51
b1	0.28	–	0.48
c	0.10	–	0.26
c1	0.10	–	0.23
D	9.70	9.90	10.20
E	5.80	6.00	6.20
E1	3.70	3.90	4.20
e	1.27 BSC		
L	0.40	–	1.27
L1	1.04 REF		
L2	0.25 BSC		
h	0.25	–	0.50
Θ	0'	–	8'

NOTES:

1. ALL DIMENSION REFER TO JEDEC STANDARD MS-012-AC.
2. DIMENSION 'D' DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURR. MOLD FLASH, PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED 0.15MM PER END. DIMENSION 'E1' DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25MM PER SIDE.
3. DIMENSION 'b' DOES NOT INCLUDE THE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.10MM TOTAL IN EXCESS OF THE 'b' DIMENSION AT MAXIMUM MATERIAL CONDITION.

LIST OF MATERIAL AND APPLICABLE DOCUMENTS

SCALE: NONE	DATE: 04/14/'17	DRAWN: JS. KANG	TITLE: SOP 150MIL 16LD PACKAGE OUTLINE
DIMENSIONAL UNIT: MM	UNTOLERANCED DIMENSIONS	ENGINEER: JH. KIM	
PROJECTION UNLESS SPECIFIED	FRAC: .XX .XXX .XXXX ANGLE	CHECKED: YJ. CHAE	
		APPROVED: YJ. CHAE	
ABOV SEMICONDUCTOR		CAD NAME: OSO-1500016	DRAWING NUMBER: OSO-1500016 · REV.: – · SHEET: 1 OF 1

Figure 4.3 16 SOPN Package

5 Pin Description

PIN Name	I/O	Function	@RESET	Shared with
P00	I/O	Port P0 8-bit I/O Port Can be set in input or output mode in 1-bit units Internal pull-up register can be selected by software when this port is used as input port Open Drain enable register can be selected by software when this port is used as output port	Input	AN0/ EC0/ DSDA
P01				AN1/ DSCL
P02				INT0/ RESETB
P03				AN2
P04				AN3/ PWM0/ PWM1
P05				AN4/ PWM0/ PWM1
P06				AN5/ PWM0/ PWM1
P07				AN6/ PWM0/ PWM1
P10	I/O	Port P1 8-bit I/O Port Can be set in input or output mode in 1-bit units Internal pull-up register can be selected by software when this port is used as input port Open Drain enable register can be selected by software when this port is used as output port	Input	AN7
P11				
P12				
P13				AN8/ INT1 / EC1
P14				AN9/ PWM0/ PWM1
P15				AN10/ PWM0/ PWM1
P16				AN11/ PWM0/ PWM1
P17				AN12/ PWM0/ PWM1
P20	I/O	Port P2 2-bit I/O Port Can be set in input or output mode in 1-bit units Internal pull-up register can be selected by software when this port is used as input port Open Drain enable register can be selected by software when this port is used as output port	Input	AN13
P21				AN14
VDD		Power Supply		
VSS		System Ground		

Table 5.1 Pin Description

NOTE) when using ports as PWM0 or PWM1 output port, set corresponding PSRPWM (PWM Port Selection Register. (0xDE)

6 Port Structure

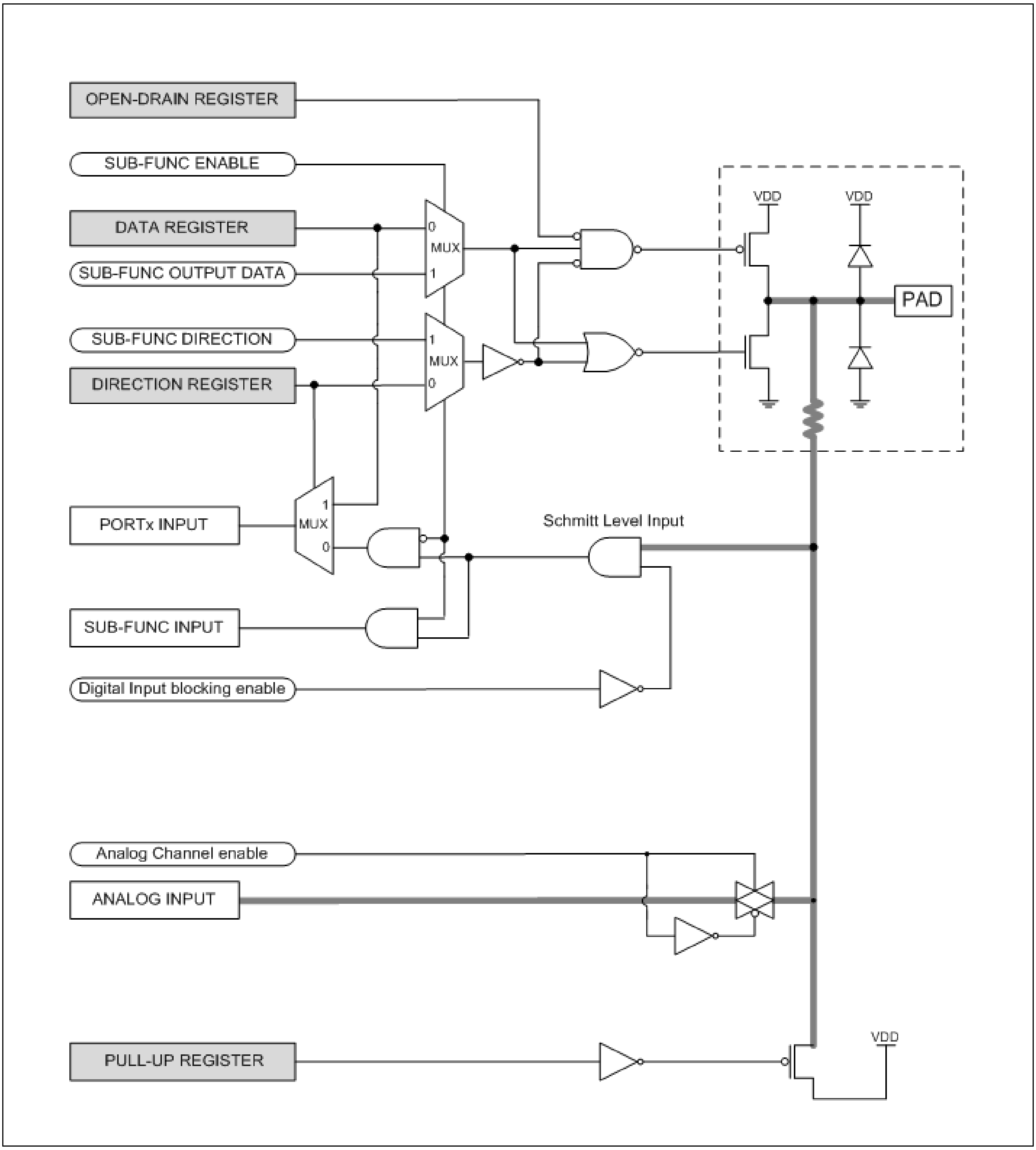


Figure 6.1 Second Function I/O Port

7 Electrical Characteristics

7.1 Absolute Maximum Ratings

Parameter	Symbol	Rating	Unit	Note
Supply Voltage	VDD	-0.3~+6.5	V	–
Normal Voltage Pin	V_I	-0.3~VDD+0.3	V	Voltage on any pin with respect to VSS
	V_O	-0.3~VDD+0.3	V	
	I_{OH}	-15	mA	Maximum current output sourced by (I_{OH} per I/O pin)
	$\sum I_{OH}$	-80	mA	Maximum current ($\sum I_{OH}$)
	I_{OL}	30	mA	Maximum current sunk by (I_{OL} per I/O pin)
	$\sum I_{OL}$	160	mA	Maximum current ($\sum I_{OL}$)
Total Power Dissipation	P_T	400	mW	–
Storage Temperature	T_{STG}	-65~+150	°C	–

Table 7.1 Absolute Maximum Ratings

NOTE) Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

7.2 Recommended Operating Conditions

(T_A=-40°C ~ +85°C)

Parameter	Symbol	Conditions		MIN	TYP	MAX	Unit
Operating Voltage	VDD	f_X= 1, 4, 8, 16MHz	Internal RC	2.2	–	5.5	V
Operating Temperature	T_{OPR}	VDD=2.2~5.5V		-40	–	85	°C

Table 7.2 Recommended Operating Conditions

7.3 A/D Converter Characteristics

(TA=-40℃ ~ +85℃, VDD= 2.2V ~ 5.5V, VSS=0V)

Parameter	Symbol	Conditions	MIN	TYP	MAX	Unit
Resolution	–	–	–-	12	–	bit
Integral Non-Linearity	INL	Analog Reference Voltage = 2.5V ~ 5.5V fx= 8MHz	–	–	±4	LSB
Differential Non-Linearity	DNL		–	–	±1	
Zero Offset Error	ZOE		-3	–	+7	
Full Scale Error	FSE		–	–	±3	
Conversion Time	t_{CON}		–	60	–	Cycle
Analog Input Voltage	V_{AIN}	–	VSS	–	VDD	V
Analog Reference Voltage	VDDREF	NOTE	2.2	–	VDD	V
	LDOREF	–	-	2.5	-	
Analog Input Leakage Current	I_{AIN}	VDDREF=5.12V	–	–	2	uA
ADC Operating Current	I_{ADC}	Enable VDD=5.12V	–	1	2	mA
		Disable	–	–	0.1	uA

Table 7.3 A/D Converter Characteristics

NOTE) When Analog Reference Voltage is lower than 2.5V, the ADC resolution is worse.
ADC zero offset value (-3LSB ~ 7 LSB) is addressed at 0x1868 of option memory. (@ LDOREF)

7.4 Low Drop Out Characteristics

(T_A=-40°C ~ +85°C, VDD=2.7 ~ 5.5V, VSS=0V)

Parameter	Symbol	Condition	MIN	TYP	MAX	Unit
Operating Current	I_{DD}	-	-	-	200	uA
Load Current	I_{LOAD}	-	-	1	-	mA
LDO Output Voltage	V_{LDO}	-40°C ~ 85°C	2.450	2.5	2.550	V
		25°C	2.475	2.5	2.525	V

Table 7.4 Low Drop Out Characteristics

7.5 Power-On Reset Characteristics

(T_A=-40°C ~ +85°C, VDD=2.2 ~ 5.5V, VSS=0V)

Parameter	Symbol	Conditions	MIN	TYP	MAX	Unit
RESET Release Level	V_{POR}	–	0.9	1.1	1.3	V
VDD Voltage Rising Time	t_R	0V to 2.0V	0.05	–	5	V/ms
POR Current	I_{POR}	–	–	0.1	–	uA

Table 7.5 Power-On Reset Characteristics

7.6 Low Voltage Reset and Low Voltage Indicator Characteristics

(T_A=-40°C ~ +85°C, VDD=5.0V, VSS=0V)

Parameter	Symbol	Conditions		MIN	TYP	MAX	Unit
Detection Level	V_{LVR} V_{LVI}	The LVR can select all levels but LVI can select other levels except 1.80V		–	1.80	1.95	V
				1.6	2.1	2.6	
				2.0	2.5	3.0	
				3.0	3.5	4.0	
Hysteresis	△V	–		–	50	-	mV
Minimum Pulse Width	t_{LW}	–		-	500	–	us
LVR and LVI Current	I_{BL}	LVR 1.80V	VDD=5V	–	1	-	uA
		LVR/LVI except 1.80V		–	-	50	

Table 7.6 LVR and LVI Characteristics

NOTE) LVR 1.80V is always ON.

7.7 Internal RC Oscillator Characteristics

(T_A=-40°C ~ +85°C, VDD=2.2V ~ 5.5V, VSS=0V)

Parameter	Symbol	Conditions		MIN	TYP	MAX	Unit
Frequency	f_{IRC}	V_{DD} = 2.2 ~ 5.5V		–	32	–	MHz
Tolerance	–	T_A = 25°C	With 0.1uF Bypass capacitor	–	–	±2.0	%
		T_A = -40°C to +85°C		–	–	±5.0	
Stabilization Time	T_{HFS}	–		–	1	-	ms
IRC Current	I_{IRC}	Enable		–	0.4	–	mA
		Disable		–	–	0.1	uA

Table 7.7 Internal RC Oscillator Characteristics

NOTE) A 0.1uF bypass capacitor should be connected to VDD and VSS.

7.8 Internal WDT Oscillator Characteristics

(T_A=-40°C ~ +85°C, VDD=2.2V ~ 5.5V, VSS=0V)

Parameter	Symbol	Conditions	MIN	TYP	MAX	Unit
Frequency	f_{WDTRC}	–	4	8	12	kHz
Stabilization Time	t_{WDTS}	–	–	1	-	ms
WDTRC Current	I_{WDTRC}	Enable	–	5	–	uA
		Disable	–	–	0.1	

Table 7.8 Internal WDT Oscillator Characteristics

7.9 DC Characteristics

(T_A=-40°C ~ +85°C, VDD=2.2V ~ 5.5V, VSS=0V, f_X=8.0MHz)

Parameter	Symbol	Conditions	MIN	TYP	MAX	Unit
Input High Voltage	V_{IH1}	P0, P1, P2	0.8VDD	–	VDD	V
Input Low Voltage	V_{IL1}	P0, P1, P2	–	–	0.2VDD	V
Output High Voltage	V_{OH1}	VDD=3.3V, I_{OH}=-5mA, All output ports	VDD-1.5	–	–	V
	V_{OH2}	VDD=5V, I_{OH}=-10mA, All output ports	VDD-1.5	–	–	V
Output Low Voltage	V_{OL}	I_{OL}= 20mA,All output ports	–	–	1.0	V
Input High Leakage Current	I_{IH}	All input ports	-1	–	1	uA
Input Low Leakage Current	I_{IL}	All input ports	-1	–	1	uA
Pull-Up Resistor	R_{PU1}	V_I=0V, T_A= 25°C All Input ports	25	50	100	kΩ
Supply Current	I_{DD1} (RUN)	Run Mode, f_X=8 MHz	-	3	5	mA
	I_{IDD2} (IDLE)	IDLE Mode, f_X=8 MHz	-	2	5	mA
	I_{DD3} (STOP1)	STOP1 Mode, WDTRC Enable	-	2	35	uA
	I_{DD4} (STOP2)	STOP2 Mode, WDTRC Disable	-	1.5	30	uA

Table 7.9 DC Characteristics

NOTE) STOP1: WDT only running, STOP2: All function disable.

7.10 AC Characteristics

(T_A= -40°C ~ +85°C, VDD=2.2V ~ 5.5V)

Parameter	Symbol	Conditions	MIN	TYP	MAX	Unit
RESETB input low width	t_{RST}	Input, VDD=5V	-	500	–	us
Interrupt input high, low width	t_{IWH}, t_{IWL}	All interrupt, VDD=5V	125	–	–	ns
External Counter Input High, Low Pulse Width	t_{ECWH}, t_{ECWL}	ECn, VDD=5V (n=0, 1)	125	–	–	ns
External Counter Transition Time	t_{REC}, t_{FEC}	ECn, VDD=5V (n=0, 1)	-	–	20	ns

Table 7.10 AC Characteristics

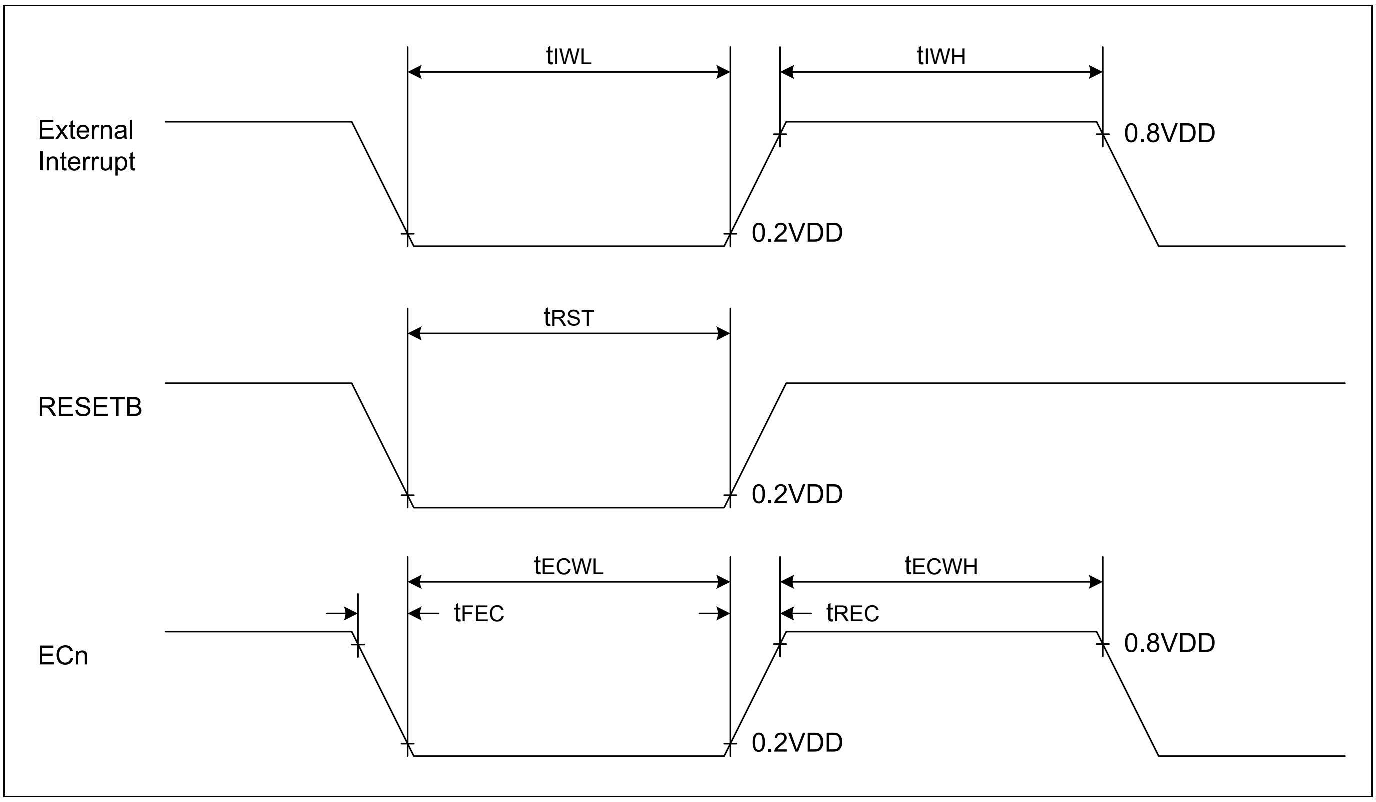


Figure 7.1 AC Timing

7.11 Operating Voltage Range

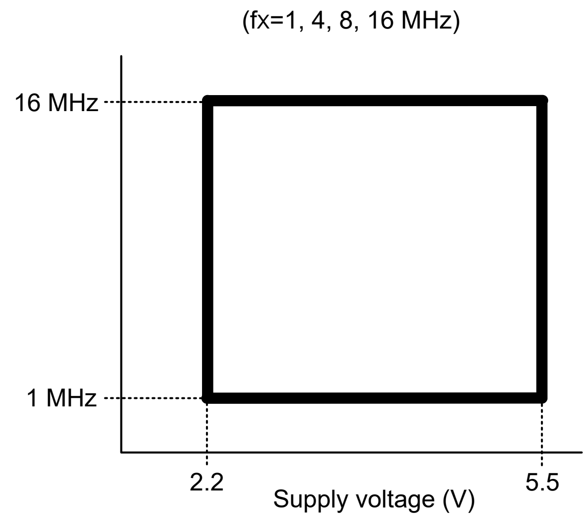


Figure 7.2 Operating Voltage Range

7.12 Typical Characteristics

These graphs and tables provided in this section are for design guidance only and are not tested or guaranteed. In some graphs or tables the data presented are outside specified operating range (e.g. outside specified VDD range). This is for information only and devices are guaranteed to operate properly only within the specified range.

The data presented in this section is a statistical summary of data collected on units from different lots over a period of time. “Typical” represents the mean of the distribution while “max” or “min” represents (mean + 3σ) and (mean - 3σ) respectively where σ is standard deviation.

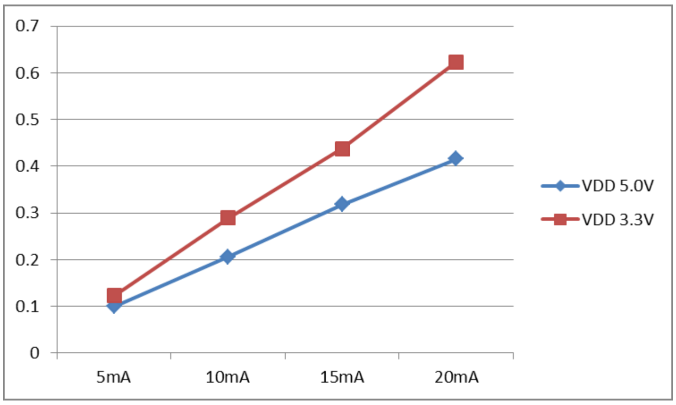


Figure 7.3 Output Low Voltage (V_{OL})

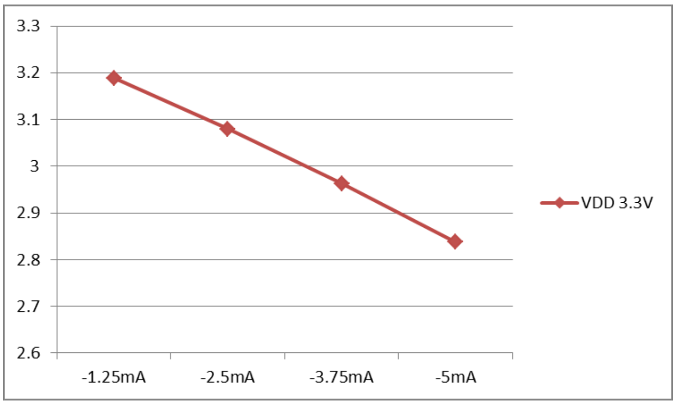


Figure 7.4 Output High Voltage (V_{OH1})

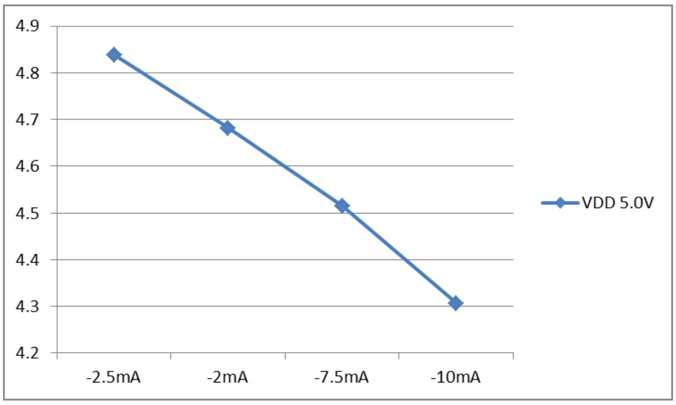


Figure 7.5 Output High Voltage (V_{OH2})

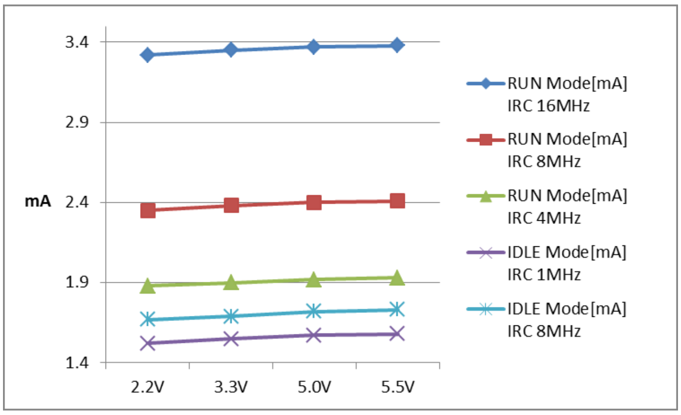


Figure 7.6 Power Supply Current (RUN, IDLE)

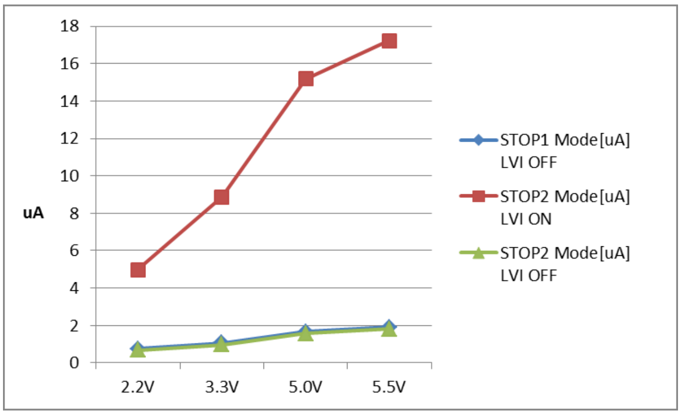


Figure 7.7 Power Supply Current (STOP1, STOP2)

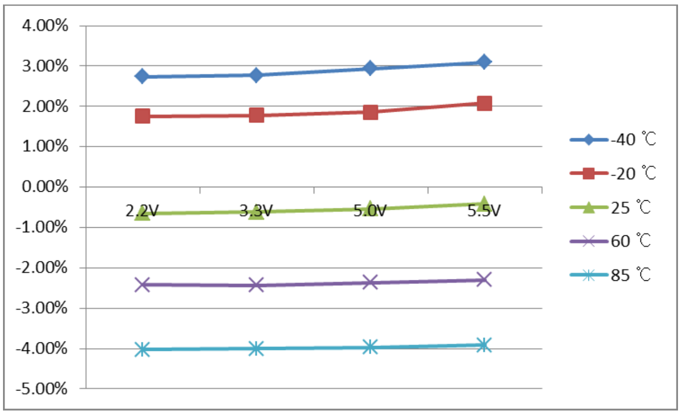


Figure 7.8 IRC Tolerance

7.13 Recommended Application Circuit

For the microprocessor and other devices in the system to function correctly, it is also necessary to monitor the supply voltage during operations. Voltage drops or glitches on the power supply lines, can cause unwanted changes in the internal registers, which can lead to instructions being incorrectly executed, incorrect output signals and errors in the operations results. If noise is applied to the VDD rising slope due to external factors during the POR, the microprocessor may malfunction because the microprocessor continues to operate and does not recognize that the voltage has fallen below the threshold due to the internal RC time constants. Therefore, VDD / GND requires a power capacitor for VDD drop and a decoupling capacitor for high frequency noise. Normally, electrolytic / tantalum capacitors of 10uf / 9V or more are recommended for power capacitors and multilayer ceramic capacitors of 0.1uF or more are recommended for decoupling capacitors. Decoupling capacitors should be placed as close as possible to the microprocessor.

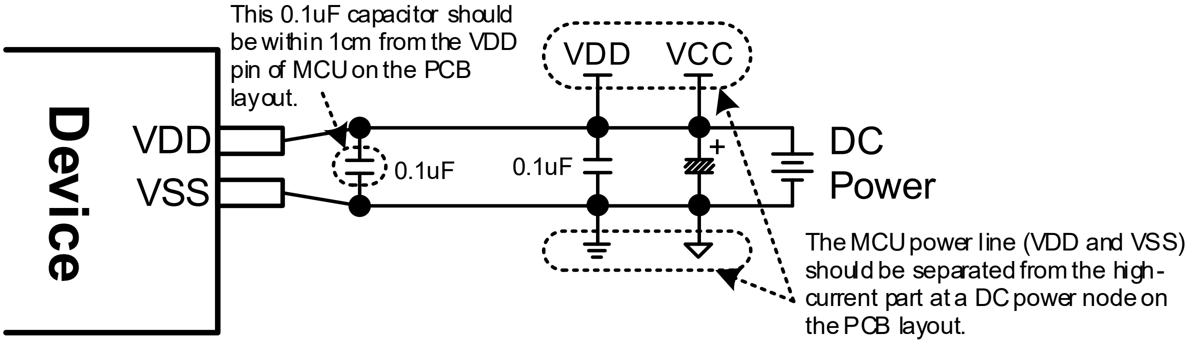

This 0.1uF capacitor should be within 1cm from the VDD pin of MCU on the PCB layout.
Device
VDD
VSS
0.1uF
0.1uF
VDD
VCC
+
DC
Power
The MCU power line (VDD and VSS) should be separated from the high-current part at a DC power node on the PCB layout.

Figure 7.9 Recommended Power Circuit part when using DC Power.

8 Memory

The MC96F1206 addresses two separate address memory stores: Program memory and Data memory. The logical separation of Program and Data memory allows Data memory to be accessed by 8-bit addresses, which can be more quickly stored and manipulated by 8-bit CPU. Nevertheless, 16-bit Data memory addresses can also be generated through the DPTR register.

Program memory can only be read, not written to. There can be up to 64Kbytes of Program memory. In the MC96F1206 FLASH version of these devices the 6 Kbytes of Program memory are provided on-chip. Data memory can be read and written to up to 256 bytes internal memory (DATA) including the stack area.

8.1 Program Memory

A 16-bit program counter is capable of addressing up to 64Kbytes, but this device has just 6 Kbytes as program memory space.

0 shows a map of the lower part of the program memory. After reset, the CPU begins execution from address 0000H. Each interrupt is assigned to a fixed address in program memory. The interrupt causes the CPU to jump to that addressed, where it commences execution of the service routine. External interrupt 0, for example, is assigned to address 0003H. If external interrupt 0 would be requested, its service routine must begin at location 0003H. When the interrupt is not used, the ROM address is used as general purpose program memory. If an interrupt service routine is short enough (as is often the case in control applications), it can reside entirely within that 8-byte interval. Longer service routines can use a jump instruction to skip over subsequent interrupt locations, if other interrupts are in use.

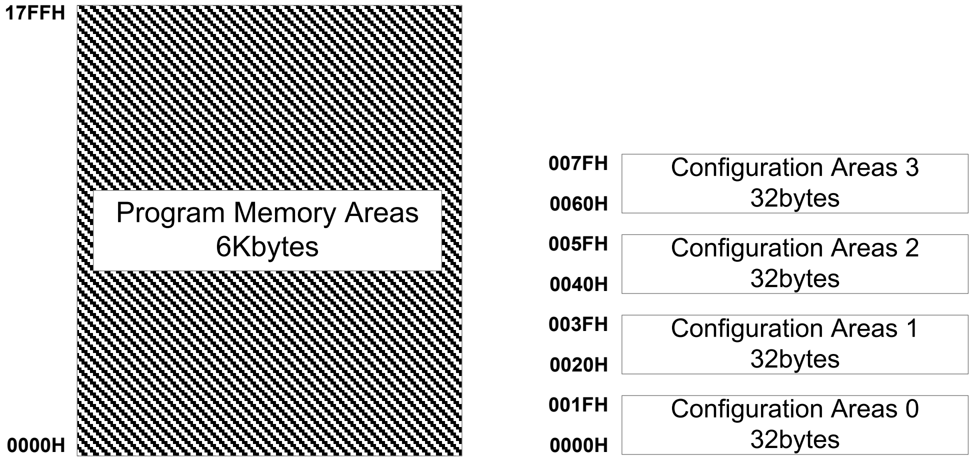


Figure 8.1 Program Memory

- User Function Mode: 6 Kbytes Included Interrupt Vector Region
- Non-volatile and reprogramming memory: Flash memory based on EEPROM cell

8.2 Data Memory

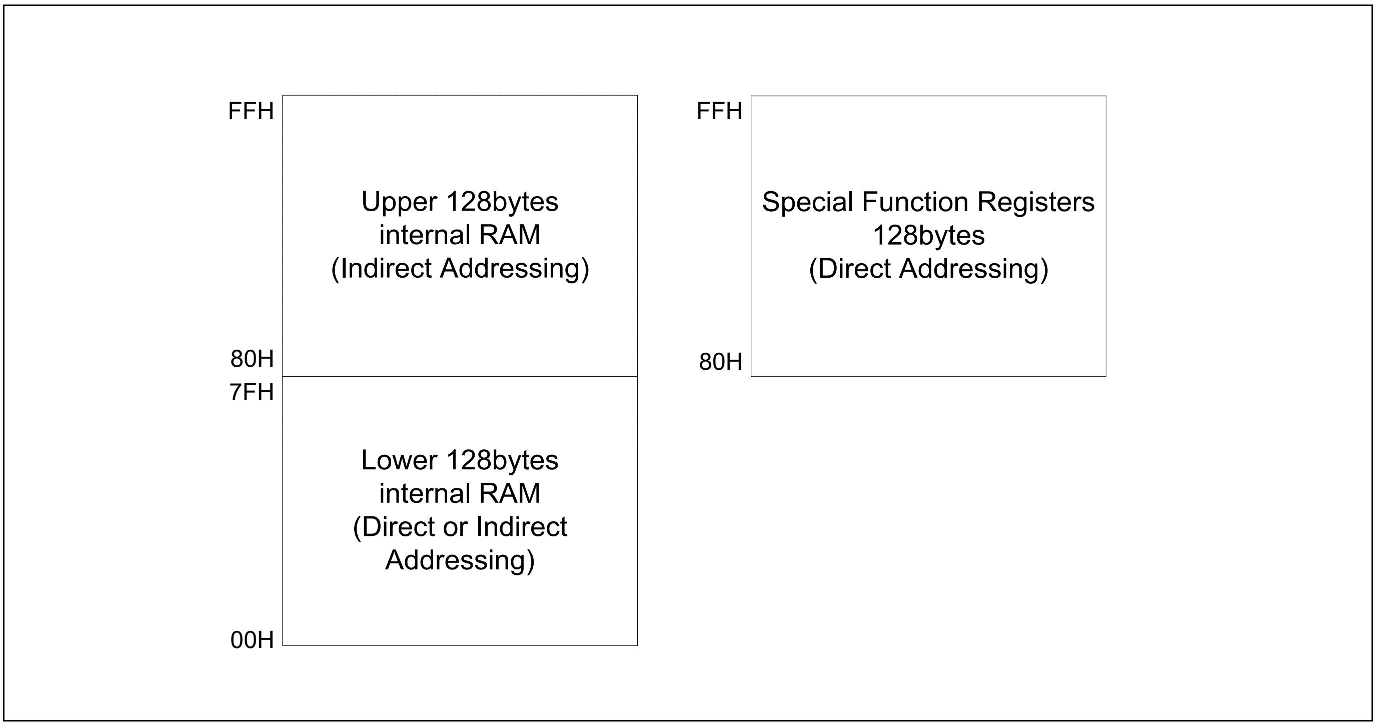


Figure 8.2 Data Memory Map

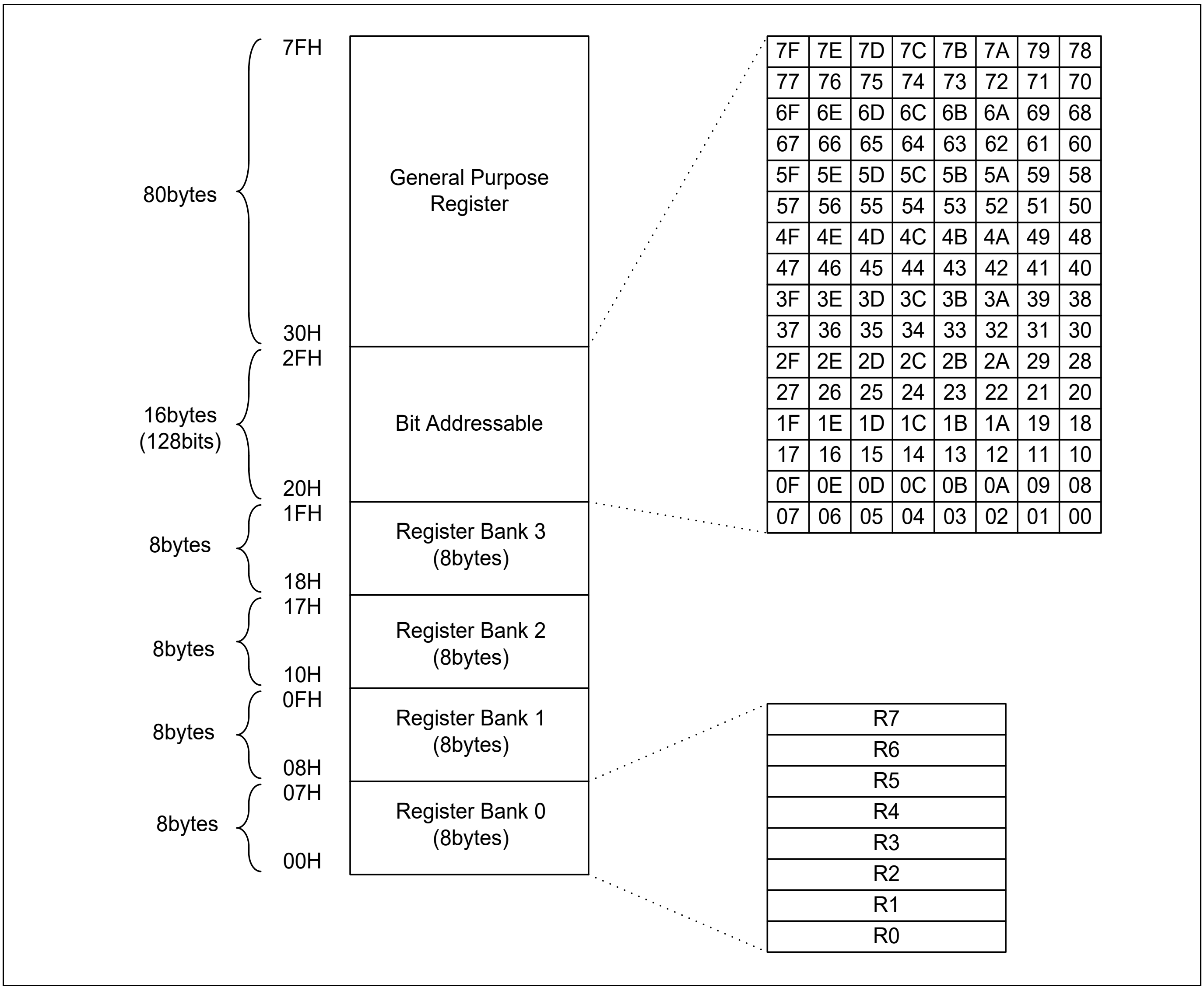
The internal data memory space is divided into two blocks, which are generally referred to as the lower 128 bytes, upper 128 bytes and SFR space.

Internal Data memory addresses are always one byte wide, which implies an address space of only 256bytes. However, the addressing modes for internal RAM can in fact accommodate 384 bytes, using a simple trick. Direct addresses higher than 7FH access one memory space and indirect addresses higher than 7FH access a different memory space. Thus 0 shows the upper 128 and SFR space occupying the same block of addresses, 80H through FFH, although they are physically separate entities.

The lower 128 bytes of RAM are present in all 8051 devices as mapped in 0. The lowest 32 bytes are grouped into 4 banks of 8 registers. Program instructions call out these registers as R0 through R7. Two bits in the Program Status Word select which register bank is in use. This allows more efficient use of code space, since register instructions are shorter than instructions that use direct addressing.

The next 16 bytes above the register banks form a block of bit-addressable memory space. The 8051 instruction set includes a wide selection of single-bit instructions, and the 128 bits in this area can be directly addressed by these instructions. The bit addresses in this area are 00H through 7FH.

All of the bytes in the lower 128 bytes can be accessed by either direct or indirect addressing. These spaces are used for data RAM and stack. The upper 128bytes RAM can only be accessed by indirect addressing.



7F	7E	7D	7C	7B	7A	79	78
77	76	75	74	73	72	71	70
6F	6E	6D	6C	6B	6A	69	68
67	66	65	64	63	62	61	60
5F	5E	5D	5C	5B	5A	59	58
57	56	55	54	53	52	51	50
4F	4E	4D	4C	4B	4A	49	48
47	46	45	44	43	42	41	40
3F	3E	3D	3C	3B	3A	39	38
37	36	35	34	33	32	31	30
2F	2E	2D	2C	2B	2A	29	28
27	26	25	24	23	22	21	20
1F	1E	1D	1C	1B	1A	19	18
17	16	15	14	13	12	11	10
0F	0E	0D	0C	0B	0A	09	08
07	06	05	04	03	02	01	00

Figure 8.3 Lower 128 bytes RAM

8.3 SFR Map

8.3.1 SFR Map Summary

	0H/8H	1H/9H	2H/AH	3H/BH	4H/CH	5H/DH	6H/EH	7H/FH
F8H	IP1							
F0H	B		FEARL	FEARM	FEARH			
E8H			FEMR	FECR	FESR	FETCR		
E0H	ACC	P2PU						
D8H		P1PU	PSR0		PSR2	PSR3	PSRPWM	
D0H	PSW	P0PU						
C8H								
C0H		P2OD						
B8H	IP	P1OD	T1CR	T1CR1	PWM1DRL C1R1L / T1L	PWM1DRH CDR1H / T1H	PWM1PRL T1DRL	PWM1PRH T1DRH
B0H		P0OD	T0CR	T0CR1	PWM0DRL CDR0L / T0L	PWM0DRH CDR0H / T0H	PWM0PRL T0DRL	PWM0PRH T0DRH
A8H	IE	IE1						
A0H		LDOCR	EO	EIENAB	EIFLAG	EIEDGE	EIPOLA	EIBOTH
98H		P2IO						PCI1
90H	P2	P1IO			ADCM1	ADCM	ADCRL	ADCRH
88H	P1	P0IO	SCCR	BCCR	BITR	WDTMR	WDTR /WDTCR	LVIR
80H	P0	SP	DPL	DPH	DPL1	DPH1	RSFR	PCON

Table 8.1 SFR Map Summary

NOTE) the registers of which lower 3-bit address are 000 are bit-addressable

8.3.2 8051 Compiler Compatible SFR

ACC (Accumulator) : E0H

7	6	5	4	3	2	1	0
ACC							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Initial value : 00H

ACC Accumulator

B (B Register) : F0H

7	6	5	4	3	2	1	0
B							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Initial value : 00H

B B Register

SP (Stack Pointer) : 81H

7	6	5	4	3	2	1	0
SP							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Initial value : 07H

SP	Stack Pointer

DPL (Data Pointer Low Byte) : 82H

7	6	5	4	3	2	1	0
DPL							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Initial value : 00H

DPL	Data Pointer Low Byte

DPH (Data Pointer High Byte) : 83H

7	6	5	4	3	2	1	0
DPH							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Initial value : 00H

DPH	Data Pointer High Byte

DPL1 (Data Pointer1 Low Byte) : 84H

7	6	5	4	3	2	1	0
DPL1							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Initial value : 00H

DPL1	Data Pointer1 Low Byte

DPH1 (Data Pointer1 High Byte) : 85H

7	6	5	4	3	2	1	0
DPH1							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Initial value : 00H

DPH1	Data Pointer1 High Byte

PSW (Program Status Word) : D0H

7	6	5	4	3	2	1	0
CY	AC	F0	RS1	RS0	OV	F1	P
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Initial value : 00H

CY	Carry Flag
AC	Auxiliary Carry Flag
F0	General Purpose User-Definable Flag
RS1	Register Bank Select bit 1
RS0	Register Bank Select bit 0
OV	Overflow Flag
F1	User-Definable Flag
P	Parity Flag. Set/cleared by hardware each instruction cycle to indicate an odd/even number of ‘1’ bits in the accumulator

EO (Extended Operation Register) : A2H

7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	DPSEL.0
R	R	R	R/W	R	R	R	R/W

Initial value : 00H

DPSEL	Select Banked Data Point Register	
	0	DPTR = {DPH, DPL}
	1	DPTR1 = {DPH1, DPL1}

9 I/O Ports

9.1 I/O Ports

The MC96F1206 has eighteen I/O ports (P0, P1 and P2). Each port can be easily configured by software as I/O pin, internal pull up and open drain pin to meet various system configurations and design requirements. Also P1 includes function that can generate interrupt according to change of state of the pin.

9.2 Port Register

9.2.1 Data Register (Px)

Data Register is a bidirectional I/O port. If ports are configured as output ports, data can be written to the corresponding bit of the Px. If ports are configured as input ports, the data can be read from the corresponding bit of the Px.

9.2.2 Direction Register (PxIO)

Each I/O pin can independently used as an input or an output through the PxIO register. Bits cleared in this read/write register will select the corresponding pin in Px to become an input, setting a bit sets the pin to output. All bits are cleared by a system reset.

9.2.3 Pull-up Resistor Selection Register (PxPU)

The on-chip pull-up resistor can be connected to them in 1-bit units with a pull-up resistor selection register (PxPU). The pull-up register selection controls the pull-up resister enable/disable of each port. When the corresponding bit is 1, the pull-up resister of the pin is enabled. When 0, the pull-up resister is disabled. All bits are cleared by a system reset.

9.2.4 Open-drain Selection Register (PxOD)

There is internally open-drain selection register (PxOD). The open-drain selection register controls the open-drain enable/disable of each port. Ports become push-pull by a system reset.

9.2.5 Pin Change Interrupt Enable Register (PCI)

The P1 can support Pin Change Interrupt function. Pin Change Interrupts PCI will trigger if any enabled P1[7:0] pin toggles. The PCI Register control which pins contribute to the pin change interrupts.

9.2.6 Register Map

Name	Address	Dir	Default	Description
P0	80H	R/W	00H	P0 Data Register
P0IO	89H	R/W	00H	P0 Direction Register
P0PU	D1H	R/W	00H	P0 Pull-up Resistor Selection Register
P0OD	B1H	R/W	00H	P0 Open-drain Selection Register
P1	88H	R/W	00H	P1 Data Register
P1IO	91H	R/W	00H	P1 Direction Register
P1PU	D9H	R/W	00H	P1 Pull-up Resistor Selection Register
P1OD	B9H	R/W	00H	P1 O1pen-drain Selection Register
P2	90H	R/W	00H	P2 Data Register
P2IO	99H	R/W	00H	P2 Direction Register
P2PU	E1H	R/W	00H	P2 Pull-up Resistor Selection Register
P2OD	C1H	R/W	00H	P2 Open-drain Selection Register
PCI1	9FH	R/W	00H	Pin change interrupt enable register
PSR0	DAH	R/W	00H	Port Debounce selection register
PSR2	DCH	R/W	00H	P0 Function Selection Register
PSR3	DDH	R/W	00H	P1, P2 Function Selection Register
PSRPWM	DEH	R/W	00H	PWM Port Select Register

Table 9.1 Register Map

9.3 Px Port

9.3.1 Px Port Description

Px is 8-bit I/O port. Px control registers consist of Data register (Px), direction register (PxIO), pull-up register selection register (PxPU), open-drain selection register (PxOD), pin change interrupt register (PCI).

9.3.2 Register description for P0

P0 (P0 Data Register) : 80H

7	6	5	4	3	2	1	0
P07	P06	P05	P04	P03	P02	P01	P00
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Initial value : 00H

P0[7:0]	I/O Data

P0IO (P0 Direction Register) : 89H

7	6	5	4	3	2	1	0
P07IO	P06IO	P05IO	P04IO	P03IO	P02IO	P01IO	P00IO
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Initial value : 00H

P0IO[7:0]	P0 data I/O direction.	
	0	Input
	1	Output

P0PU (P0 Pull-up Resistor Selection Register) : D1H

7	6	5	4	3	2	1	0
P07PU	P06PU	P05PU	P04PU	P03PU	P02PU	P01PU	P00PU
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Initial value : 00H

P0PU[7:0]	Configure pull-up resistor of P0 port	
	0	Disable
	1	Enable

P0OD (P0 Open-drain Selection Register) : B1H

7	6	5	4	3	2	1	0
P07OD	P06OD	P05OD	P04OD	P03OD	P02OD	P01OD	P00OD
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Initial value : 00H

P0OD[7:0]	Configure open-drain of P0 port	
	0	Disable
	1	Enable

9.3.3 Register description for P1

P1 (P1 Data Register) : 88H

7	6	5	4	3	2	1	0
P17	P16	P15	P14	P13	P12	P11	P10
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Initial value : 00H

P1[7:0]	I/O Data

P1IO (P1 Direction Register) : 91H

7	6	5	4	3	2	1	0
P17IO	P16IO	P15IO	P14IO	P13IO	P12IO	P11IO	P10IO
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Initial value : 00H

P1IO[7:0]	P1 data I/O direction.	
	0	Input
	1	Output

P1PU (P1 Pull-up Resistor Selection Register) : D9H

7	6	5	4	3	2	1	0
P17PU	P16PU	P15PU	P14PU	P13PU	P12PU	P11PU	P10PU
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Initial value : 00H

P1PU[7:0]	Configure pull-up resistor of P1 port	
	0	Disable
	1	Enable

P1OD (P1 Open-drain Selection Register) : B9H

7	6	5	4	3	2	1	0
P17OD	P16OD	P15OD	P14OD	P13OD	P12OD	P11OD	P10OD
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Initial value : 00H

P1OD[7:0]	Configure open-drain of P1 port	
	0	Disable
	1	Enable

9.3.4 Register description for P2

P2 (P2 Data Register) : 90H

7	6	5	4	3	2	1	0
-	-	-	-	-	-	P21	P20
-	-	-	-	-	-	R/W	R/W

Initial value : 00H

P2[1:0] I/O Data

P2IO (P2 Direction Register) : 99H

7	6	5	4	3	2	1	0
-	-	-	-	-	-	P21IO	P20IO
-	-	-	-	-	-	R/W	R/W

Initial value : 00H

P2IO[1:0] P2 data I/O direction.

0 Input

1 Output

P2PU (P2 Pull-up Resistor Selection Register) : E1H

7	6	5	4	3	2	1	0
-	-	-	-	-	-	P21PU	P20PU
-	-	-	-	-	-	R/W	R/W

Initial value : 00H

P2PU[1:0] Configure pull-up resistor of P2 port

0 Disable

1 Enable

P2OD (P2 Open-drain Selection Register) : C1H

7	6	5	4	3	2	1	0
-	-	-	-	-	-	P21OD	P20OD
-	-	-	-	-	-	R/W	R/W

Initial value : 00H

P2OD[1:0] Configure open-drain of P2 port

0 Disable

1 Enable

PCI1 (Pin Change Interrupt Register) : 9FH

7	6	5	4	3	2	1	0
PCI17	PCI16	PCI15	PCI14	PCI13	PCI12	PCI11	PCI10
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Initial value : 00H

PCI[7:0] Select PCI interrupt enable or disable of P1x

0 Disable

1 Enable

PSR0 (Port Debounce selection register) : DAH

7	6	5	4	3	2	1	0
-	-	-	-	-	-	PSR01	PSR00
-	-	-	-	-	-	R/W	R/W

Initial value : 00H

PSR01	P13 Port Debounce Enable Register	
	0	disable
	1	enable (about 500us fix)
PSR00	P02 Port Debounce Enable Register	
	0	disable
	1	enable (about 500us fix)

NOTE) Before you use MCU STOP1/2 mode, you must disable P02, P13 debounce.

PSR2 (P0, P1, P2 Port Selection Register) : DCH

7	6	5	4	3	2	1	0
PSR27	PSR26	PSR25	PSR24	PSR23	PSR22	PSR21	PSR20
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Initial value : 00H

PSR27	P10 Port Selection Register	
	0	P10
	1	AN7
PSR26	P07 Port Selection Register	
	0	P07
	1	AN6
PSR25	P06 Port Selection Register	
	0	P06
	1	AN5
PSR24	P05 Port Selection Register	
	0	P05
	1	AN4
PSR23	P04 Port Selection Register	
	0	P04
	1	AN3
PSR22	P03 Port Selection Register	
	0	P03
	1	AN2
PSR21	P01 Port Selection Register	
	0	P01
	1	AN1
PSR20	P00 Port Selection Register	
	0	P00
	1	AN0

PSR3 (P1, P2 Port Selection Register) : DDH

7	6	5	4	3	2	1	0
-	PSR36	PSR35	PSR34	PSR33	PSR32	PSR31	PSR30
-	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Initial value : 00H

PSR36	P21 Port Selection Register	
	0	P21
	1	AN14
PSR35	P20 Port Selection Register	
	0	P20
	1	AN13
PSR34	P17 Port Selection Register	
	0	P17
	1	AN12
PSR33	P16 Port Selection Register	
	0	P16
	1	AN11
PSR32	P15 Port Selection Register	
	0	P15
	1	AN10
PSR31	P14 Port Selection Register	
	0	P14
	1	AN9
PSR30	P13 Port Selection Register	
	0	P13
	1	AN8

PSRPWM (PWM Port Selection Register) : DEH

7	6	5	4	3	2	1	0
-	PSRPWM6	PSRPWM5	PSRPWM4	-	PSRPWM2	PSRPWM1	PSRPWM0
-	R/W	R/W	R/W	-	R/W	R/W	R/W

Initial value : 00H

PSRPWM[6:4] PWM1 Ports Selection Register

0	PWM1 out to P04(default)
1	PWM1 out to P05
2	PWM1 out to P06
3	PWM1 out to P07
4	PWM1 out to P14
5	PWM1 out to P15
6	PWM1 out to P16
7	PWM1 out to P17

PSRPWM[2:0] PWM0 Ports Selection Register

0	PWM0 out to P04(default)
1	PWM0 out to P05
2	PWM0 out to P06
3	PWM0 out to P07
4	PWM0 out to P14
5	PWM0 out to P15
6	PWM0 out to P16
7	PWM0 out to P17

NOTE) When using ports as PWM0 and PWM1 output port (PSRPWM=0x00), PWM0 is preferentially operated.

10 Interrupt Controller

10.1 Overview

The MC96F1206 supports up to 9 interrupt sources. The interrupts have separate enable register bits associated with them, allowing software control. They can also have four levels of priority assigned to them. The interrupt controller has following features:

- receive the request from 9 interrupt source
- 6 group priority
- 4 priority levels
- Multi Interrupt possibility
- If the requests of different priority levels are received simultaneously, the request of higher priority level is serviced
- Each interrupt source can control by EA bit and each IEx bit
- Interrupt latency: 5~8 machine cycles in single interrupt system

The maskable interrupts are enabled through five pair of interrupt enable registers (IE, IE1). Bits of IE, IE1 register each individually enable/disable a particular interrupt source. Overall control is provided by bit 7 of IE (EA). When EA is set to ‘0’, all interrupts are disabled: when EA is set to ‘1’, interrupts are individually enabled or disabled through the other bits of the interrupt enable registers. The MC96F1206 supports a four-level priority scheme. Each maskable interrupt is individually assigned to one of three priority levels by writing to IP or IP1.

Priority sets two bit which is to IP and IP1 register about group. If two requests of different priority levels are received simultaneously, the request of higher priority level is serviced. If the request of same or lower priority level is received, that request is not serviced.

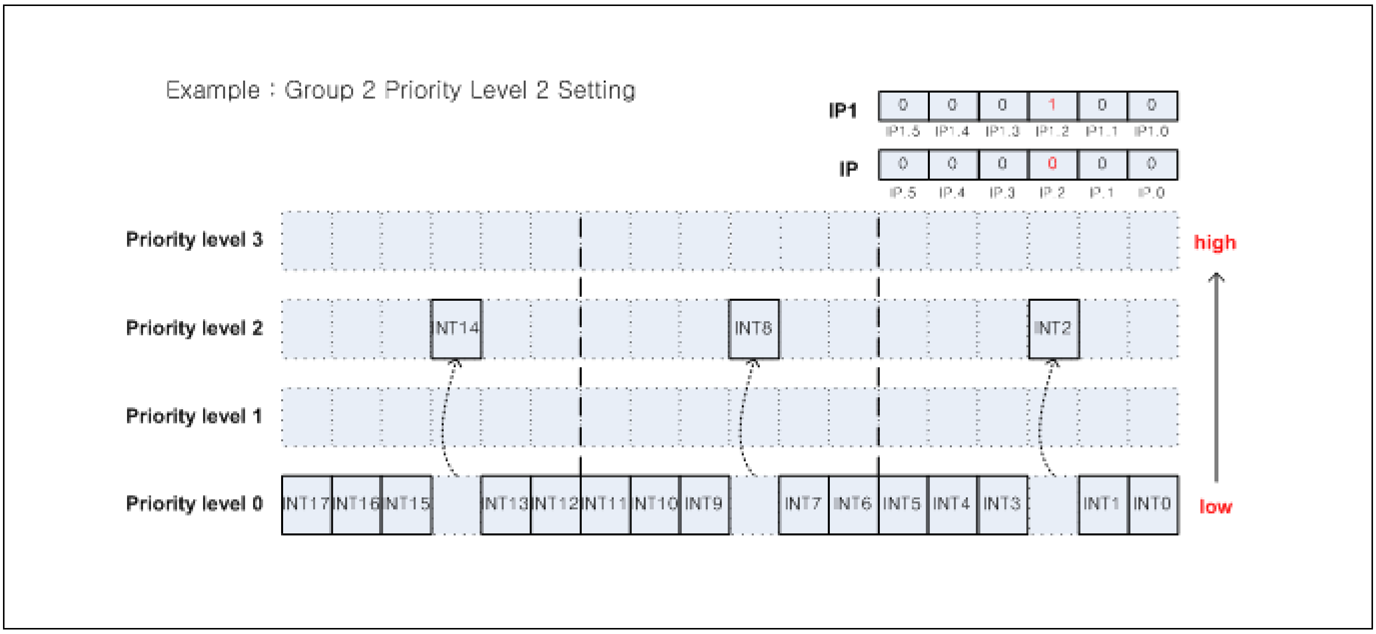

Example : Group 2 Priority Level 2 Setting
IP1
0 0 0 1 0 0
IP1.5 IP1.4 IP1.3 IP1.2 IP1.1 IP1.0
IP
0 0 0 0 0 0
IP.5 IP.4 IP.3 IP.2 IP.1 IP.0
Priority level 3
Priority level 2
Priority level 1
Priority level 0
INT14
INT8
INT2
INT17 INT16 INT15 INT13 INT12 INT11 INT10 INT9 INT7 INT6 INT5 INT4 INT3 INT1 INT0
high
low

Figure 10.1 Interrupt Group Priority Level

10.2 Pin Change Interrupt

The pin change interrupt on P1 ports receive the both edge (Falling-edge and Rising-edge) interrupt request as shown in Figure 10.2. Also each pin change interrupt source has enable setting bits. The FLAG (flag register) register provides the status of ports change interrupts.

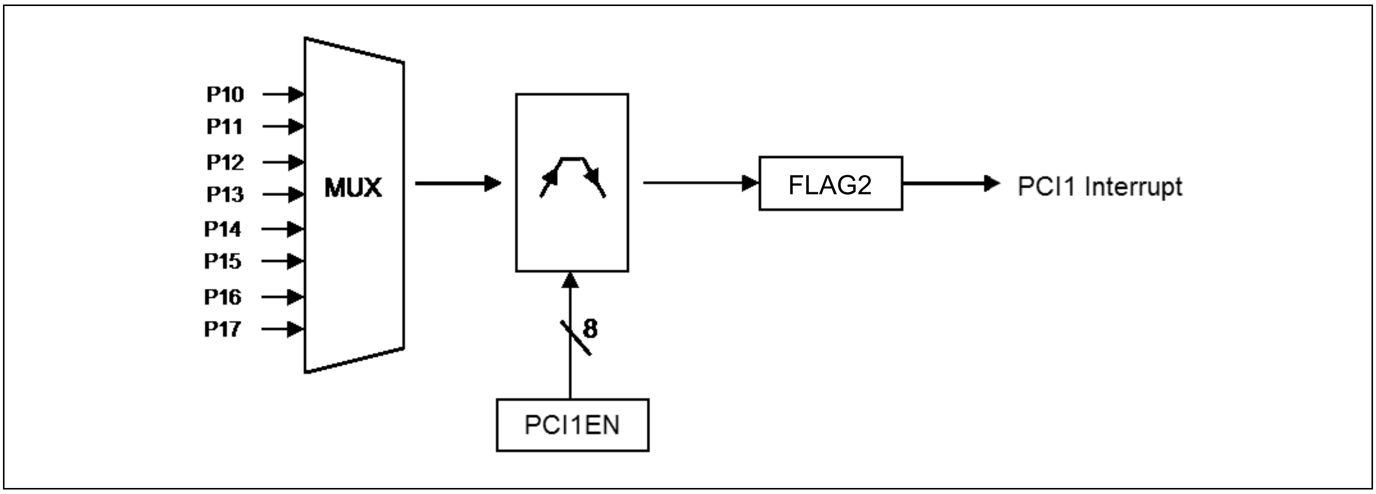


Figure 10.2 External Interrupt Description

10.3 Block Diagram

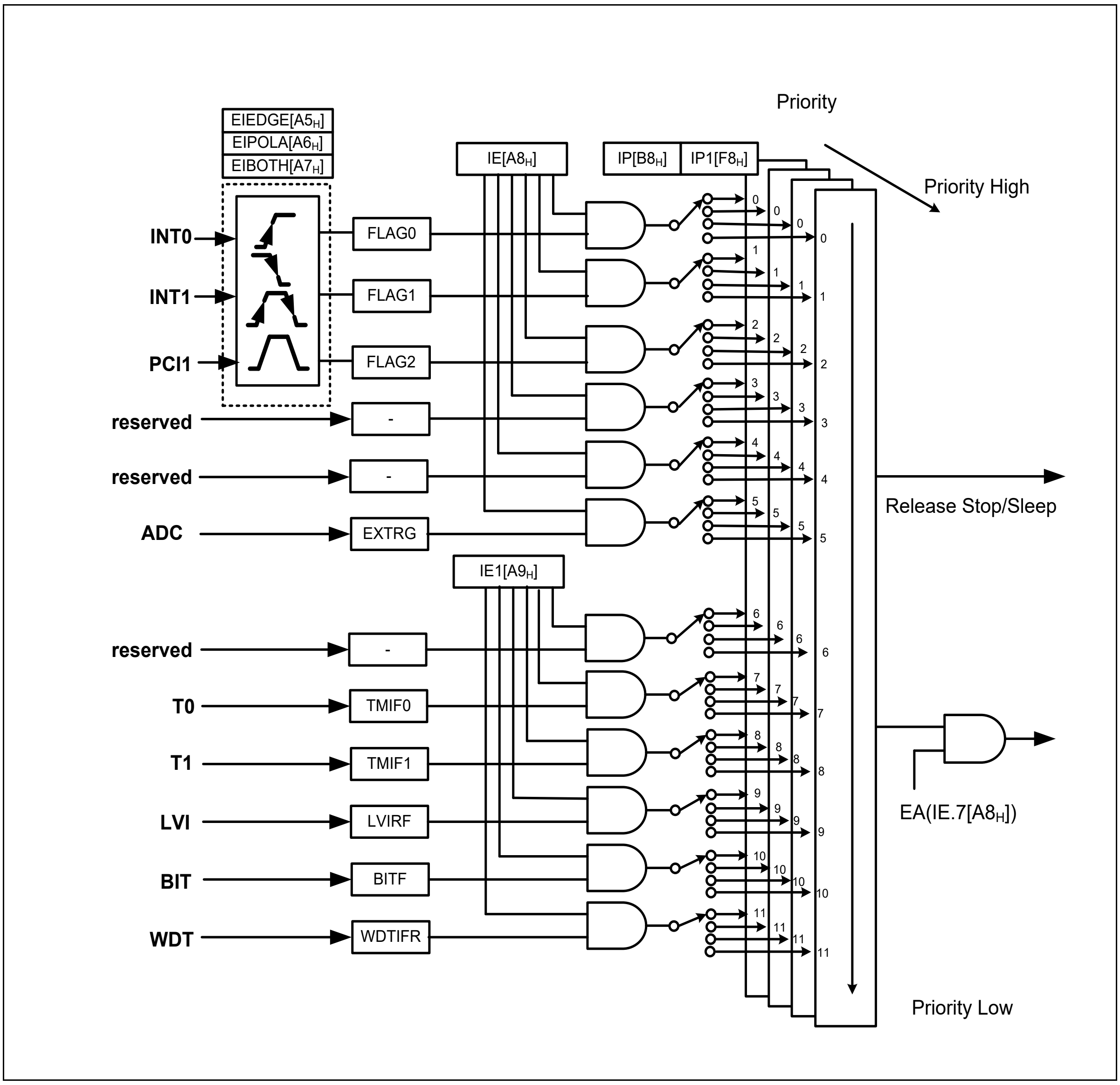


Figure 10.3 Block Diagram of Interrupt

10.4 Interrupt Vector Table

The interrupt controller supports 9 interrupt sources as shown in the Table 10.1 below. When interrupt becomes service, long call instruction (LCALL) is executed in the vector address. Interrupt request 9 has a decided priority order.

Interrupt Source	Symbol	Interrupt Enable bit	Priority	Mask	Vector Address
Hardware Reset	RESETB	0	0	Non-Maskable	0000H
External Interrupt 0	INT0	IE.0	1	Maskable	0003H
External Interrupt 1	INT1	IE.1	2	Maskable	000BH
PCI	INT2	IE.2	3	Maskable	0013H
-	INT3	IE.3	4	Maskable	001BH
-	INT4	IE.4	5	Maskable	0023H
ADC	INT5	IE.5	6	Maskable	002BH
-	INT6	IE.6	7	Maskable	0033H
TIMER 0	INT7	IE1.1	8	Maskable	003BH
TIMER 1	INT8	IE1.2	9	Maskable	0043H
LVI	INT9	IE1.3	10	Maskable	004BH
BIT	INT10	IE1.4	11	Maskable	0053H
WDT	INT11	IE1.5	12	Maskable	005BH

Table 10.1 Interrupt Vector Address Table

For maskable interrupt execution, first EA bit must set ‘1’ and specific interrupt source must set ‘1’ by writing a ‘1’ to associated bit in the IEx. If interrupt request is received, specific interrupt request flag set ‘1’. And it remains ‘1’ until CPU accepts interrupt. After that, interrupt request flag will be cleared automatically.

10.5 Interrupt Sequence

An interrupt request is held until the interrupt is accepted or the interrupt latch is cleared to '0' by a reset or an instruction. Interrupt acceptance always generates at last cycle of the instruction. So instead of fetching the current instruction, CPU executes internally LCALL instruction and saves the PC stack. For the interrupt service routine, the interrupt controller gives the address of LJMP instruction to CPU. After finishing the current instruction, at the next instruction to go interrupt service routine needs 5~8 machine cycle and the interrupt service task is terminated upon execution of an interrupt return instruction [RETI]. After generating interrupt, to go to interrupt service routine, the following process is progressed.

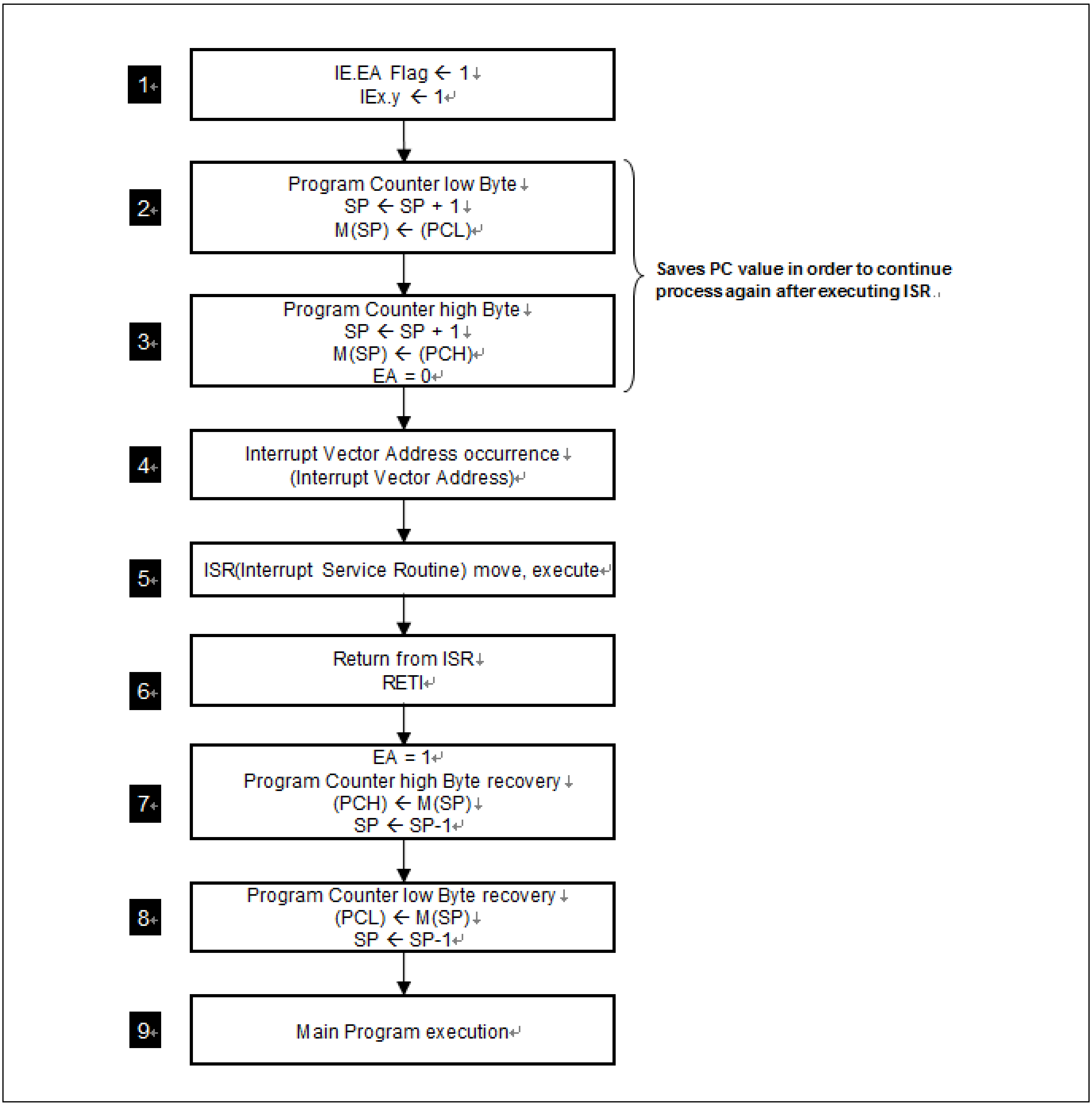
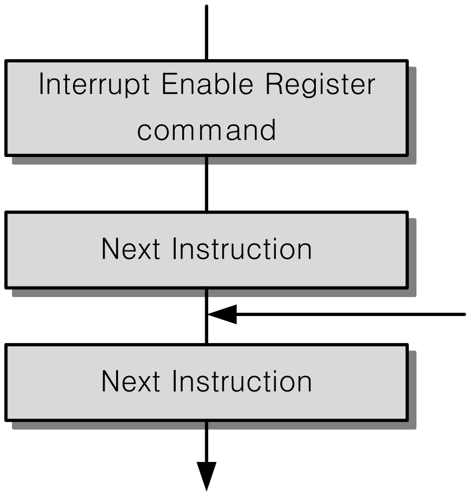

1
IE.EA Flag ← 1
IEx.y ← 1
2
Program Counter low Byte
SP ← SP + 1
M(SP) ← (PCL)
3
Program Counter high Byte
SP ← SP + 1
M(SP) ← (PCH)
EA = 0
Saves PC value in order to continue process again after executing ISR.
4
Interrupt Vector Address occurrence
(Interrupt Vector Address)
5
ISR(Interrupt Service Routine) move, execute
6
Return from ISR
RETI
7
EA = 1
Program Counter high Byte recovery
(PCH) ← M(SP)
SP ← SP-1
8
Program Counter low Byte recovery
(PCL) ← M(SP)
SP ← SP-1
9
Main Program execution

Figure 10.4 Interrupt Execution Flow

10.6 Effective Timing after Controlling Interrupt bit



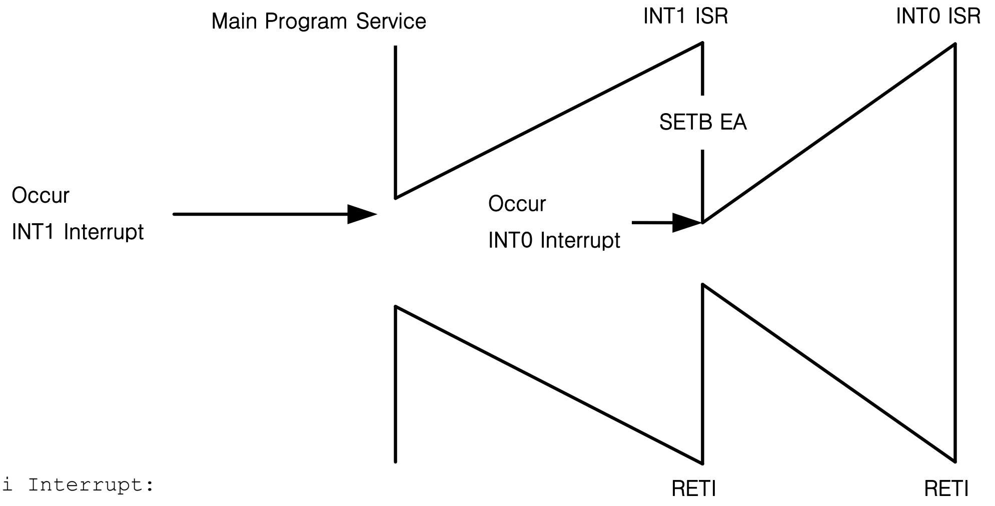
Setting both EA bit and individual interrupt enable bit INTnE makes the pending interrupt active after executing the next instruction.

Figure 10.5 Interrupt Enable Register effective Timing

10.7 Multi Interrupt

If two requests of different priority levels are received simultaneously, the request of higher priority level is serviced. At this time, an interrupt polling sequence determines which request is serviced by hardware. However, multiple processing through software for special features is possible.

Following example is shown to service INT0 routine during INT1 routine in 0. In this example, INT0 interrupt priority is higher than INT1 interrupt priority. If some interrupt is lower than INT1 priority, it can't service its interrupt service routine.



```
Example) Software Multi Interrupt:

INT1 : MOV   IE, #03H  ; Enable INT0 only
       SETB  EA        ; Enable global interrupt (necessary for multi interrupt)
       ...
       RETI
```

Figure 10.6 Execution of Multi Interrupt

10.8 Interrupt Enable Accept Timing

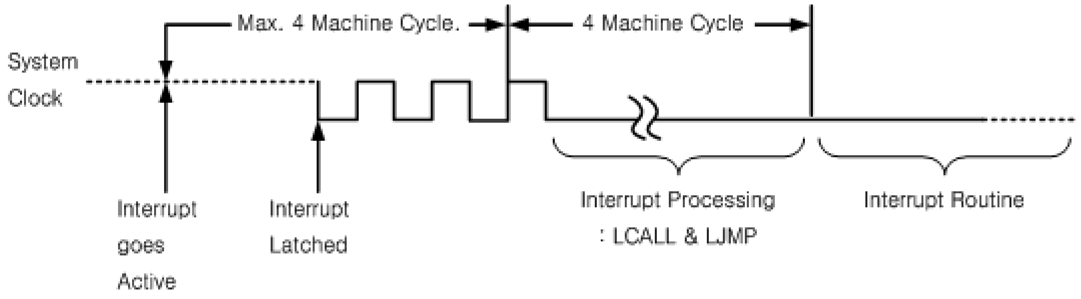


Figure 10.7 Interrupt Response Timing Diagram

10.9 Interrupt Service Routine Address

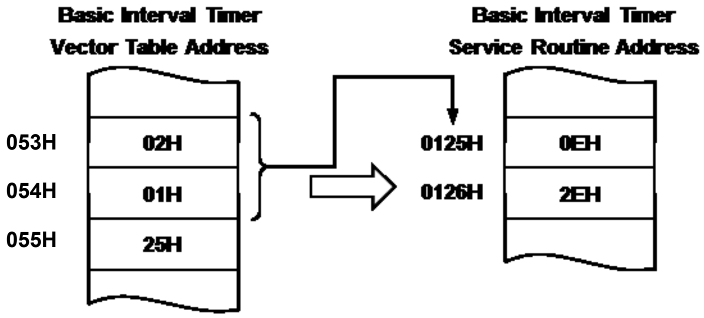
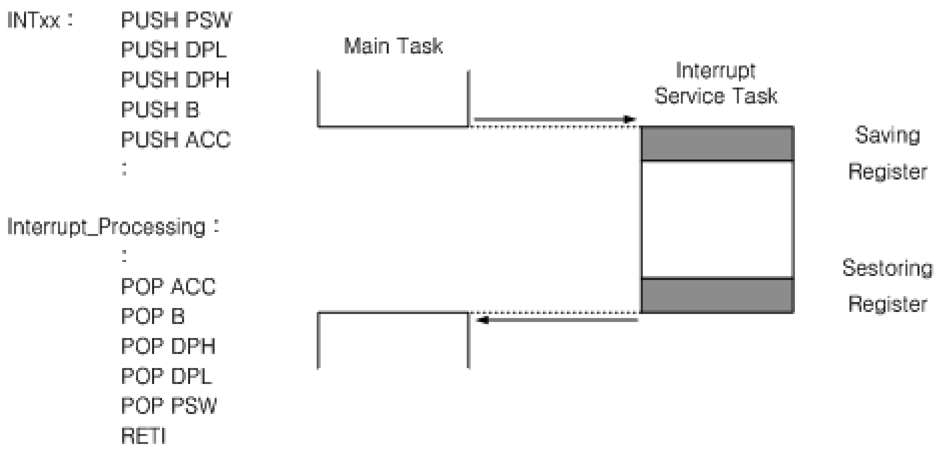

Basic Interval Timer Vector Table Address
Basic Interval Timer Service Routine Address
053H
02H
054H
01H
055H
25H
0125H
0EH
0126H
2EH

Figure 10.8 Correspondence between Vector Table Address and the Entry Address of ISR

10.10 Saving/Restore General-Purpose Registers



```
INTxx :    PUSH PSW
           PUSH DPL
           PUSH DPH
           PUSH B
           PUSH ACC
           :

Interrupt_Processing :
           :
           POP ACC
           POP B
           POP DPH
           POP DPL
           POP PSW
           RETI
```

Figure 10.9 Saving/Restore Process Diagram and Sample Source

10.11 Interrupt Timing

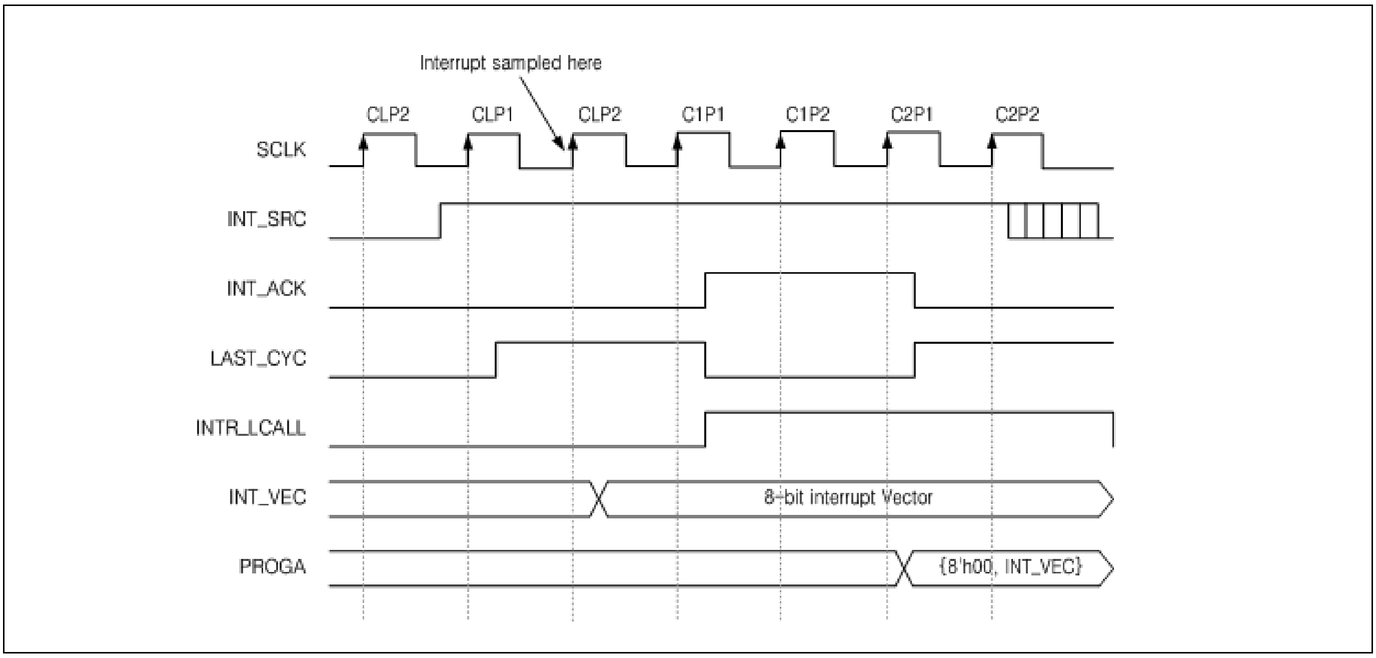


Figure 10.10 Timing Chart of Interrupt Acceptance and Interrupt Return Instruction

Interrupt source sampled at last cycle of the command. When sampling interrupt source, it is decided to low 8-bit of interrupt vector. M8051 core makes interrupt acknowledge at first cycle of command, executes long call to jump interrupt routine as INT_VEC.

NOTE) command cycle CLPx : L=Last cycle, 1=1st cycle or 1st phase, 2=2nd cycle or 2nd phase

10.12 External Interrupt

The external interrupt on INT0, INT1pins receive various interrupt request depending on the edge selection register EIEDGE (External Interrupt Edge register) and EIPOLA (External Interrupt Polarity register) as shown in Figure 10.11. Also each external interrupt source has control setting bits. The EIFLAG (External interrupt flag register) register provides the status of external interrupts.

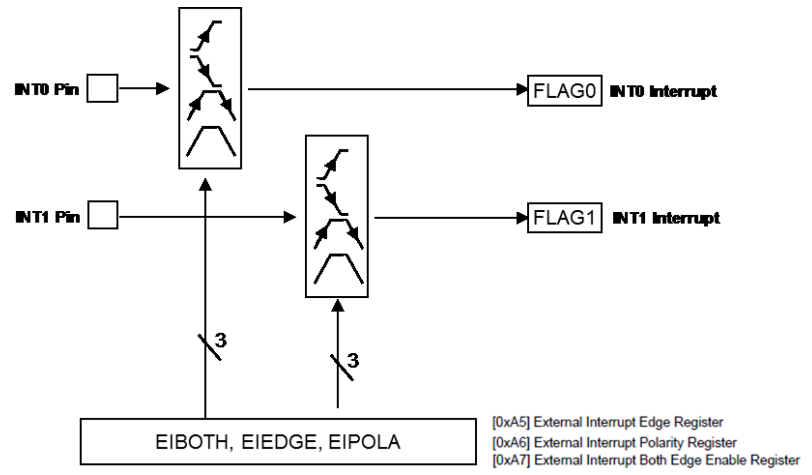

INT0 Pin
FLAG0
INT0 Interrupt
INT1 Pin
FLAG1
INT1 Interrupt
3
3
EIBOTH, EIEDGE, EIPOLA
[0xA5] External Interrupt Edge Register
[0xA6] External Interrupt Polarity Register
[0xA7] External Interrupt Both Edge Enable Register

Figure 10.11 External Interrupt Description

10.13 Interrupt Register Overview

10.13.1 Interrupt Enable Register (IE, IE1)

Interrupt enable register consists of Global interrupt control bit (EA) and peripheral interrupt control bits. Totally 32 peripheral are able to control interrupt.

10.13.2 Interrupt Priority Register (IP, IP1)

The 32 interrupt divides 8 groups which have each 4 interrupt sources. A group can decide 4 levels interrupt priority using interrupt priority register. Level 3 is the high priority, while level 0 is the low priority. Initially, IP, IP1 reset value is '0'. At that initialization, low interrupt number has a higher priority than high interrupt number. If decided the priority, low interrupt number has a higher priority than high interrupt number in that group.

10.13.3 Register Map

Name	Address	Dir	Default	Description
IE	A8H	R/W	00H	Interrupt Enable Register
IE1	A9H	R/W	00H	Interrupt Enable Register 1
IP	B8H	R/W	00H	Interrupt Priority Register
IP1	F8H	R/W	00H	Interrupt Priority Register 1
EIENAB	A3H	R/W	00H	Interrupt Enable Register
EIFLAG	A4H	R/W	00H	Interrupt Flag Register
EIEDGE	A5H	R/W	00H	Interrupt Edge Register
EIPOLA	A6H	R/W	00H	Interrupt Polarity Register
EIBOTH	A7H	R/W	00H	Interrupt Both Edge Register

Table 10.2 Register Map

10.14 Interrupt Register Description

The Interrupt Register is used for controlling interrupt functions. Also it has External interrupt control registers. The interrupt register consists of Interrupt Enable Register (IE), Interrupt Enable Register 1 (IE1), Interrupt Priority Register (IP), Interrupt Priority Register 1 (IP1), P1 Pin Change Interrupt Enable Register (PCI1).

The pin change interrupt on P1 ports receive the both edge (Falling edge and Rising edge) interrupt request.

10.14.1 Register Description for Interrupt

IE (Interrupt Enable Register) : A8H

7	6	5	4	3	2	1	0
EA	-	INT5E	-	-	INT2E	INT1E	INT0E
R/W	-	R/W	-	-	R/W	R/W	R/W

Initial value : 00H

EA	Enable or disable all interrupt bits	
	0	All Interrupt disable
	1	All Interrupt enable
INT5E	Enable or disable ADC Interrupt	
	0	ADC interrupt Disable
	1	ADC interrupt Enable
INT2E	Enable or disable Pin Change Interrupt	
	0	Pin Change Interrupt Disable
	1	Pin Change Interrupt Enable
INT1E	Enable or disable External Interrupt 1	
	0	External interrupt 1 Disable
	1	External interrupt 1 Enable
INT0E	Enable or disable External Interrupt 0	
	0	External interrupt 0 Disable
	1	External interrupt 0 Enable

IE1 (Interrupt Enable Register 1) : A9H

7	6	5	4	3	2	1	0
-	-	INT11E	INT10E	INT9E	INT8E	INT7E	-
-	-	R/W	R/W	R/W	R/W	R/W	-

Initial value : 00H

INT11E	Enable or disable WDT Interrupt		
	0	WDT interrupt Disable	
	1	WDT interrupt Enable	
INT10E	Enable or disable BIT Interrupt		
	0	BIT interrupt Disable	
	1	BIT interrupt Enable	
INT9E	Enable or disable LVI Interrupt		
	0	LVI interrupt Disable	
	1	LVI interrupt Enable	
INT8E	Enable or disable Timer 1 Interrupt		
	0	Timer1 interrupt Disable	
	1	Timer1 interrupt Enable	
INT7E	Enable or disable Timer 0 Interrupt		
	0	Timer0 interrupt Disable	
	1	Timer0 interrupt Enable	

IP (Interrupt Priority Register) :B8H

7	6	5	4	3	2	1	0
-	-	IP5	IP4	IP3	IP2	IP1	IP0
-	-	R/W	R/W	R/W	R/W	R/W	R/W

Initial value : 00H

IP1 (Interrupt Priority Register High) :F8H

7	6	5	4	3	2	1	0
-	-	IPH5	IPH4	IPH3	IPH2	IPH1	IPH0
-	-	R/W	R/W	R/W	R/W	R/W	R/W

Initial value : 00H

IP[5:0], IPH[5:0]

Select Interrupt Priority.
Each IPH and IP corresponds to INT5~INT0.

IPH	IP	Description
0	0	level 0 (lowest)
0	1	level 1
1	0	level 2
1	1	level 3 (highest)

EIENAB (External Interrupt Enable Register) : A3H

7	6	5	4	3	2	1	0
-	-	-	-	-	-	ENAB1	ENAB0
-	-	-	-	-	-	R/W	R/W

Initial value: 0H

ENAB1 Enable or Disable External Interrupt 1

0 Disable External Interrupt 1(default)

1 Enable External Interrupt 1

ENAB0 Enable or Disable External Interrupt 0

0 Disable External Interrupt 0(default)

1 Enable External Interrupt 0

EIFLAG (External Interrupt Flag Register) : A4H

7	6	5	4	3	2	1	0
-	-	-	-	-	FLAG2	FLAG1	FLAG0
-	-	-	-	-	R/W	R/W	R/W

Initial value: 0H

If External Interrupt is occurred, the flag becomes ‘1’. The flag can be cleared by writing a ‘0’ to bit. It is also cleared automatically after interrupt service routine is served.

FLAG2 When Pin Change Interrupt is occurred this bit is set.

0 Pin Change Interrupt is not occurred

1 Pin Change Interrupt is occurred

FLAG1 When External Interrupt 1 is occurred this bit is set.

0 External Interrupt 1 is not occurred

1 External Interrupt 1 is occurred

FLAG0 When External Interrupt 0 is occurred this bit is set.

0 External Interrupt 0 is not occurred

1 External Interrupt 0 is occurred

EIEDGE (External Interrupt Edge Register) : A5H

7	6	5	4	3	2	1	0
-	-	–	-	-	-	EDGE1	EDGE0
-	-	-	-	-	-	R/W	R/W

Initial value : 0H

EDGE1 Determines the type of External interrupt 1, edge or level sensitive.

0 Level (default)

1 Edge

EDGE0 Determines the type of External interrupt 0, edge or level sensitive.

0 Level (default)

1 Edge

EIPOLA (External Interrupt Polarity Register) : A6H

7	6	5	4	3	2	1	0
-	-	-	-	-	-	POLA1	POLA0
-	-	-	-	-	-	R/W	R/W

Initial value: 0H

According to EIEDGE, this register acts differently. If EIEDGE is level type, external interrupt polarity have level value. If EIEDGE is edge type, external interrupt polarity have edge value.

POLA1 Determine the polarity of External Interrupt 1

0	When High level or rising edge, Interrupt occur(default)
1	When Low level or falling edge, Interrupt occur

POLA0 Determine the polarity of External Interrupt 0

0	When High level or rising edge, Interrupt occur(default)
1	When Low level or falling edge, Interrupt occur

EIBOTH (External Interrupt Both Edge Enable Register) : A7H

7	6	5	4	3	2	1	0
-	-	-	-	-	-	BOTH1	BOTH0
-	-	-	-	-	-	R/W	R/W

Initial value: 0H

If BOTHx is written to ‘1’, the corresponding external pin interrupt is enabled by both edges (no level).

And EIEDGE and EIPOLA register value are ignored.

BOTH1 Determine the type of External Interrupt 1

0	Both edge detection Disable (default)
1	Both edge detection Enable

BOTH0 Determine the type of External Interrupt 0

0	Both edge detection Disable (default)
1	Both edge detection Enable

11 Peripheral Hardware

11.1 Clock Generator

11.1.1 Overview

The clock generator produces the basic clock pulses which provide the system clock to CPU and peripheral hardware. The internal RC-OSC is used as system clock and the default division rate is two.

- Calibrated Internal RC Oscillator (32MHz)

. INTERNAL CLOCK(16MHz)/1 (16MHz)

. INTERNAL CLOCK(16MHz)/2 (8MHz, Default system clock)

. INTERNAL CLOCK(16MHz)/4 (4MHz)

. INTERNAL CLOCK(16MHz)/16 (1MHz)

11.1.2 Block Diagram

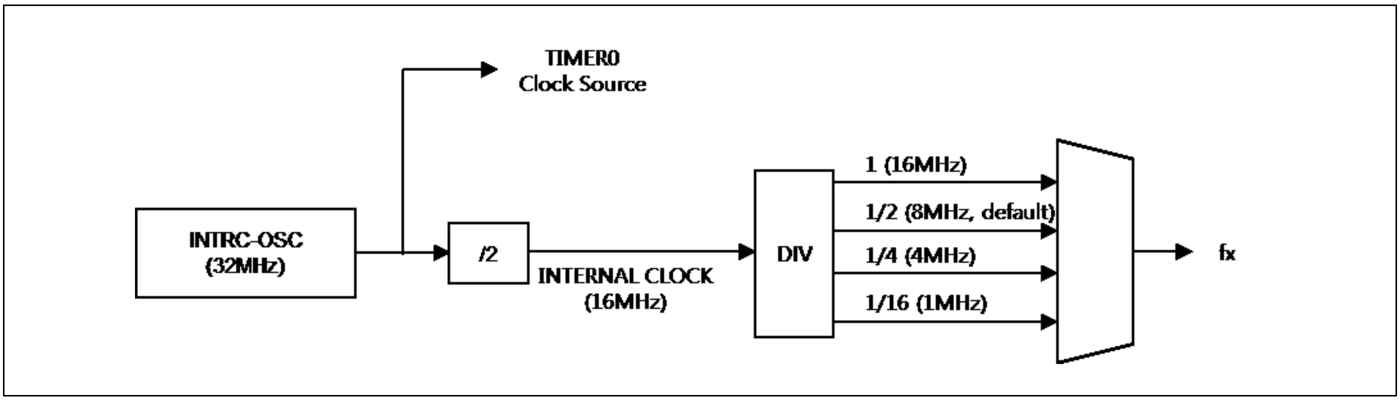


Figure 11.1 Clock Generator Block Diagram

11.1.3 Register Map and Register Description for Clock Generator

Name	Address	Dir	Default	Description
SCCR	8AH	R/W	00H	System and Clock Control Register

Table 11.1 Register Map

SCCR (System and Clock Control Register) : 8AH

7	6	5	4	3	2	1	0
STOP1	DIV1	DIV0	CBYS	ISTOP	-	-	CS
R/W	R/W	R/W	R/W	R/W	-	-	R/W

Initial value : 20H

STOP1 Control the STOP Mode

NOTE) When PCON=0x03, This bit is applied. When PCON=0x01, This bit is not applied.

0	STOP2 Mode (at PCON=0x03) (default)
1	STOP1 Mode (at PCON=0x03)

DIV[1:0] When using internal clock as system clock, determine division rate. NOTE) when using internal clock as system clock, only division rate come into effect.

NOTE) To change by software, CBYS set to ‘1’

DIV1	DIV0	description
0	0	1-Div (16MHz)
0	1	2-Div (8MHz, default system clock)
1	0	4-Div (4MHz)
1	1	16-Div (1MHz)

CBYS Control the scheme of clock change. If this bit set to ‘0’, clock change is controlled by hardware. But if this set to ‘1’, clock change is controlled by software. Ex) when setting CS, if CBYS bit set to ‘0’, it is not changed right now, CPU goes to STOP mode and then when wake-up, it applies to clock change.

NOTE) when clear this bit, keep other bits in SCCR.

0	Clock changed by hardware during stop mode (default)
1	Clock changed by software

ISTOP Control the operation of INT-RC Oscillation

NOTE) when CBYS=’1’, It is applied

0	RC-Oscillation enable (default)
1	RC-Oscillation disable

CS Determine System Clock

NOTE) by CBYS bit, reflection point is decided

CS	Description
0	System clock (default 8MHz)
1	f_{WDTOSC} (8 kHz)

11.2 BIT

11.2.1 Overview

The MC96F1206 has one 8-bit Basic Interval Timer that is free-run and can't stop. Block diagram is shown in . In addition, the Basic Interval Timer generates the time base for watchdog timer counting. It also provides a Basic interval timer interrupt (BITF).

- The MC96F1206 has these Basic Interval Timer (BIT) features:

. During Power On, BIT gives a stable clock generation time

. On exiting Stop mode, BIT gives a stable clock generation time

. As clock function, time interrupt occurrence

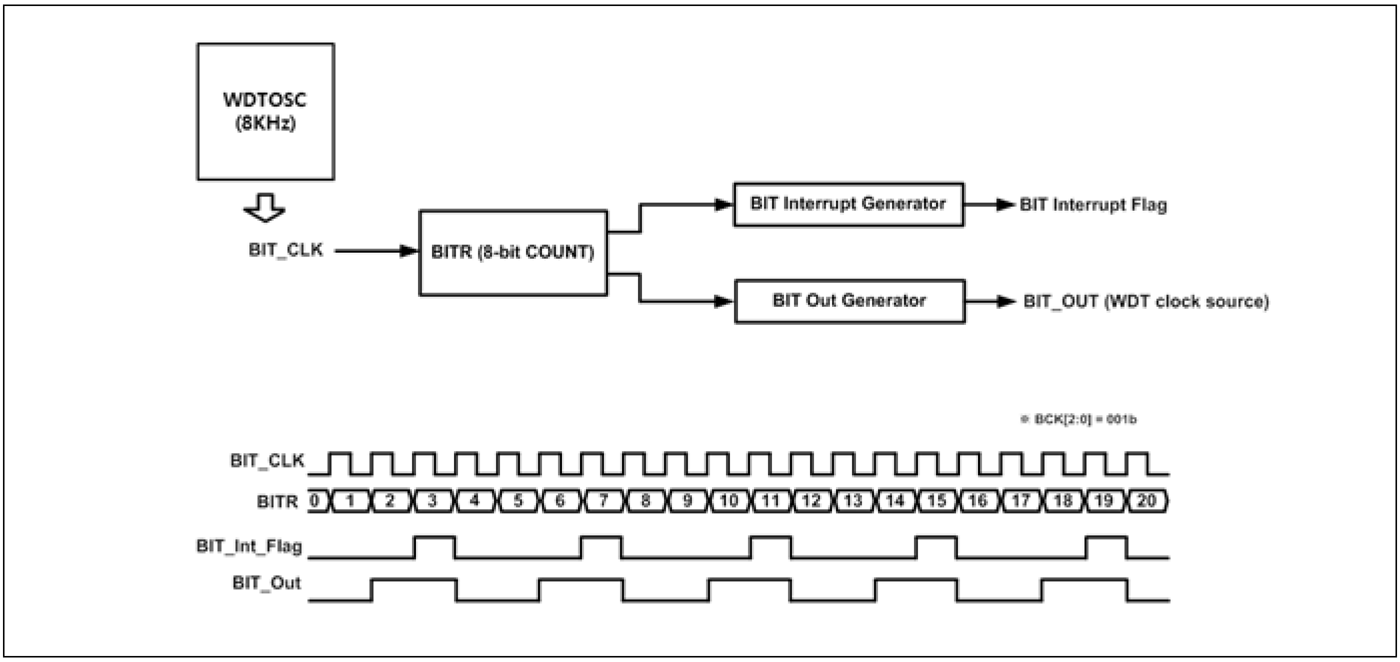


Figure 11.2 BIT Block Diagram

Name	Address	Dir	Default	Description
BCCR	8BH	R/W	06H	BIT Clock Control Register
BITR	8CH	R	00H	Basic Interval Timer Register

Table 11.2 Register Map

11.2.2 Bit Interval Timer Register description

The Bit Interval Timer Register consists of BIT Clock control register (BCCR) and Basic Interval Timer register (BITR). If BCLR bit set to '1', BITR becomes '0' and then counts up. After 1 machine cycle, BCLR bit is cleared as '0' automatically.

11.2.3 Register description for Bit Interval Timer

BCCR (BIT Clock Control Register) : 8BH

7	6	5	4	3	2	1	0
BITF	-	-	IRC_SEL	BCLR	BCK2	BCK1	BCK0
R/W	R	R	R/W	R/W	R/W	R/W	R/W

Initial value : 06H

BITF When BIT Interrupt occurs, this bit becomes '1'. For clearing bit, write '0' to this bit.

0 no generation

1 generation

IRC_SEL BIT Clock source select

0 WDT 8kHz

1 64kHz (IRC Clock source)

BCLR If BCLR Bit is written to '1', BIT Counter is cleared as '0'

0 Free Running

1 Clear Counter

BCK[2:0] Select BIT overflow period (ex) BIT Clock ≒ 8kHz)

BCK2	BCK1	BCK0	
0	0	0	0.25msec (BIT Clock * 2)
0	0	1	0.50msec
0	1	0	1.00msec
0	1	1	2.00msec
1	0	0	4.00msec
1	0	1	8.00msec
1	1	0	16.0msec (default)
1	1	1	32.0msec

BCK[2:0]	WDT 8kHz (IRCSEL=0)	IRC divider 64kHz (IRCSEL=1)
000	0.25 msec	0.03125 msec
001	0.50 msec	0.0625 msec
010	1.00 msec	0.125 msec
011	2.00 msec	0.250 msec
100	4.00 msec	0.500 msec
101	8.00 msec	1.000 msec
110 (default)	16.00 msec	2.000 msec
111	32.00 msec	4.000 msec

Table 11.3 BIT period Table

BITR (Basic Interval Timer Register) : 8CH

7	6	5	4	3	2	1	0
BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
R	R	R	R	R	R	R	R

Initial value : 00H

BIT[7:0]	BIT Counter

11.3 Watch Dog Timer

11.3.1 Overview

The watchdog timer rapidly detects the CPU malfunction such as endless looping caused by noise or the like, and resumes the CPU to the normal state. The watchdog timer signal for detecting malfunction can be selected either a reset CPU or an interrupt request. When the watchdog timer is not being used for malfunction detection, it can be used as a timer to generate an interrupt at fixed intervals. It is possible to use free running 8-bit timer mode (WDTRSON='0') or watch dog timer mode (WDTRSON='1') as setting WDTMR[6] bit. If writing WDTMR[5] to '1', WDT counter value is cleared and counts up. After 1 machine cycle, this bit has '0' automatically. The watchdog timer consists of 8-bit binary counter and the watchdog timer data register. When the value of 8-bit binary counter is equal to the 8 bits of WDTR, the interrupt request flag is generated. This can be used as Watchdog timer interrupt or reset the CPU in accordance with the bit WDTRSON.

The clock source of Watch Dog Timer is BIT overflow output. The interval of watchdog timer interrupt is decided by BIT overflow period and WDTR set value. The equation is as below

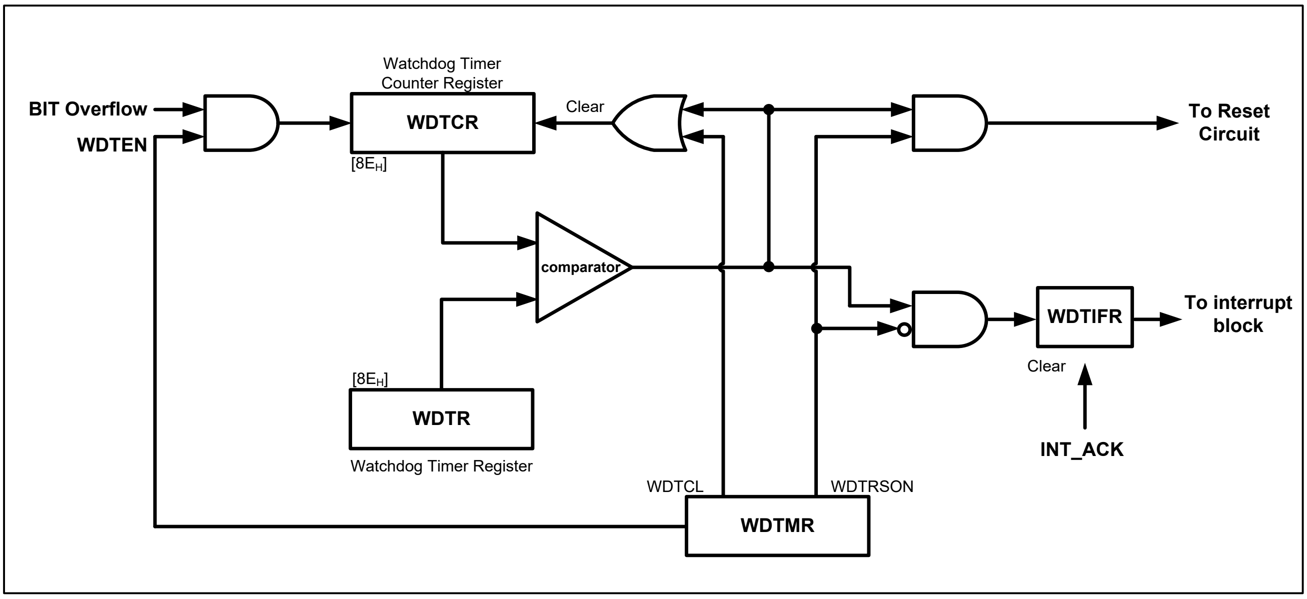


Figure 11.3 WDT Block Diagram

11.3.2 Register Map

Name	Address	Dir	Default	Description
WDTR	8EH	W	FFH	Watch Dog Timer Register
WDTCR	8EH	R	00H	Watch Dog Timer Counter Register
WDTMR	8DH	R/W	00H	Watch Dog Timer Mode Register

Table 11.4 Register Map

11.3.3 Register Description for Watch Dog Timer

WDTR (Watch Dog Timer Register) : 8EH

7	6	5	4	3	2	1	0
WDTR7	WDTR6	WDTR5	WDTR4	WDTR3	WDTR2	WDTR1	WDTR0
W	W	W	W	W	W	W	W

Initial value : FFH

WDTR[7:0] Set a period
WDT Interrupt Interval=(BIT Interrupt Interval) x(WDTR Value+1)

NOTE) To guarantee proper operation, the data should be greater than 01H.

WDTCR (Watch Dog Timer Counter Register: Read Case) : 8EH

7	6	5	4	3	2	1	0
WDTCR7	WDTCR6	WDTCR5	WDTCR4	WDTCR3	WDTCR2	WDTCR1	WDTCR0
R	R	R	R	R	R	R	R

Initial value : 00H

WDTCR[7:0] WDT Counter

WDTMR (Watch Dog Timer Mode Register) : 8DH

7	6	5	4	3	2	1	0
WDTEN	WDTRSON	WDTCL	-	-	-	-	WDTIFR
R/W	R/W	R/W	-	-	-	-	R/W

Initial value : 00H

WDTEN Control WDT operation
0 disable
1 enable

WDTRSON Control WDT Reset operation
0 Free Running 8-bit timer
1 Watch Dog Timer Reset ON

WDTCL Clear WDT Counter
0 Free Run
1 Clear WDT Counter (auto clear after 1 Cycle)

WDTIFR When WDT Interrupt occurs, this bit becomes ‘1’. For clearing bit, write ‘0’ to this bit or auto clear by INT_ACK signal.
0 WDT Interrupt no generation
1 WDT Interrupt generation

11.3.4 WDT Interrupt Timing Waveform

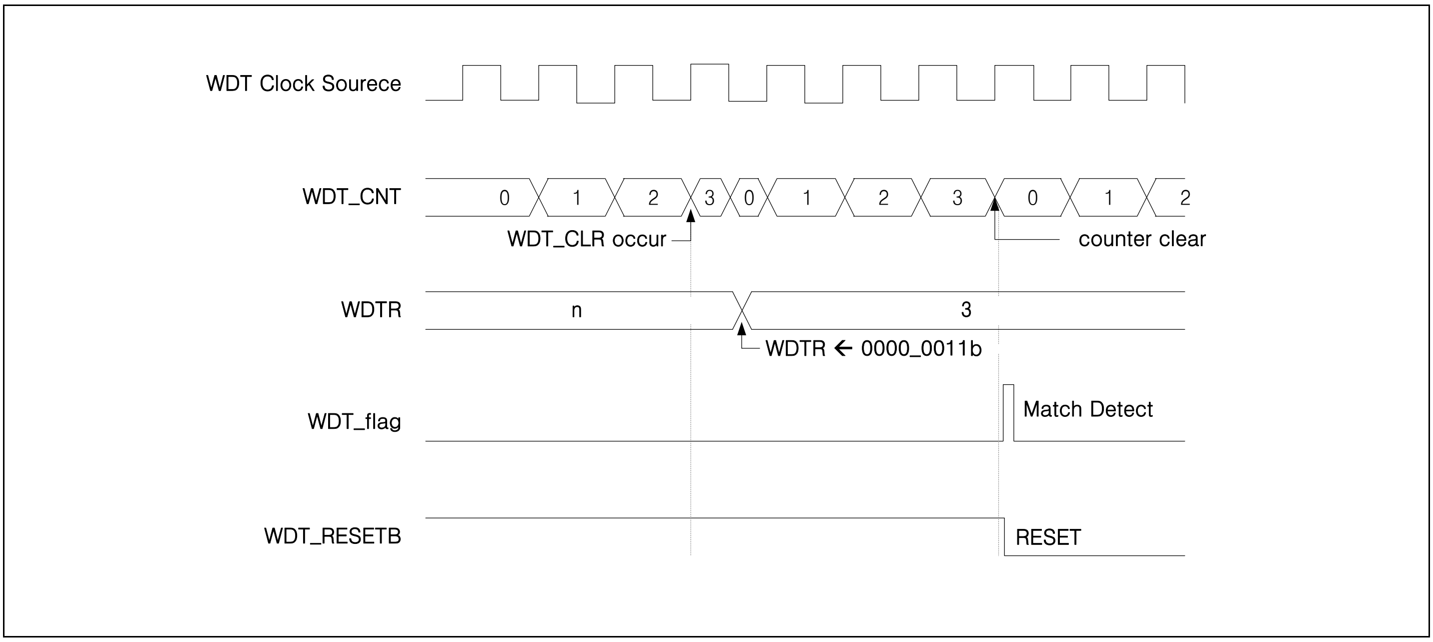


Figure 11.4 WDT Interrupt Timing Waveform

11.4 Timer/PWM

11.4.1 Overview

The 16-bit timer x(0~1) consists of Multiplexer, Timer Data Register High/Low, Timer Register High/Low, Timer Mode Control Register, PWM Duty High/Low, PWM Period High/Low Register. It is able to use internal 16-bit timer/ counter without a port output function.

The 16-bit timer x can be clocked by internal or external clock source (EC0, EC1). The divided clock of the main clock selected from prescaler output.

T32M in the T0CR1 register is select internal-RCOSC(32MHz) as Timer0 clock source.

11.4.2 16-bit Timer/Counter Mode

In the 16-bit Timer/Counter Mode, If the TxH + TxL value and the TxDRH + TxDRL value are matched, Tx/PWMx port outputs. The output is 50:50 of duty square wave, the frequency is following

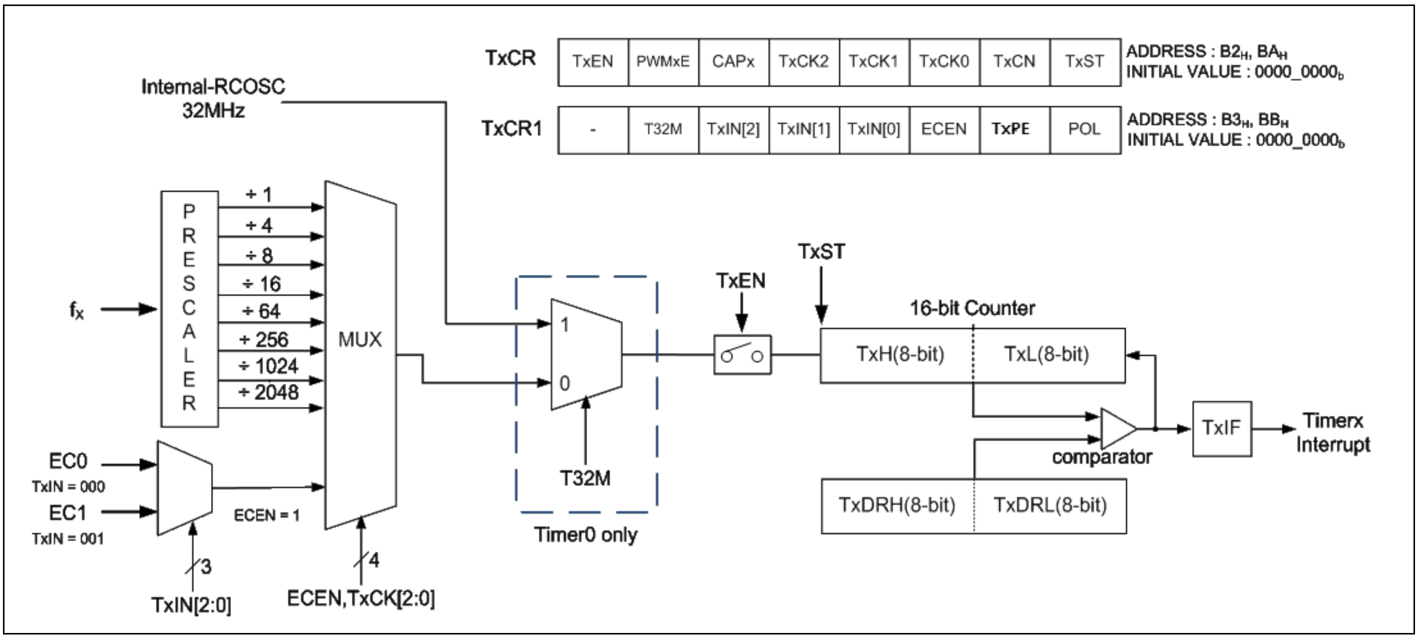
$$f_{COMP} = \frac{\text{Timer Clock Frequency}}{2 \times \text{Prescaler Value} \times (TxDR + 1)}$$

f_{COMP} is timer output frequency and TxDR is the 16 bits value of TxDRH and TxDRL.

To export the compare output as Tx/PWMx, the Tx_PE bit in the TxCR1 register must set to ‘1’.

The 16-bit Timer/Counter Mode is selected by control registers as shown in Figure 11.5

When TxH, TxL are read, TxL should be read first. Because when TxL is read TxH is captured to buffer, and when TxH is read captured value of TxH is read.



TxCR	TxEN	PWMxE	CAPx	TxCK2	TxCK1	TxCK0	TxCN	TxST	ADDRESS : $B2_H$, BA_H INITIAL VALUE : 0000_0000_b
TxCR1	-	T32M	TxIN[2]	TxIN[1]	TxIN[0]	ECEN	TxPE	POL	ADDRESS : $B3_H$, BB_H INITIAL VALUE : 0000_0000_b

Figure 11.5 Timerx 16-bit Mode Block Diagram

11.4.3 16-bit Capture Mode

The timer x(0~1) capture mode is set by CAPx as ‘1’ in TxCR register. The clock is same source as Output Compare mode. The interrupt occurs at TxH, TxL and TxDRH, TxDRL matching time. The capture result is loaded into CDRxH, CDRxL. The TxH, TxL value is automatically cleared(0000$_H$) by hardware and restarts counter.

This timer interrupt in capture mode is very useful when the pulse width of captured signal is wider than the maximum period of timer. As the EIEDGE and EIPOLA and EIBOTH register setting, the external interrupt INTx function is chosen.

The CDRxH, PWMxDRH and TxH are in same address. In the capture mode, reading operation is read the CDRxH, not TxH because path is opened to the CDRxH. PWMxDRH will be changed in writing operation. The PWMxDRL, TxL, CDRxL has the same function.

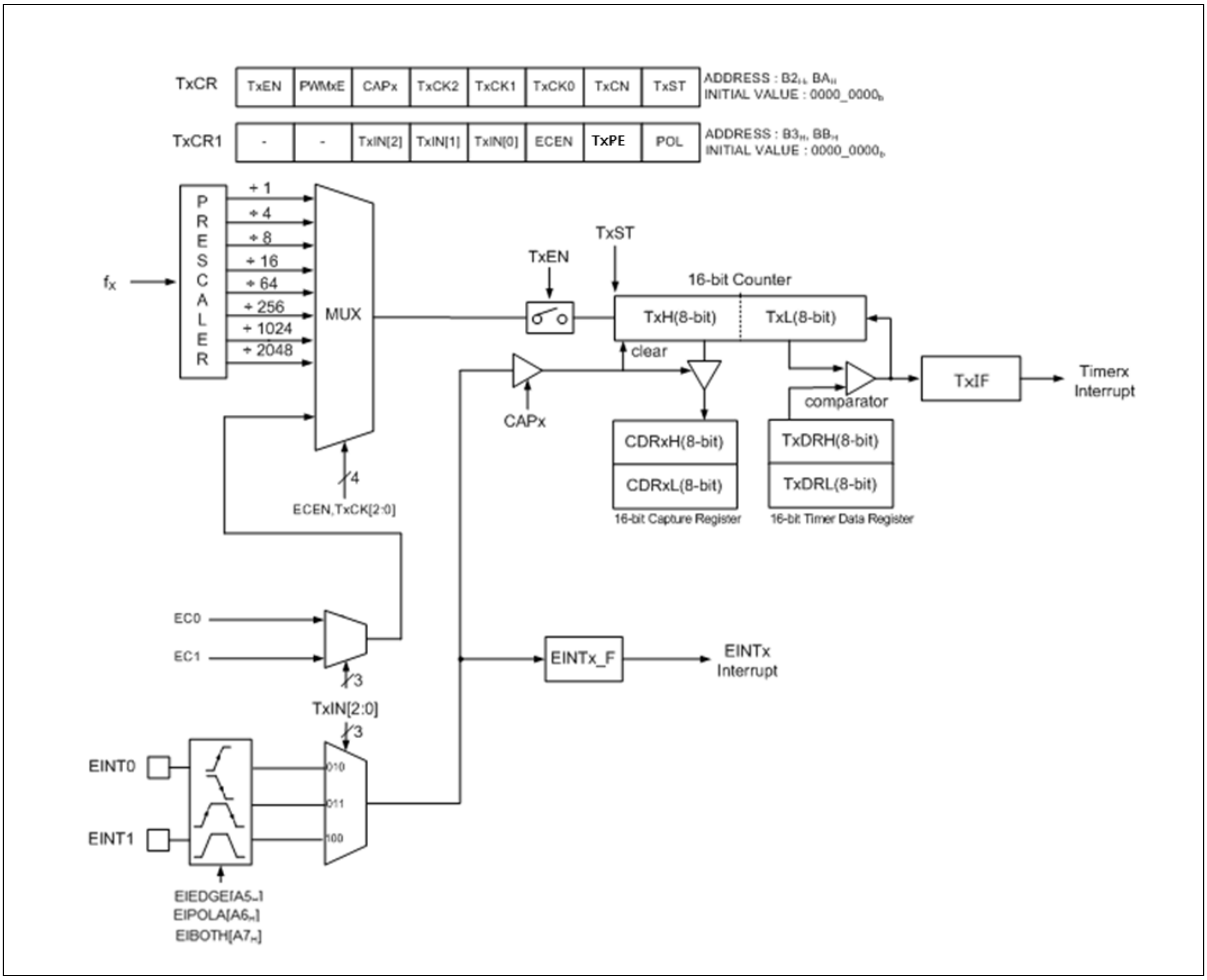


Figure 11.6 Timerx 16-bit Capture Mode

11.4.4 PWM Mode

The timer x(0~1) has a PWM (pulse Width Modulation) function. In PWM mode, the Tx/PWMx output pin outputs up to 16-bit resolution PWM output. This pin should be configured as a PWM output by set TX_PE to '1'. The PWM output mode is determined by the PWMxPRH, PWMxPRL, PWMxDRH and PWMxDRL. And you should configure PWMxE bit to "1" in TxCR register before write to PWM registers.

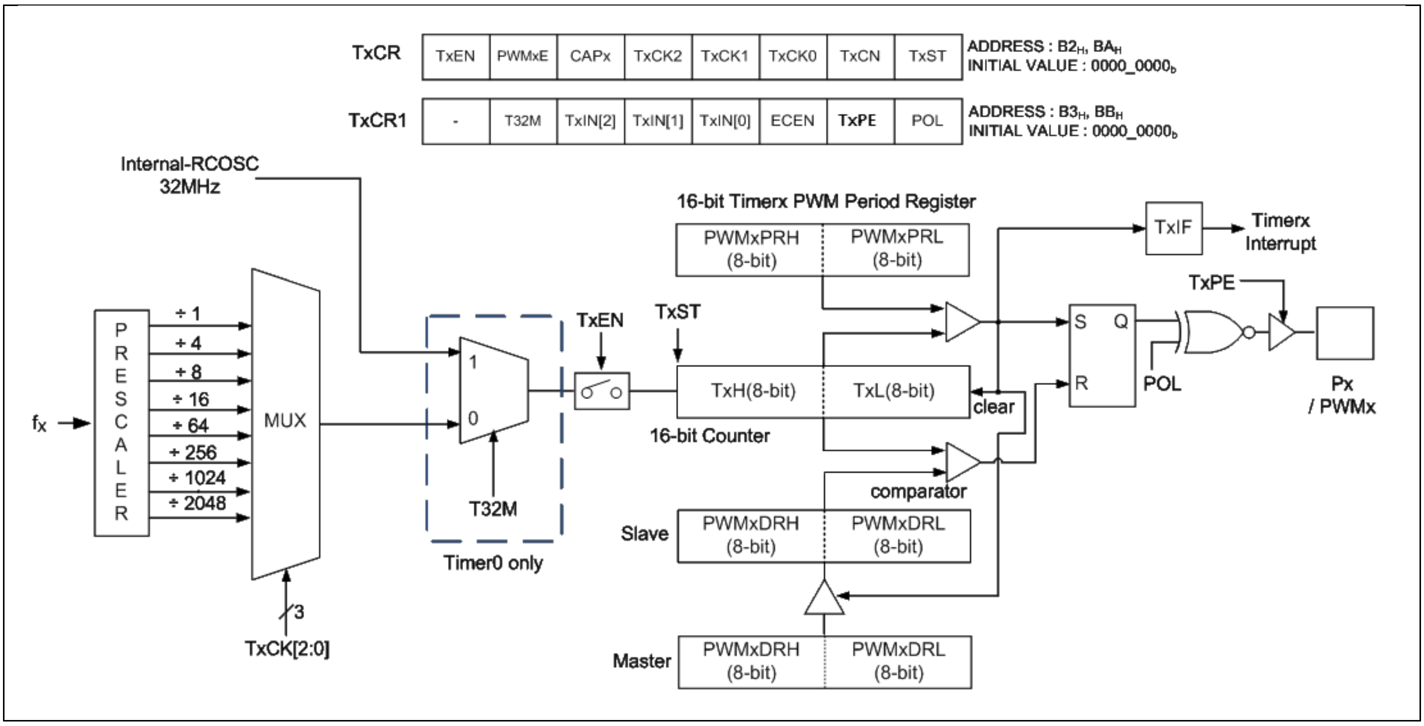
PWM Period = ({PWMxPRH, PWMxPRL} + 1) X Timerx Clock Period

PWM Duty = ({PWMxDRH, PWMxDRL} + 1) X Timerx Clock Period

Resolution	Frequency (MC96F1206)			
	T32M = 1	T32M = 0 TxCK[2:0]=000 (62.5ns)	T32M = 0 TxCK[2:0]=001 (250ns)	T32M = 0 TxCK[2:0]=010 (500ns)
16-bit	488.281 Hz	244.141 Hz	61.035 Hz	30.517 Hz
15-bit	976.563 Hz	488.281 Hz	122.07 Hz	61.035 Hz
10-bit	31.250 kHz	15.625 kHz	3.906 kHz	1.953 kHz
9-bit	62.500 kHz	31.250 kHz	7.812 kHz	3.906 kHz
8-bit	125.00 kHz	62.500 kHz	15.625 kHz	7.812 kHz

Table 11.5 PWM Frequency vs. Resolution at 16MHz and 32MHz

In PWM mode, the duty value and counter matching enables the period value and counter comparison. After counter and the period value matching, counter restarts. If the duty value is set same to the period value, counter doesn't restart after the duty value and counter matching. It is highly recommended that the duty value is not set same to the period value. PWM Period and Duty same output shown in Figure 11.9. The POL bit of TxCR register decides the polarity of duty cycle.



TxCR	TxEN	PWMxE	CAPx	TxCK2	TxCK1	TxCK0	TxCN	TxST	ADDRESS : $B2_H$, BA_H INITIAL VALUE : 0000_0000_b
TxCR1	-	T32M	TxIN[2]	TxIN[1]	TxIN[0]	ECEN	TxPE	POL	ADDRESS : $B3_H$, BB_H INITIAL VALUE : 0000_0000_b

Figure 11.7 PWM Mode

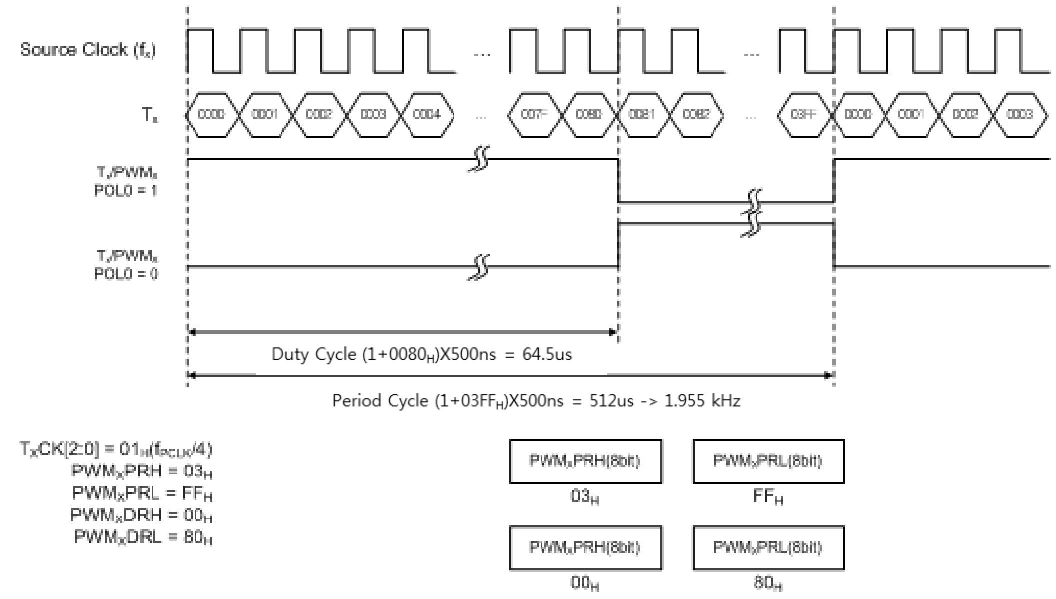


Figure 11.8 Example of PWM at 8MHz

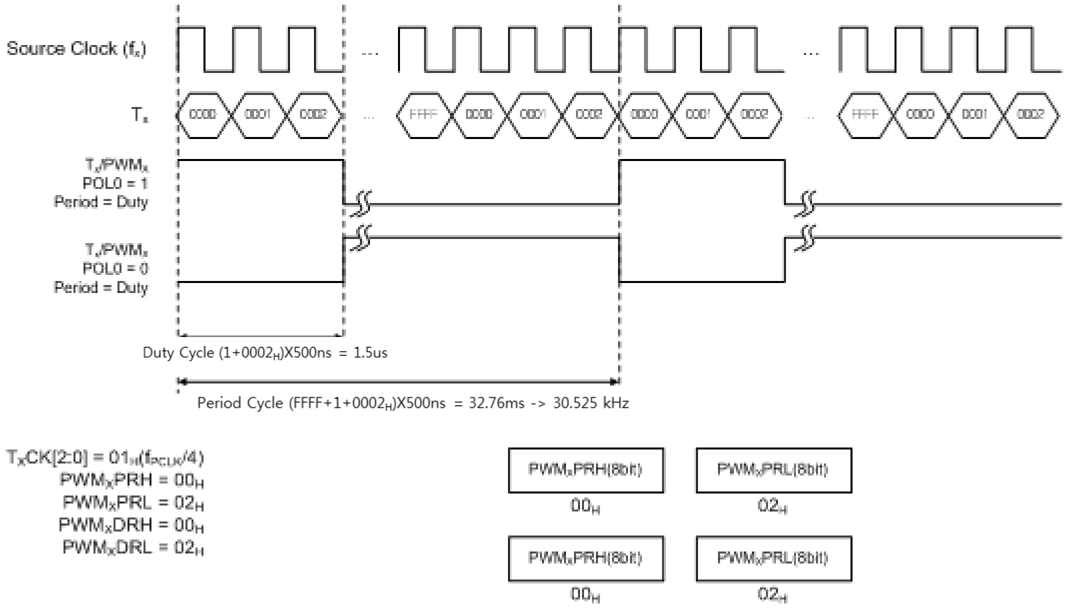


Figure 11.9 Example of PWM at 8MHz (Period = Duty)

11.4.5 Timer Data and Period/Duty Write

When writing a value to the Timer x data registers, write to the TxDRH first, then write to the TxDRL. When writing to the high register, it is stored in a temporary buffer. When writing to the low register, temporary buffer is saved the data high register. Timer period/duty registers (PWMxDRH, PWMxDRL, PWMxPRH, PWMxPRL) operate in the same way. Whenever the counter is started, data high/low registers are loaded to the compare registers.

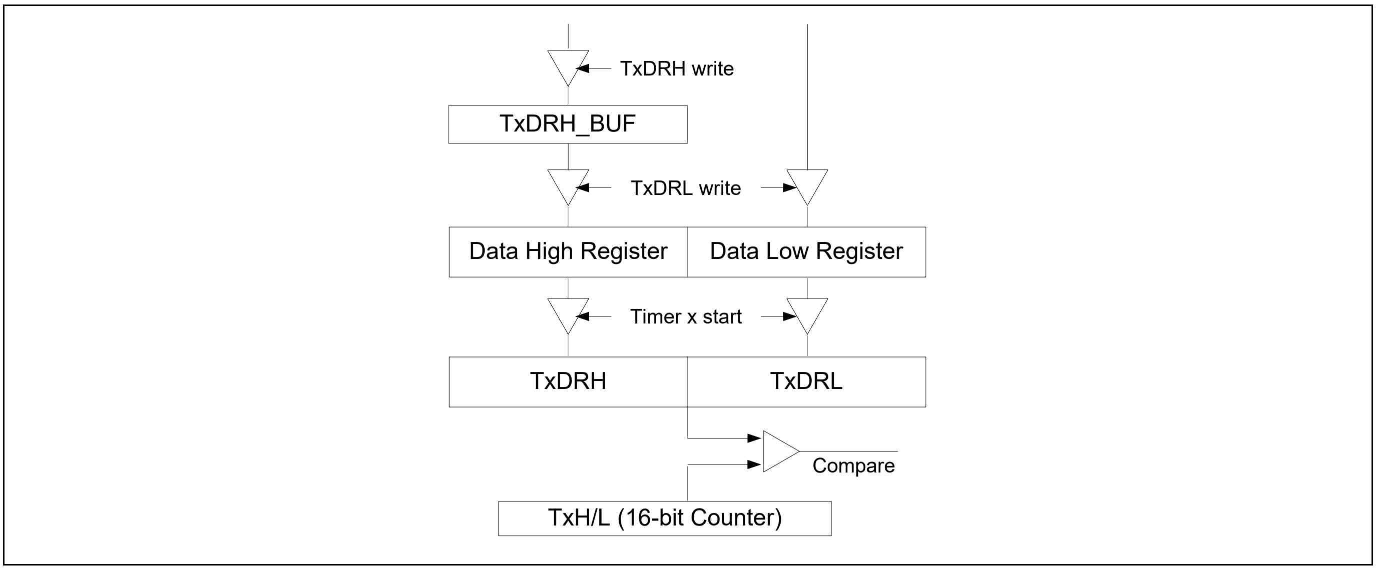


Figure 11.10 Timer x Compare Data Write

11.4.6 Register Map

Name	Address	Dir	Default	Description
T0CR	B2$_H$	R/W	00$_H$	Timer 0 Mode Control Register
T0CR1	B3$_H$	R/W	00$_H$	Timer 0 Mode Control Register 1
T0L	B4$_H$	R	00$_H$	Timer 0 Low Register
PWM0DRL	B4$_H$	R/W	00$_H$	PWM 0 Duty Register Low
CDR0L	B4$_H$	R	00$_H$	Timer 0 Capture Data Register Low
T0H	B5$_H$	R	00$_H$	Timer 0 Register High
PWM0DRH	B5$_H$	R/W	00$_H$	PWM 0 Duty Register High
CDR0H	B5$_H$	R	00$_H$	Timer 0 Capture Data Register High
T0DRL	B6$_H$	W	FF$_H$	Timer 0 Data Register Low
PWM0PRL	B6$_H$	W	FF$_H$	PWM 0 Period Register Low
T0DRH	B7$_H$	W	FF$_H$	Timer 0 Data Register High
PWM0PRH	B7$_H$	W	FF$_H$	PWM 0 Period Register High
T1CR	BA$_H$	R/W	00$_H$	Timer 1 Mode Control Register
T1CR1	BB$_H$	R/W	00$_H$	Timer 1 Mode Control Register 1
T1L	BC$_H$	R	00$_H$	Timer 1 Register Low
PWM1DRL	BC$_H$	R/W	00$_H$	PWM 1 Duty Register Low
CDR1L	BC$_H$	R	00$_H$	Timer 1 Capture Data Register Low
T1H	BD$_H$	R	00$_H$	Timer 1 Register High
PWM1DRH	BD$_H$	R/W	00$_H$	PWM 1 Duty Register High
CDR1H	BD$_H$	R	00$_H$	Timer 1 Capture Data Register High
T1DRL	BE$_H$	W	FF$_H$	Timer 1 Data Register Low
PWM1PRL	BE$_H$	W	FF$_H$	PWM 1 Period Register Low
T1DRH	BF$_H$	W	FF$_H$	Timer 1 Data Register High
PWM1PRH	BF$_H$	W	FF$_H$	PWM 1 Period Register High

Table 11.6 Register Map

11.4.7 Register description for Timer/Counter x

TxCR (Timer 0~1 Mode Control Register): B2H, BAH

7	6	5	4	3	2	1	0
TxEN	PWMxE	CAPx	TxCK2	TxCK1	TxCK0	TxCN	TxST
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Initial value : 00_H

TxEN Control Timer x

0 Timer x disable

1 Timer x enable

PWMxE Control PWM enable

0 PWM disable

1 PWM enable

CAPx Control Timer x capture mode.

0 Timer/Counter mode

1 Capture mode

TxCK[2:0] Select clock source of Timer x. Fx is the frequency of main system

TxCK2	TxCK1	TxCK0	description
0	0	0	f_X
0	0	1	$f_X/4$
0	1	0	$f_X/8$
0	1	1	$f_X/16$
1	0	0	$f_X/64$
1	0	1	f_X /256
1	1	0	$f_X/1024$
1	1	1	$f_X/2048$

TxCN Control Timer x Count pause/continue.

0 Temporary count stop

1 Continue count

TxST Control Timer x start/stop

0 Counter stop

1 Clear counter and start

NOTE) set TxST bit after write to Tx, PWM, CDRx registers.

.

TxCR1 (Timer 0~1 Mode Control Register 1) : B3H, BBH

7	6	5	4	3	2	1	0
-	T32M	TxIN[2]	TxIN[1]	TxIN[0]	ECEN	Tx_PE	POL
-	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Initial value : 00H

T32M Select the Timer Clock Source to 32MHz IRC. (Timer0 Only)

0 Clock Source is selected by TxCK[2:0]

1 32MHz Clock Source

TxIN[2:0] Select Event Counter and External Interrupt for Capture mode

TxIN2	TxIN1	TxIN0	description
0	0	0	EC0
0	0	1	EC1
0	1	0	XINT0
0	1	1	XINT1
1	0	0	-
1	0	1	-
1	1	0	-
1	1	1	-

ECEN Control Event Counter

0 Event Counter disable

1 Event Counter enable

Tx_PE Control Timer x Output port

0 Timer x Output disable

1 Timer x Output enable

POL Configure PWM polarity

0 Negative (Duty Match: Clear)

1 Positive (Duty Match: Set)

TxL (Timer 0~1 Register Low, Read Case) : B4H, BCH

7	6	5	4	3	2	1	0
TxL7	TxL6	TxL5	TxL4	TxL3	TxL2	TxL1	TxL0
R	R	R	R	R	R	R	R

Initial value : 00H

TxL[7:0] TxL Counter Period Low data.

CDRxL (Capture 0~1 Data Register Low, Read Case) : B4H, BCH

7	6	5	4	3	2	1	0
CDRxL07	CDRxL06	CDRxL05	CDRxL04	CDRxL03	CDRxL02	CDRxL01	CDRxL00
R	R	R	R	R	R	R	R

Initial value : 00H

CDRxL[7:0] Tx Capture Low data.

PWMxDRL (PWM 0~1 Duty Register Low, Write Case) : B4H, BCH

7	6	5	4	3	2	1	0
PWMxDRL7	PWMxDRL6	PWMxDRL5	PWMxDRL4	PWMxDRL3	PWMxDRL2	PWMxDRL1	PWMxDRL0
W	W	W	W	W	W	W	W

Initial value : 00H

PWMxDRL[7:0] Tx PWM Duty Low data
NOTE) Writing is effective only when PWMxE = 1 and TxST = 0

TxH (Timer 0~1 Register High, Read Case) : B5H, BDH

7	6	5	4	3	2	1	0
TxH7	TxH6	TxH5	TxH4	TxH3	TxH2	TxH1	TxH0
R	R	R	R	R	R	R	R

Initial value : 00_H

TxH[7:0] TxH Counter Period High data.

CDRxH (Capture 0~1 Data High Register, Read Case) : B5H, BDH

7	6	5	4	3	2	1	0
CDRxH07	CDRxH06	CDRxH05	CDRxH04	CDRxH03	CDRxH02	CDRxH01	CDRxH00
R	R	R	R	R	R	R	R

Initial value : 00_H

CDRxH[7:0] Tx Capture High data

PWMxDRH (PWM0~1 Duty Register High, Write Case) : B5H, BDH

7	6	5	4	3	2	1	0
PWMxDRH7	PWMxDRH6	PWMxDRH5	PWMxDRH4	PWMxDRH3	PWMxDRH2	PWMxDRH1	PWMxDRH0
W	W	W	W	W	W	W	W

Initial value : 00_H

PWMxDRH[7:0] Tx PWM Duty High data
NOTE) Writing is effective only when PWMxE = 1 and TxST = 0

TxDRL (Timer 0~1 Data Register Low, Write Case) : B6H, BEH

7	6	5	4	3	2	1	0
TxDRL7	TxDRL6	TxDRL5	TxDRL4	TxDRL3	TxDRL2	TxDRL1	TxDRL0
W	W	W	W	W	W	W	W

Initial value : FF_H

TxDRL[7:0] TxL Compare Low data

NOTE) Be sure to clear PWMxE before loading this register.

PWMxPRL (PWM 0~1 Period Register Low, Write Case) : B6H, BEH

7	6	5	4	3	2	1	0
PWMxPRL7	PWMxPRL6	PWMxPRL5	PWMxPRL4	PWMxPRL3	PWMxPRL2	PWMxPRL1	PWMxPRL0
W	W	W	W	W	W	W	W

Initial value : FF_H

PWMxPRL[7:0] TxPWM Period Low data
NOTE) Writing is effective only when PWMxE = 1 and TxST = 0

TxDRH (Timer 0~1 Data Register High, Write Case) : B7H, BFH

7	6	5	4	3	2	1	0
TxDRH7	TxDRH6	TxDRH5	TxDRH4	TxDRH3	TxDRH2	TxDRH1	TxDRH0
W	W	W	W	W	W	W	W

Initial value : FF_H

TxDRH[7:0] TxH Compare High data
NOTE) Be sure to clear PWMxE before loading this register.

PWMxPRH (PWM 0~1 Period Register High, Write Case) : B7H, BFH

7	6	5	4	3	2	1	0
PWMxPRH7	PWMxPRH6	PWMxPRH5	PWMxPRH4	PWMxPRH3	PWMxPRH2	PWMxPRH1	PWMxPRH0
R/W	W	W	W	W	W	W	W

Initial value : FF_H

PWMxPRH[7:0] TxPWM Period High data
NOTE) Writing is effective only when PWMxE = 1 and TxST = 0

11.5 12-bit A/D Converter

11.5.1 Overview

The analog-to-digital converter (A/D) allows conversion of an analog input signal to a corresponding 12-bit digital value. The A/D module has tenth analog inputs. The output of the multiplex is the input into the converter, which generates the result via successive approximation. The A/D module has four registers which are the control register ADCM (A/D Converter Mode Register), ADCM1 (A/D Converter Mode Register 1) and A/D result register ADCHR (A/D Converter Result High Register) and ADCLR (A/D Converter Result Low Register). It is selected for the corresponding channel to be converted by setting ADSEL[3:0]. To executing A/D conversion, ADST bit sets to '1'. The register ADCHR and ADCLR contains the results of the A/D conversion. When the conversion is completed, the result is loaded into the ADCHR and ADCLR, the A/D conversion status bit AFLAG is set to '1', and the A/D interrupt is set. For processing A/D conversion, AFLAG bit is read as '0'. If using STBY (power down) bit, the ADC is disabled. Also internal timer, external generating event, comparator, the trigger of timer1pwm and etc. can start ADC regardless of interrupt occurrence.

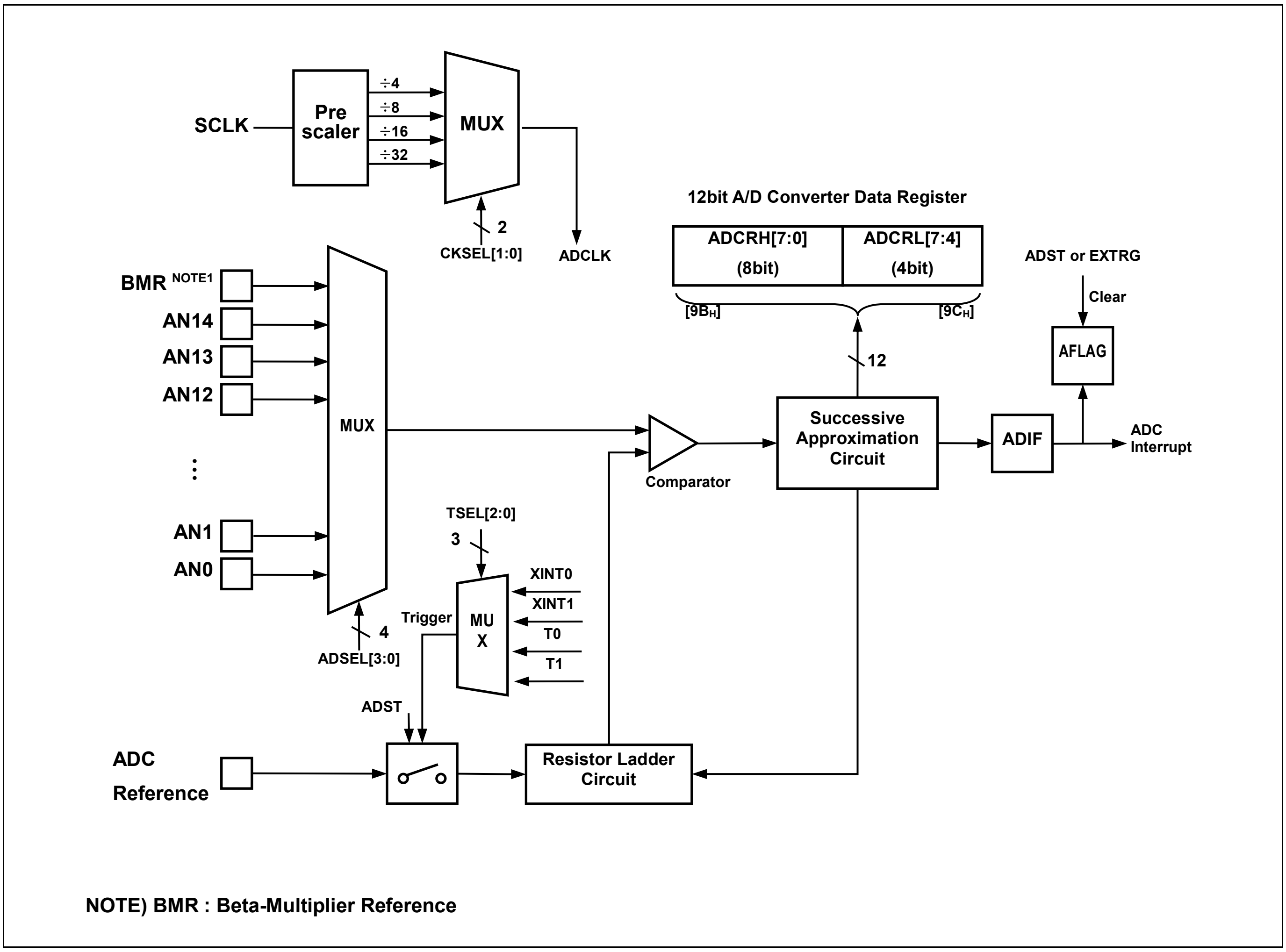
ADC Conversion Time = ADCLK * 60 cycles

After STBY bit is reset (ADC power enable) and it is restarted, during some cycle, ADC conversion value may have an inaccurate value.
When using ports as ADC input port, it is recommended to set corresponding PSR2, PSR3 registers to prevent current leakage or unexpected function, because analog value enters to digital circuit.

ADC zero offset value is written to 1868h of option memory.
To read the zero offset value, refer to the assembly code below.

```
(Example)
char Zero_offset;                        // signed value
#pragma ASM
  mov    A, #0                            ;
  mov    DPTR, #1868h                    ; ADC Zero offset value is addressed at 0x1868
  movc   A, @A+DPTR                      ; A = ADC zero offset value
#pragma ENDASM
 Zero_offset = ACC;                      //
```

11.5.2 Block Diagram



NOTE) BMR : Beta-Multiplier Reference

Figure 11.11 ADC Block Diagram

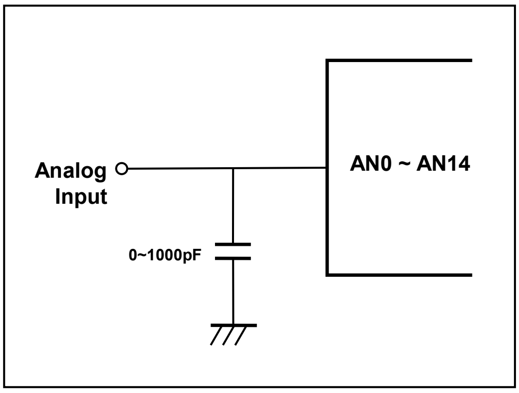


Figure 11.12 A/D Analog Input Pin Connecting Capacitor

11.5.3 ADC Operation

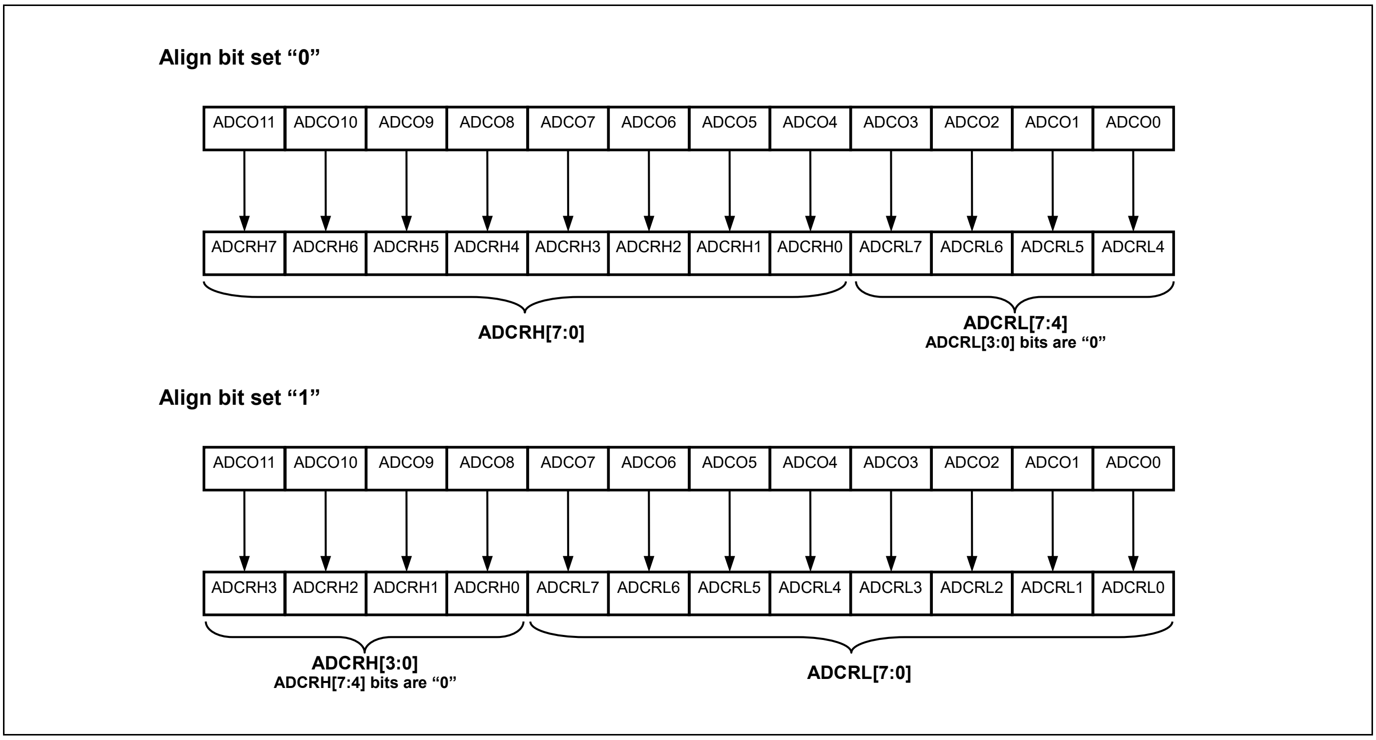

Align bit set “0”
ADCO11 ADCO10 ADCO9 ADCO8 ADCO7 ADCO6 ADCO5 ADCO4 ADCO3 ADCO2 ADCO1 ADCO0
ADCRH7 ADCRH6 ADCRH5 ADCRH4 ADCRH3 ADCRH2 ADCRH1 ADCRH0 ADCRL7 ADCRL6 ADCRL5 ADCRL4
ADCRH[7:0]
ADCRL[7:4]
ADCRL[3:0] bits are “0”
Align bit set “1”
ADCO11 ADCO10 ADCO9 ADCO8 ADCO7 ADCO6 ADCO5 ADCO4 ADCO3 ADCO2 ADCO1 ADCO0
ADCRH3 ADCRH2 ADCRH1 ADCRH0 ADCRL7 ADCRL6 ADCRL5 ADCRL4 ADCRL3 ADCRL2 ADCRL1 ADCRL0
ADCRH[3:0]
ADCRH[7:4] bits are “0”
ADCRL[7:0]

Figure 11.13 ADC Operation for Align bit

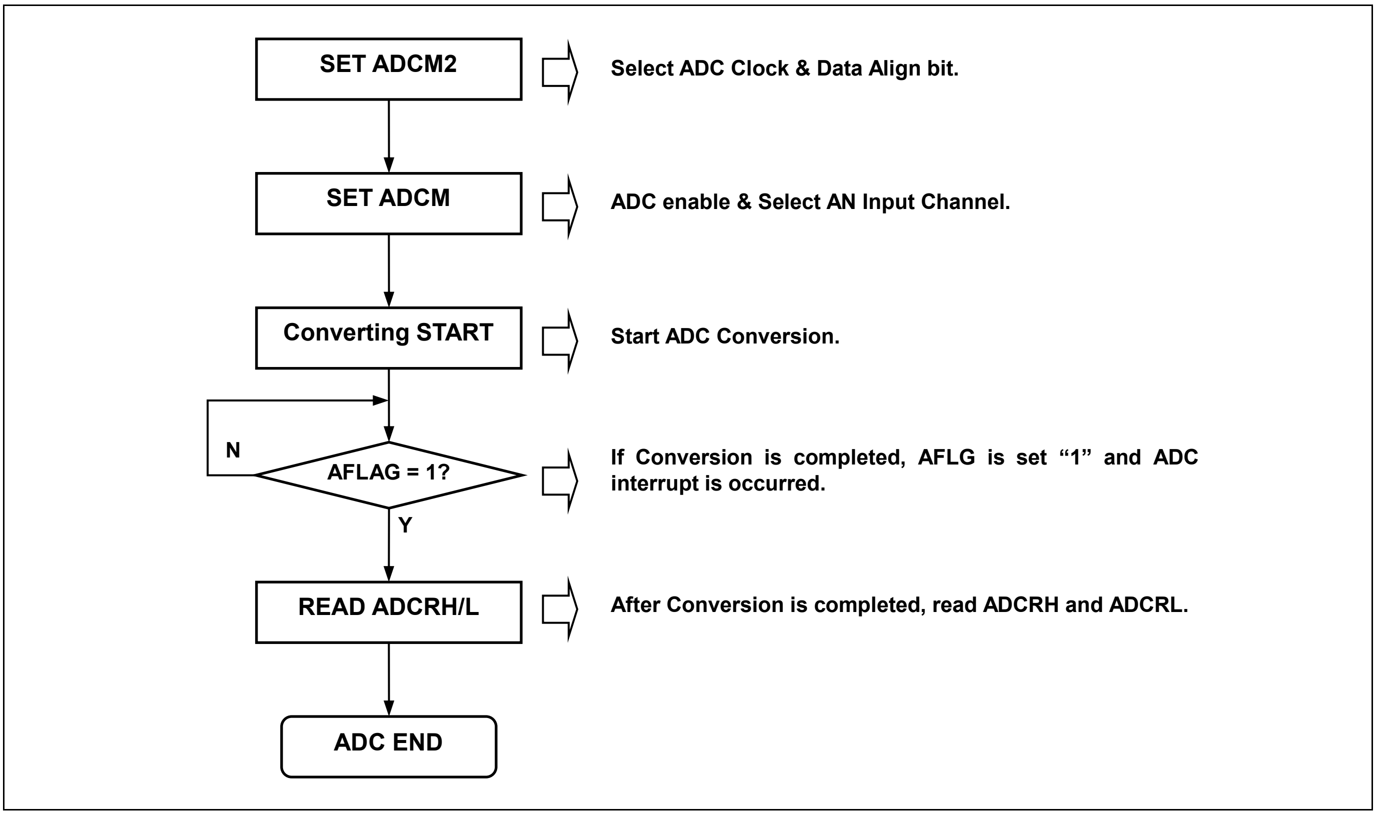

SET ADCM2
Select ADC Clock & Data Align bit.
SET ADCM
ADC enable & Select AN Input Channel.
Converting START
Start ADC Conversion.
N
AFLAG = 1?
Y
If Conversion is completed, AFLG is set “1” and ADC interrupt is occurred.
READ ADCRH/L
After Conversion is completed, read ADCRH and ADCRL.
ADC END

Figure 11.14 Converter Operation Flow

11.5.4 Register Map

Name	Address	Dir	Default	Description
ADCM	95H	R/W	8FH	A/D Converter Mode Register
ADCM1	94H	R/W	01H	A/D Converter Mode 1 Register
ADCRL	96H	R	xxH	A/D Converter Result Low Register
ADCRH	97H	R	xxH	A/D Converter Result High Register
LDOCR	A1H	R/W	00H	LDO Control Register

Table 11.7 Register Map

11.5.5 Register Description for ADC

The ADC Register consists of A/D Converter Mode Register (ADCM), A/D Converter Result High Register (ADCRH), A/D Converter Result Low Register (ADCRL), A/D Converter Mode 1 Register (ADCM1)..

NOTE) When STBY bit is set to '1', ADCM1 is read.
If ADC enables, it is possible only to write ADCM1. When reading, ADCRL is read.

ADCM (A/D Converter Mode Register) : 95H

7	6	5	4	3	2	1	0
STBY	ADST	REFSEL	AFLAG	ADSEL3	ADSEL2	ADSEL1	ADSEL0
R/W	R/W	R/W	R	R/W	R/W	R/W	R/W

Initial value : 8FH

STBY Control operation of A/D standby (power down)
0 ADC module enable
1 ADC module disable (power down)

ADST Control A/D Conversion stop/start.
0 ADC Conversion Stop
1 ADC Conversion Start

REFSEL A/D Converter reference selection
0 VDD Reference (default)
1 Internal LDO (2.5V) Reference

AFLAG A/D Converter operation state
0 During A/D Conversion
1 A/D Conversion finished

ADSEL[3:0] A/D Converter input selection

ADSEL3	ADSEL2	ADSEL1	ADSEL0	Description
0	0	0	0	Channel0(AN0)
0	0	0	1	Channel1(AN1)
0	0	1	0	Channel2(AN2)
0	0	1	1	Channel3(AN3)
0	1	0	0	Channel4(AN4)
0	1	0	1	Channel5(AN5)
0	1	1	0	Channel6(AN6)
0	1	1	1	Channel7(AN7)
1	0	0	0	Channel8(AN8)
1	0	0	1	Channel9(AN9)
1	0	1	0	Channel10(AN10)
1	0	1	1	Channel11(AN11)
1	1	0	0	Channel12(AN12)
1	1	0	1	Channel13(AN13)
1	1	1	0	Channel14(AN14)
1	1	1	1	Channel15(BMR)

NOTE) When using ports as ADC input port, set corresponding PSR2, PSR3 register to ADC input mode in order to open analog input switch and to prevent digital input.

ADCRH (A/D Converter Result High Register) : 97H

7	6	5	4	3	2	1	0
ADDM11	ADDM10	ADDM9	ADDM8	ADDM7 ADDL11	ADDM6 ADDL10	ADDM5 ADDL9	ADDM4 ADDL8
R	R	R	R	R	R	R	R

Initial value : xxH

ADDM[11:4] MSB align, A/D Converter High result (8-bit), default

ADDL[11:8] LSB align, A/D Converter High result (4-bit)

ADCRL (A/D Converter Result Low Register) : 96H

7	6	5	4	3	2	1	0
ADDM3 ADDL7	ADDM2 ADDL6	ADDM1 ADDL5	ADDM0 ADDL4	ADDL3	ADDL2	ADDL1	ADDL0
R	R	R	R	R	R	R	R

Initial value : xxH

ADDM[3:0] MSB align, A/D Converter Low result (4-bit), default

ADDL[7:0] LSB align, A/D Converter Low result (8-bit)

ADCM1 (A/D Converter Mode Register) : 94H

7	6	5	4	3	2	1	0
EXTRG	TSEL2	TSEL1	TSEL0	-	ALIGN	CKSEL1	CKSEL0
R/W	R/W	R/W	R/W	-	R/W	R/W	R/W

Initial value : 01H

EXTRG A/D external Trigger

0 External Trigger disable

1 External Trigger enable

TSEL[2:0] A/D Trigger Source selection

TSEL2	TSEL1	TSEL0	Description
0	0	0	Ext. Interrupt 0
0	0	1	Ext. Interrupt 1
0	1	0	-
0	1	1	-
1	0	0	Timer0 interrupt
1	0	1	Timer1 interrupt
1	1	0	-

ALIGN A/D Converter data align selection.

0 MSB align (ADCRH[7:0], ADCRL[7:4])

1 LSB align (ADCRH[3:0], ADCRL[7:0])

CKSEL[1:0] A/D Converter Clock selection

CKSEL1	CKSEL0	ADC Clock	ADC VDD
0	0	fx/4	3V~5V
0	1	fx/8	3V~5V
1	0	fx/16	2.7V~3V
1	1	fx/32	2.4V~2.7V

NOTE) fx : system clock
ADC clock should be used below 3MHz

LDOCR (LDO Control Register) : A1H

7	6	5	4	3	2	1	0
-	-	-	-	-	VREF2P3SEL	DSCHGEN	LDOEN
-	-	-	-	-	R/W	R/W	R/W

Initial value : 00H

VREF2P3SEL	LDO output voltage select (Test only)	
	0	2.5V (default)
	1	About 2.3V
DSCHGEN	LDO Output Voltage Discharge Enable (Test only)	
	0	Disable
	1	Enable
LDOEN	2.5V LDO Enable	
	0	Disable (default)
	1	Enable

12 Power Down Operation

12.1 Overview

The MC96F1206 has three power-down modes to minimize the power consumption of the device. In power down mode, power consumption is reduced considerably. The device provides three kinds of power saving functions, IDLE, STOP1 and STOP2 mode. In three modes, program is stopped.

To go to STOP1 mode, WDTRC should be set by writing '1' to STOP1 bit in SCCR register.

12.2 Peripheral Operation in IDLE/STOP Mode

Peripheral	IDLE Mode	STOP1 Mode STOP1 = '1'	STOP2 Mode STOP1 = '0'
CPU	ALL CPU Operation are Disable	ALL CPU Operation are Disable	ALL CPU Operation are Disable
RAM	Retain	Retain	Retain
Watch Dog Timer	Operates Continuously	Operates Continuously	Stop
Timer	Operates Continuously	Halted (Only when the Event Counter Mode is Enable, Timer operates Normally)	Halted (Only when the Event Counter Mode is Enable, Timer operates Normally)
Internal OSC (32MHz)	Oscillation	Stop	Stop
Internal WDTOSC (8kHz)	Oscillation	Oscillation	Stop
I/O Port	Retain	Retain	Retain
Control Register	Retain	Retain	Retain
Address Data Bus	Retain	Retain	Retain
Release Method	By RESET, all Interrupts	By RESET, External Interrupt, WDT, LVI, TIMER(EC)	By RESET, External Interrupt, LVI, TIMER(EC)

Table 12.1 Peripheral Operation during Power Down Mode

NOTE) Before you use MCU STOP1/2 mode, you must disable P02, P13 debounce.

12.3 IDLE Mode

The power control register is set to ‘01h’ to enter the IDLE Mode. In this mode, the internal oscillation circuits remain active. Oscillation continues and peripherals are operated normally but CPU stops. It is released by reset or interrupt. To be released by interrupt, interrupt should be enabled before IDLE mode. If using reset, because the device becomes initialized state, the registers have reset value.

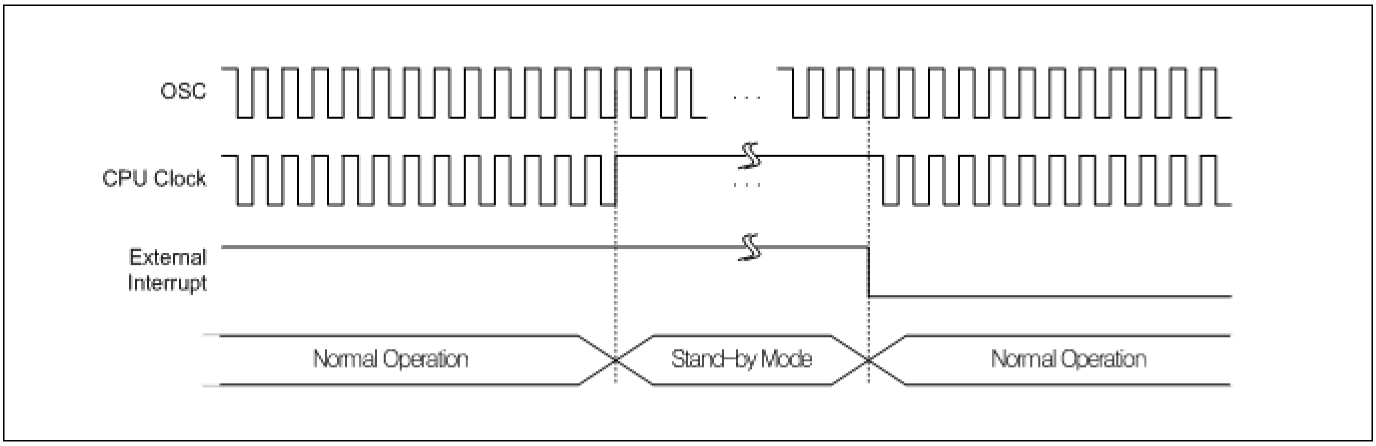


Figure 12.1 IDLE Mode Release Timing by External Interrupt

(Ex) MOV PCON, #0000_0001b ; setting of IDLE mode : set the bit of STOP and IDLE Control register (PCON)

12.4 STOP Mode

The power control register is set to ‘03h’ to enter the STOP Mode. In the stop mode, the main oscillator, system clock and peripheral clock is stopped, but watch timer continue to operate if STOP1 bit in SCCR register is written to ‘1’. With the clock frozen, all functions are stopped, but the on-chip RAM and control registers are held.

The source for exit from STOP mode is hardware reset and interrupts. The reset re-defines all the control registers.

When exit from STOP mode, enough oscillation stabilization time is required to normal operation. It is proportional to the system clock.

Oscillation stabilization time = Default 16ms @ 8kHz WDTRC

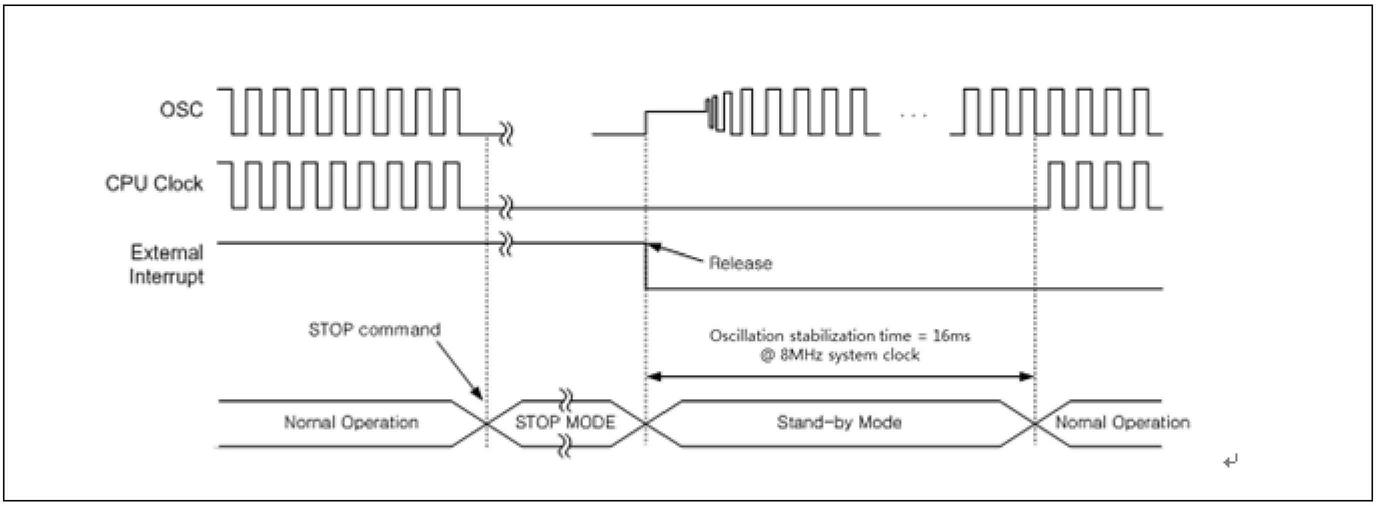


Figure 12.2 STOP Mode Release Timing by External Interrupt

12.5 Release Operation of STOP1, 2 Mode

After STOP1, 2 mode is released, the operation begins according to content of related interrupt register just before STOP1, 2 mode start (Figure 12.3). Interrupt Enable Flag of All (EA) of IE should be set to `1`. Released by only interrupt which each interrupt enable flag = `1`, and jump to the relevant interrupt service routine.

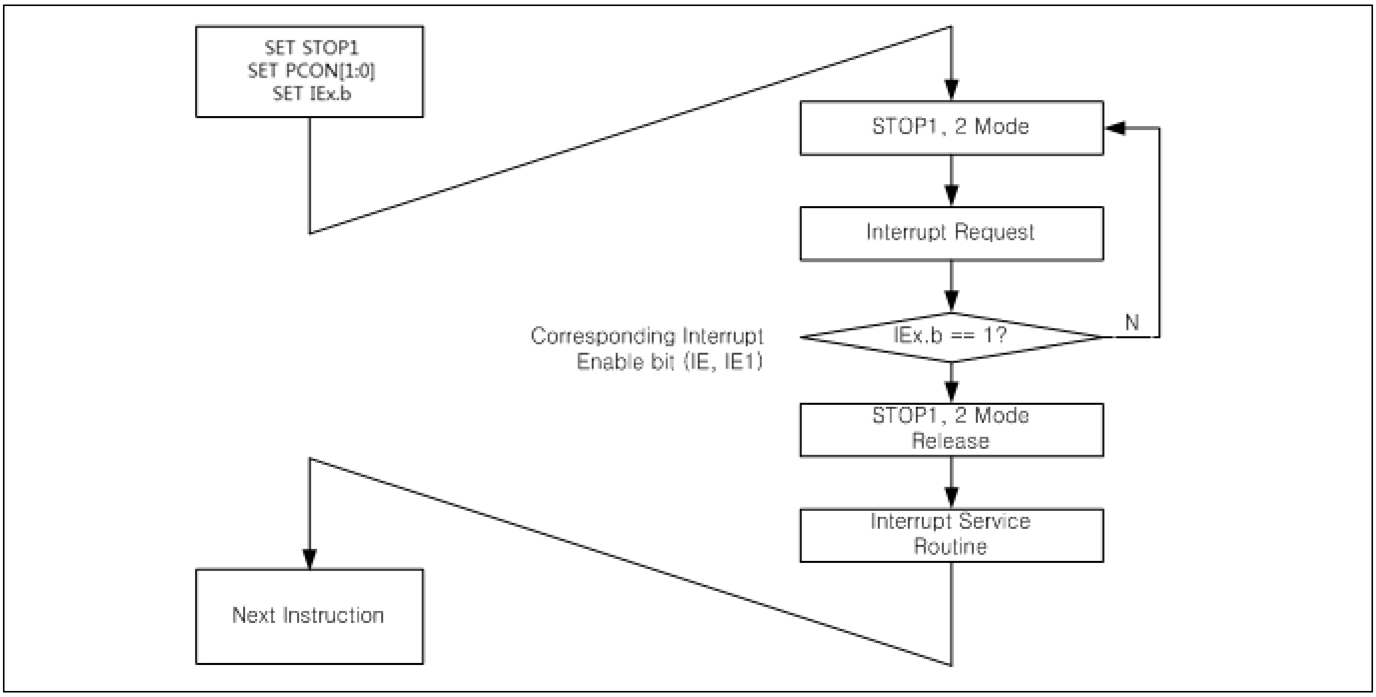


Figure 12.3 STOP1, 2 Mode Release Flow

12.5.1 Register Map and Register Description for Power Down Operation

Name	Address	Direction	Default	Description
PCON	87H	R/W	00H	Power Control Register

Table 12.2 Register Map

PCON (Power Control Register) : 87H

7	6	5	4	3	2	1	0
bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Initial value : 00H

01H	IDLE mode enable
03H	STOP1, 2 mode enable

NOTE)
1. To enter IDLE mode, PCON must be set to '01H'.
2. To STOP1, 2 mode, PCON must be set to '03H'.
   (In STOP1, 2 mode, PCON register is cleared automatically by interrupt or reset)
3. When PCON is set to '03H', if STOP1 (in the SCCR register) is set to '1', it enters the STOP1 mode. if
4. STOP1 is cleared to '0', it enters the STOP2 mode
5. The different thing in STOP 1, 2 is only clock operation of internal 8 kHz-WDTOSC during STOP mode operating.

13 RESET

13.1 Overview

The MC96F1206 has reset by external RESETB pin. The following is the hardware setting value.

On Chip Hardware	Initial Value
Program Counter (PC)	0000h
Accumulator	00h
Stack Pointer (SP)	07h
Peripheral Clock	On
Control Register	Peripheral Registers refer
Low Voltage Indicator	Enable

Table 13.1 Reset state

13.2 Reset Source

The MC96F1206 has six types of reset generation procedures. The following is the reset sources.

- External RESETB
- Power ON RESET (POR)
- WDT Overflow Reset (In the case of WDT_EN = ‘1’)
- LVR Reset
- OCD Reset
- LVI Reset (In the case of LVILS ≠ ‘000’)

13.3 RESET Block Diagram

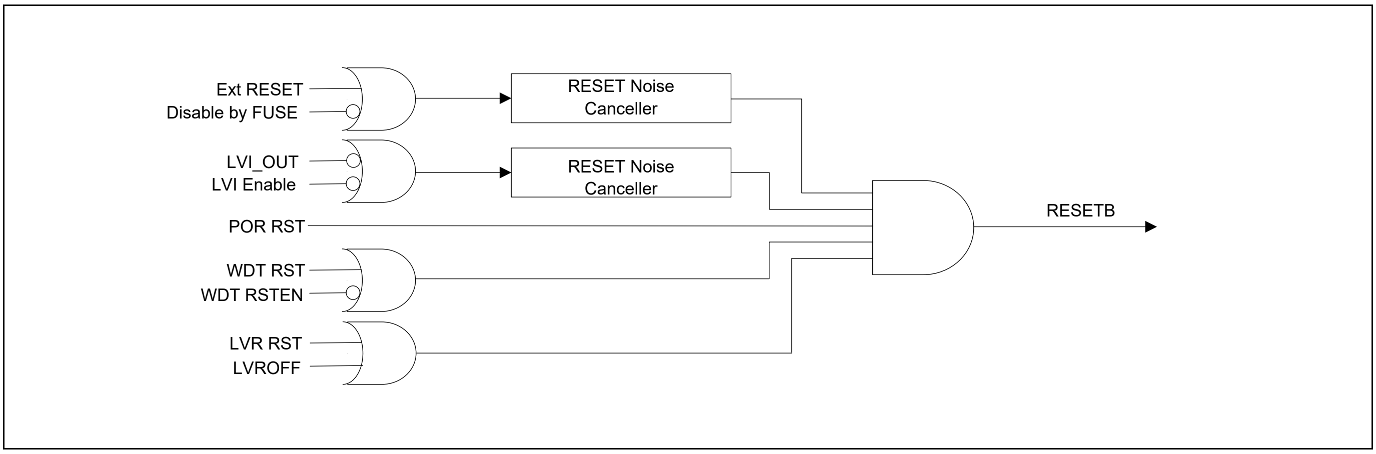


Figure 13.1 RESET Block Diagram

13.4 Power on RESET

When rising device power, the POR (Power ON Reset) have a function to reset the device. If using POR, it executes the device RESET function instead of the RESET IC or the RESET circuits. And External RESET PIN is able to use as Normal I/O pin.

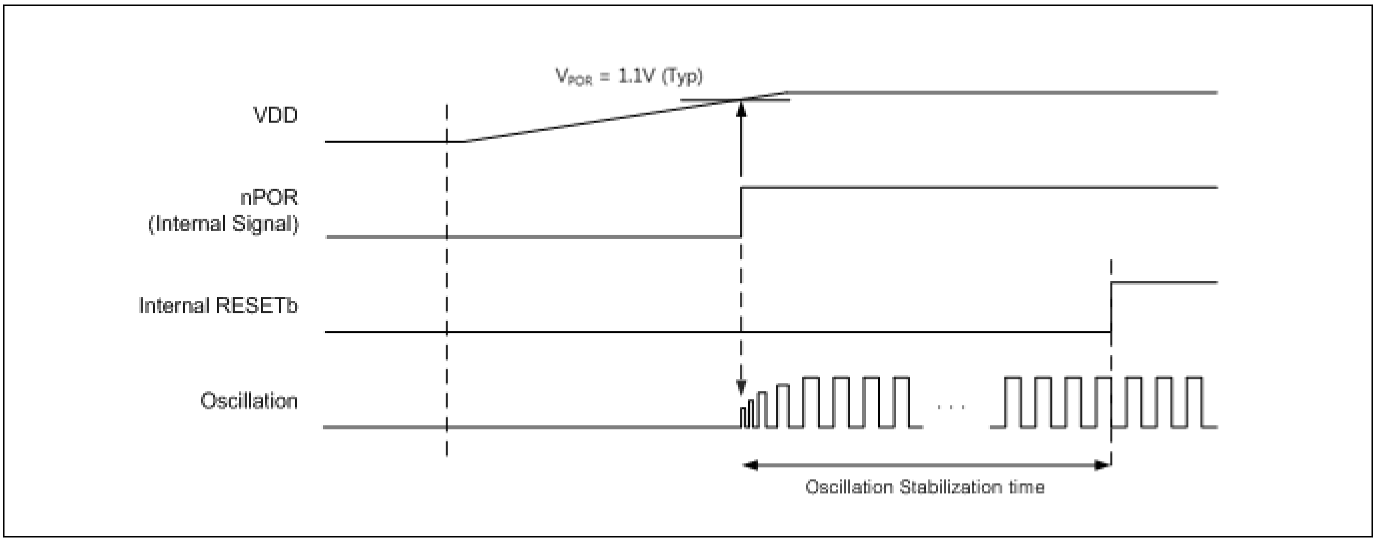


Figure 13.2 Internal RESET Release Timing On Power-Up

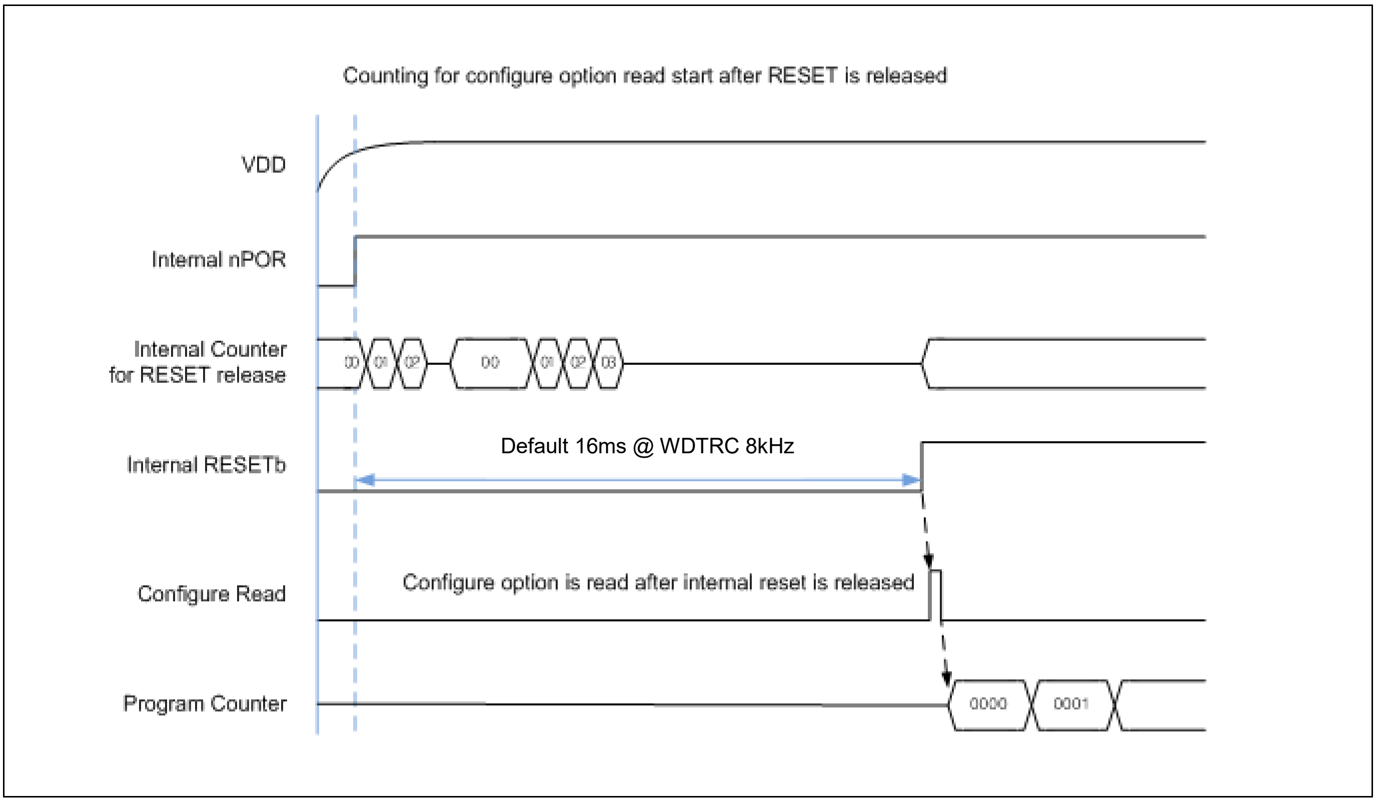

Counting for configure option read start after RESET is released
VDD
Internal nPOR
Internal Counter
for RESET release
00
01
02
00
01
02
03
Internal RESETb
Default 16ms @ WDTRC 8kHz
Configure Read
Configure option is read after internal reset is released
Program Counter
0000
0001

Figure 13.3 Configuration timing when Power-on

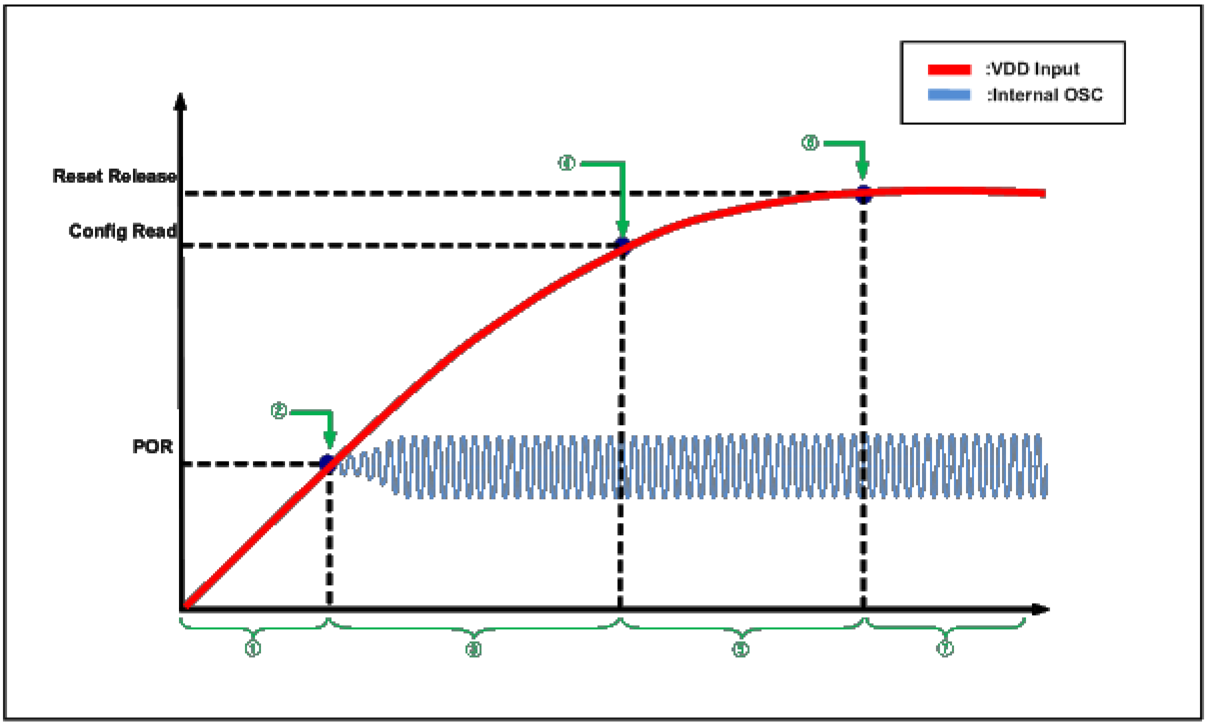


Figure 13.4 Boot Process Waveform

Process	Description	Remarks
①	-No Operation	
②	-1st POR level Detection -Internal OSC (32MHz) ON	-about 1.2V ~ 1.6V
③	-Delay section (=12ms) -VDD input voltage must rise over than flash operating voltage for Config read	-Slew Rate >= 0.05V/ms
④	- Config read point	-about 1.5V ~ 1.6V -Config Value is determined by Writing Option
⑤	- Rising section to Reset Release Level	-16ms point after POR or EXT_reset release
⑥	- Reset Release section (BIT overflow) i) after16ms, after External Reset Release (External reset) ii) 16ms point after POR (POR only)	- BIT is used for Peripheral stability
⑦	-Normal operation	

Table 13.2 Boot Process Description

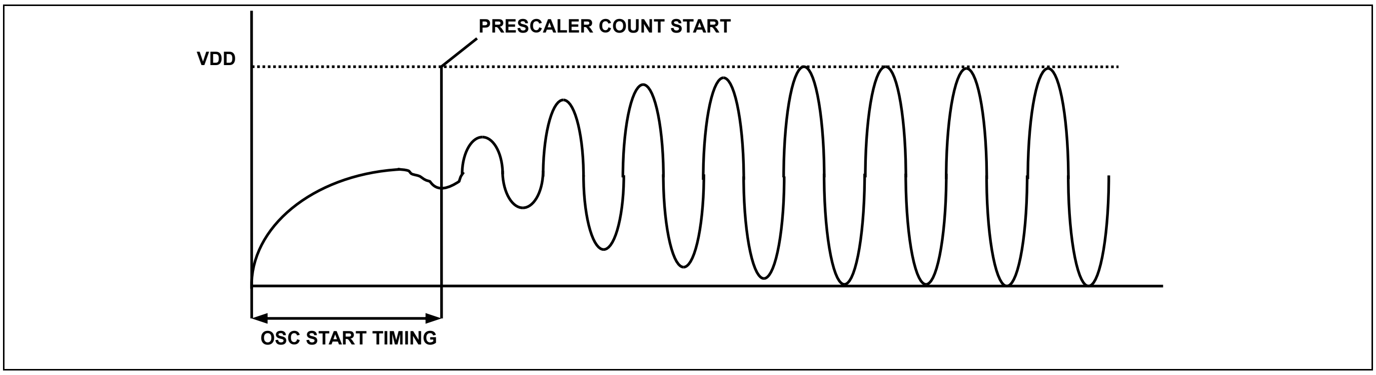


Figure 13.5 Oscillator generating waveform example

NOTE) As shown Figure 13.5, the stable generating time is not included in the start-up time.

13.5 External RESETB Input

The External RESETB is the input to a Schmitt trigger. A reset in accomplished by holding the reset pin low for at least 10us over, within the operating voltage range and oscillation stable, it is applied, and the internal state is initialized. After reset state becomes ‘1’, it needs the stabilization time with default 16ms and after the stable state, the internal RESET becomes ‘1’. And the program execution starts at the vector address stored at address 0000H.

The Figure 13.6 is the Noise canceller time diagram. It has the Noise cancel value of about 500us (@V_{DD}=5V) to the low input of System Reset.

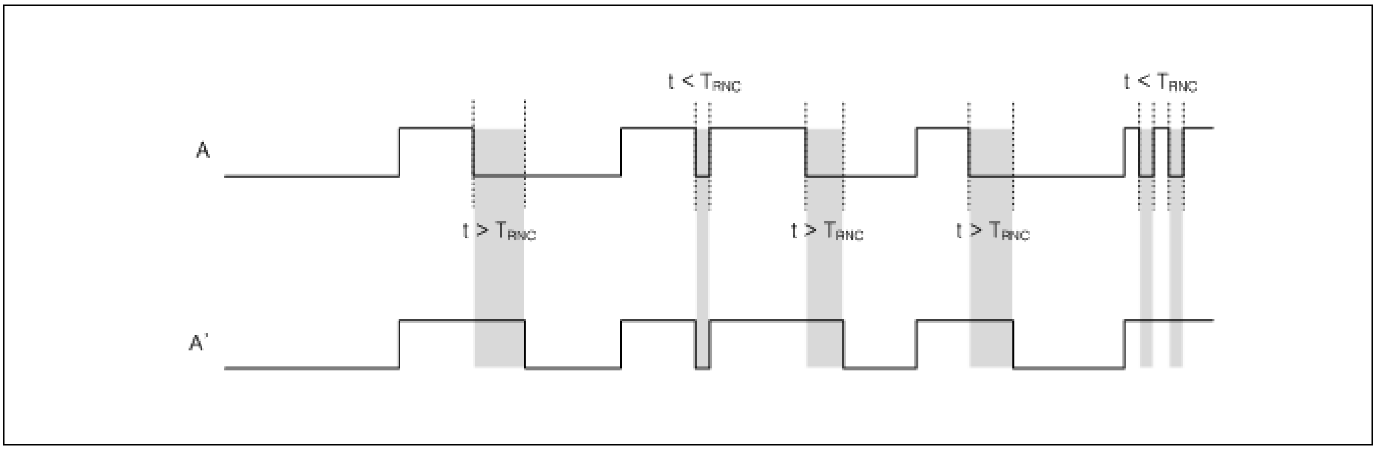


Figure 13.6 Reset noise canceller time diagram

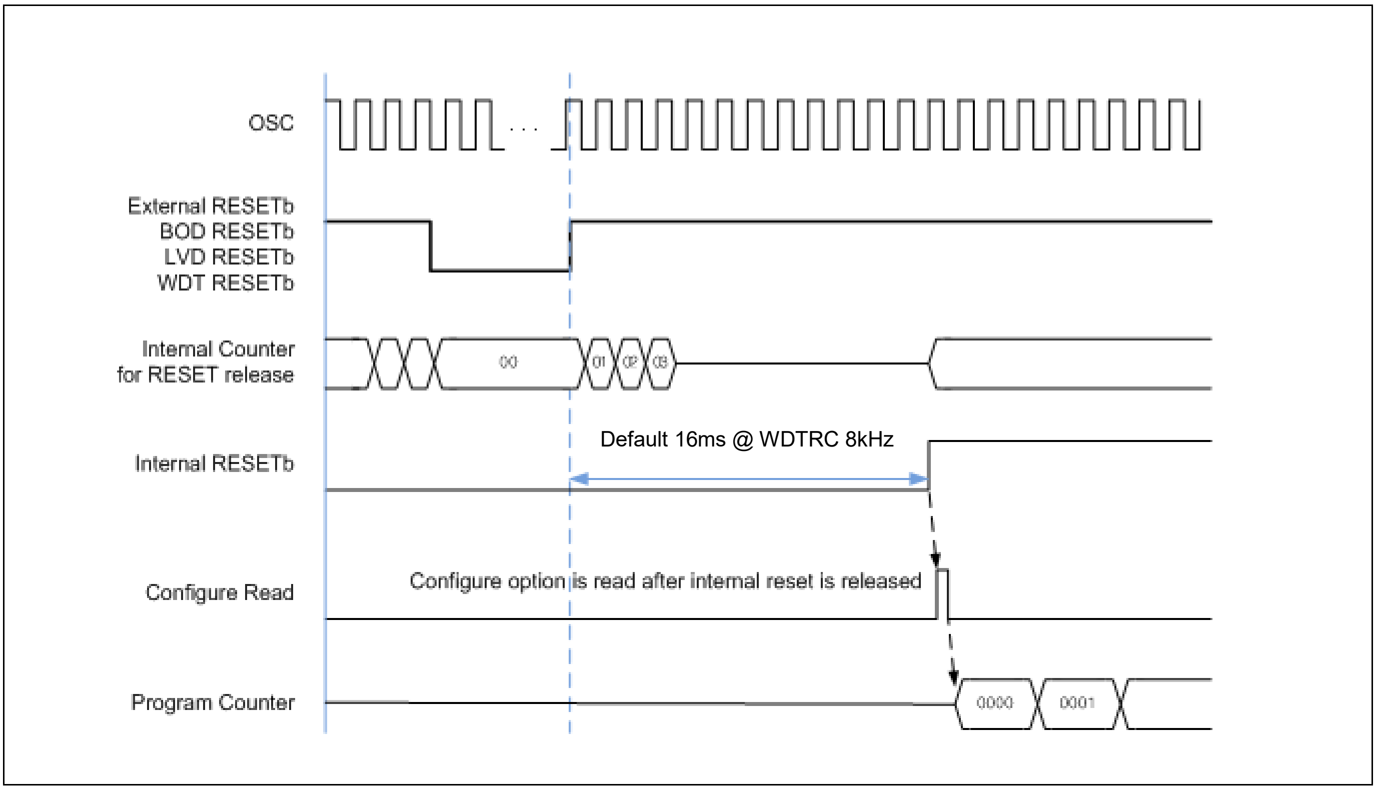

OSC
External RESETb
BOD RESETb
LVD RESETb
WDT RESETb
Internal Counter for RESET release
00
01
02
03
Internal RESETb
Default 16ms @ WDTRC 8kHz
Configure Read
Configure option is read after internal reset is released
Program Counter
0000
0001

Figure 13.7 Timing Diagram after RESET

13.6 Low Voltage Indicator Processor

The MC96F1206 has an On-chip Low Voltage Indicator circuit for monitoring the VDD level during operation by comparing it to a fixed trigger level. The trigger level for the LVI can be selected by LVILS[2:0]. In the STOP mode, this will contribute significantly to the total current consumption. So to minimize the current consumption, the LVILS[2:0] is set to off by software.

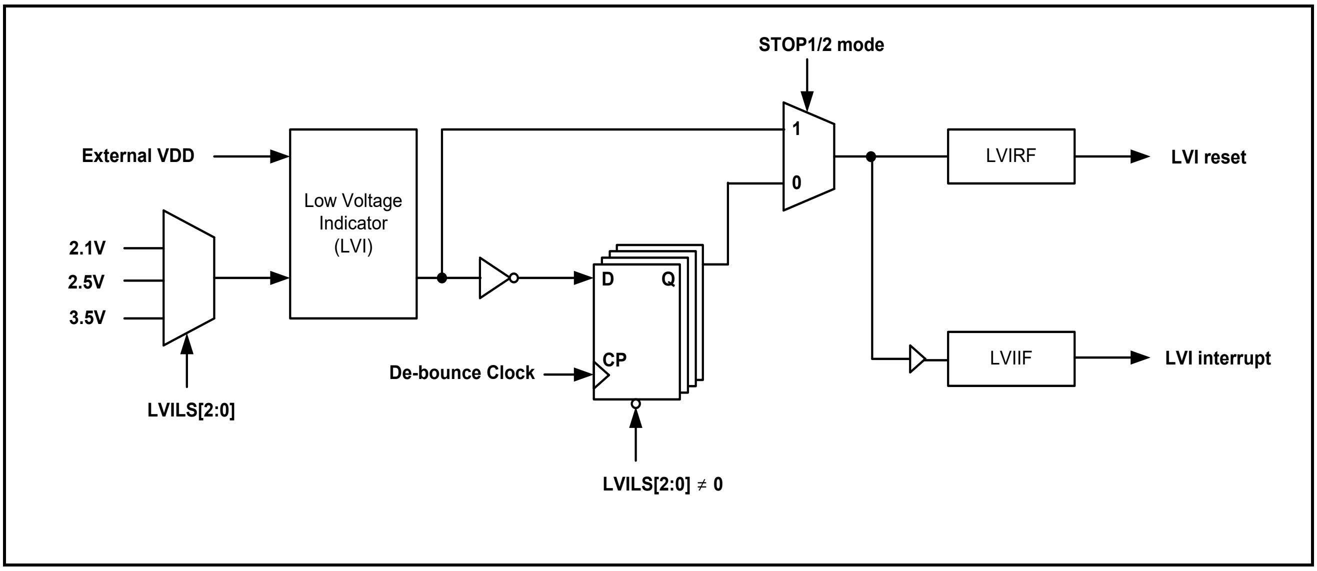


Figure 13.8 Block Diagram of LVI

13.6.1 Register Map

Name	Address	Dir	Default	Description
RSFR	86H	R/W	84H	Reset Source Flag Register
LVIR	8FH	R/W	40H	LVI Control Register

Table 13.3 Register Map

13.6.2 Register Description for Reset Operation

RSFR (Reset Source Flag Register) : 86H

7	6	5	4	3	2	1	0
PORF	EXTRF	WDTRF	OCDRF	LVIRF	LVRRF	-	-
R/W	R/W	R/W	R/W	R/W	R/W	-	-

Initial value : C4H

PORF Power-On Reset flag bit. The bit is reset by writing ‘0’ to this bit.

0 No detection

1 Detection

EXTRF External Reset flag bit. The bit is reset by writing ‘0’ to this bit or by Power ON reset.

0 No detection

1 Detection

WDTRF Watch Dog Reset flag bit. The bit is reset by writing ‘0’ to this bit or by Power ON reset.

0 No detection

1 Detection

OCDRF On-Chip Debug Reset flag bit. The bit is reset by writing ‘0’ to this bit or by Power ON reset.

0 No detection

1 Detection

LVIRF Low Voltage Indicator Reset flag bit. The bit is reset by writing ‘0’ to this bit or by Power ON reset.

0 No detection

1 Detection

LVRRF Low Voltage Reset flag bit. The bit is reset by writing ‘0’ to this bit or by Power ON reset.

0 No detection

1 Detection

LVIR (LVI Control Register) : 8FH

7	6	5	4	3	2	1	0
-	LVIINTON	-	-	-	LVILS2	LVILS1	LVILS0
-	R/W	-	-	-	R/W	R/W	R/W

Initial value : 40H

LVIINTON Select LVI reset or Interrupt

0	Reset
1	Interrupt

LVILS[2:0] LVI level Voltage

LVILS2	LVILS1	LVILS0	Description
0	0	0	LVI disable (default)
0	0	1	2.1V
0	1	0	LVI disable
0	1	1	2.5V
1	0	0	LVI disable
1	0	1	3.5V
1	1	0	LVI disable
1	1	1	LVI disable

14 On-chip Debug System

14.1 Overview

14.1.1 Description

On-chip debug System (OCD2) of MC96F1206 can be used for programming the non-volatile memories and on-chip debugging. Detailed descriptions for programming via the OCD2 interface can be found in the following chapter. Figure 14.1 shows a block diagram of the OCD2 interface and the On-chip Debug system.

14.1.2 Feature

- Two-wire external interface: 1-wire serial clock input, 1-wire bi-directional serial data bus
- Debugger Access to:
  - All Internal Peripheral Units
  - Internal data RAM
  - Program Counter
  - Flash Memories
- Extensive On-chip Debug Support for Break Conditions, Including
  - Break Instruction
  - Single Step Break
  - Program Memory Break Points on Single Address
  - Programming of Flash, EEPROM, Fuses, and Lock bits through the two-wire Interface
  - On-chip Debugging Supported by OCD2 Dongle
- Operating frequency

  Supports the maximum frequency of the target MCU

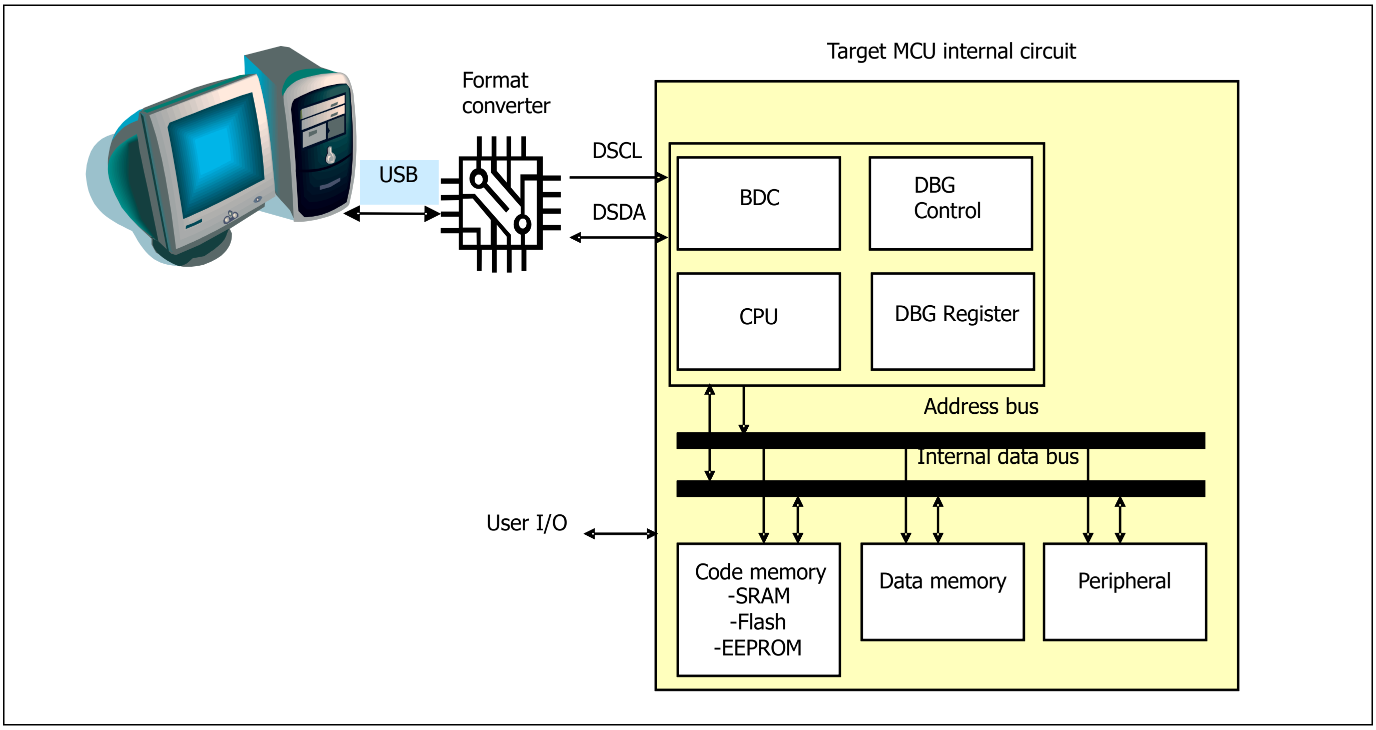


Figure 14.1 Block Diagram of On-chip Debug System

14.2 Two-Pin External Interface

14.2.1 Basic Transmission Packet

- 10-bit packet transmission using two-pin interface.
- 1-packet consists of 8-bit data, 1-bit parity and 1-bit acknowledge.
- Parity is even of ‘1’ for 8-bit data in transmitter.
- Receiver generates acknowledge bit as ‘0’ when transmission for 8-bit data and its parity has no error.
- When transmitter has no acknowledge (Acknowledge bit is ‘1’ at tenth clock), error process is executed in transmitter.
- When acknowledge error is generated, host PC makes stop condition and transmits command which has error again.
- Background debugger command is composed of a bundle of packet.
- Star condition and stop condition notify the start and the stop of background debugger command respectively.

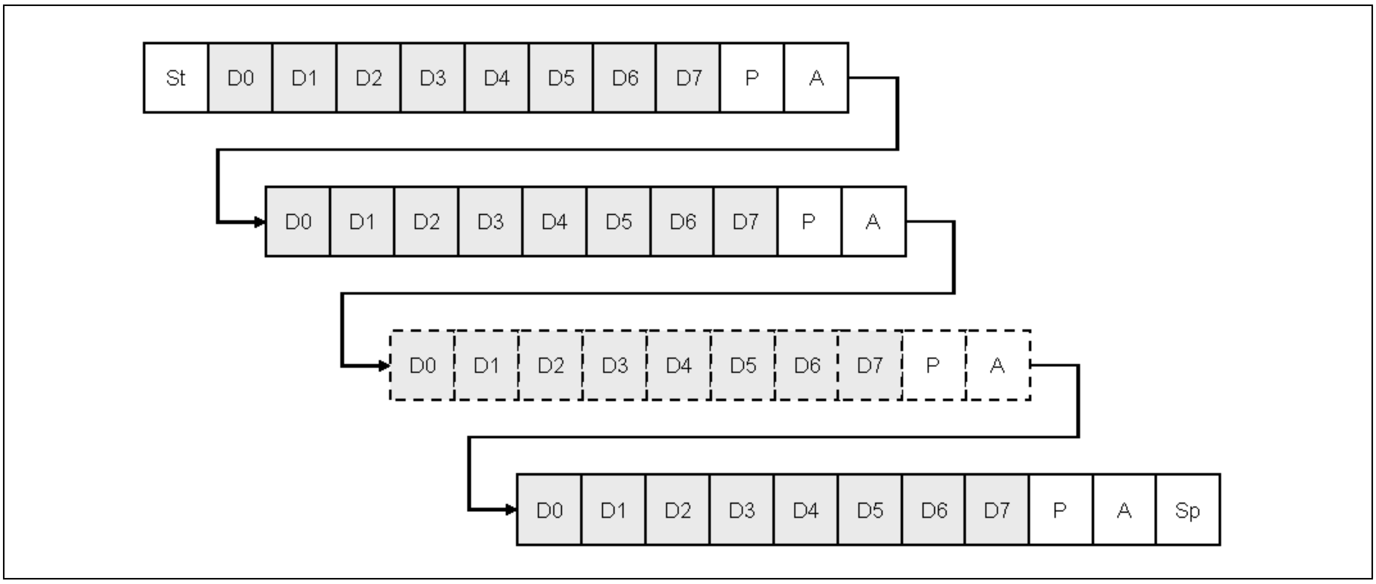


Figure 14.2 10-bit transmission packet

14.2.2 Packet Transmission Timing

14.2.2.1 Data Transfer

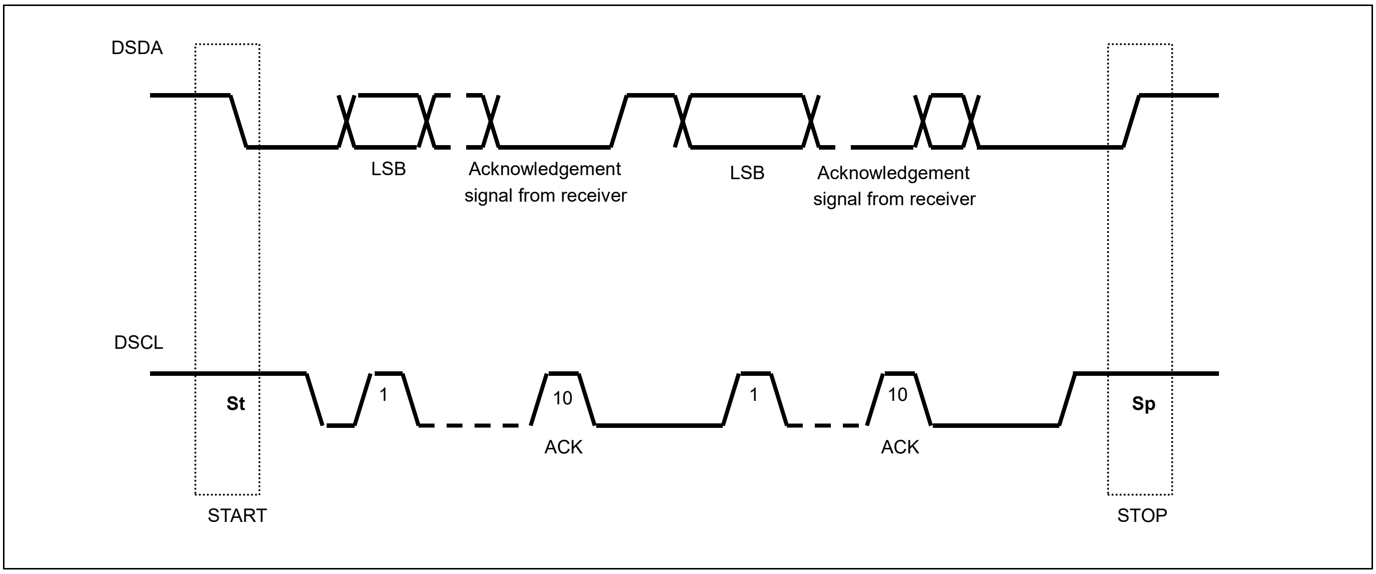

DSDA
LSB
Acknowledgement signal from receiver
LSB
Acknowledgement signal from receiver
DSCL
St
1
10
ACK
1
10
ACK
Sp
START
STOP

Figure 14.3 Data transfer on the twin bus

14.2.2.2 Bit Transfer

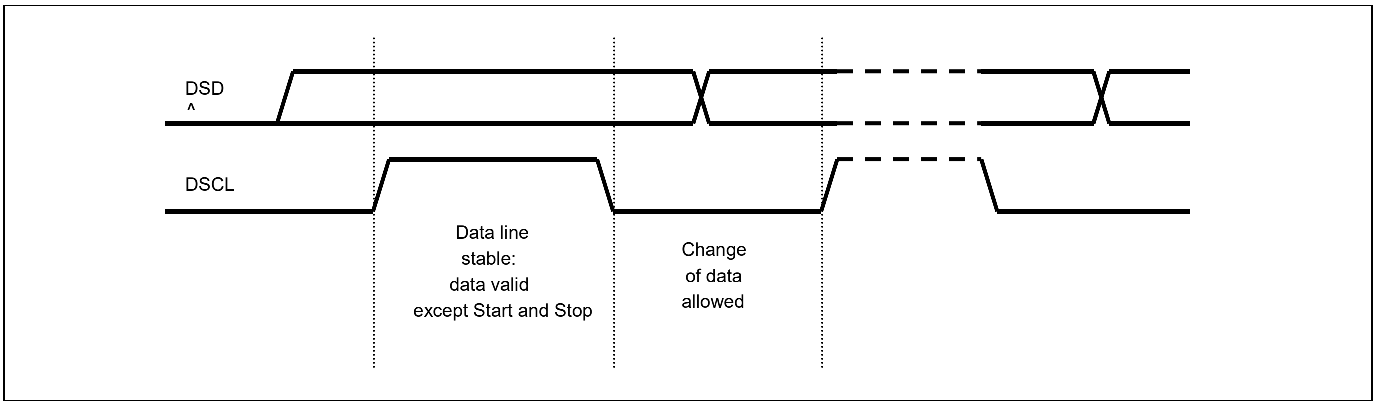


Figure 14.4 Bit transfer on the serial bus

14.2.2.3 Start and Stop Condition

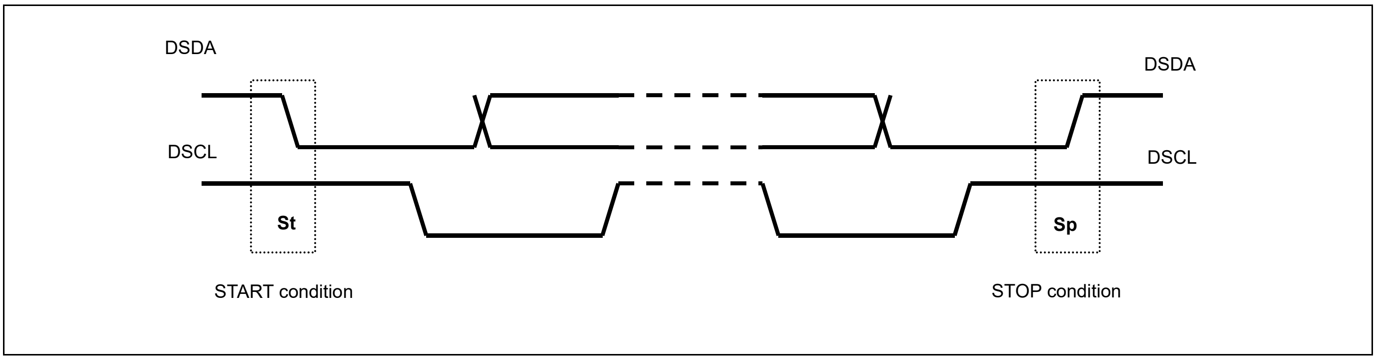


Figure 14.5 Start and stop condition

14.2.2.4 Acknowledge bit

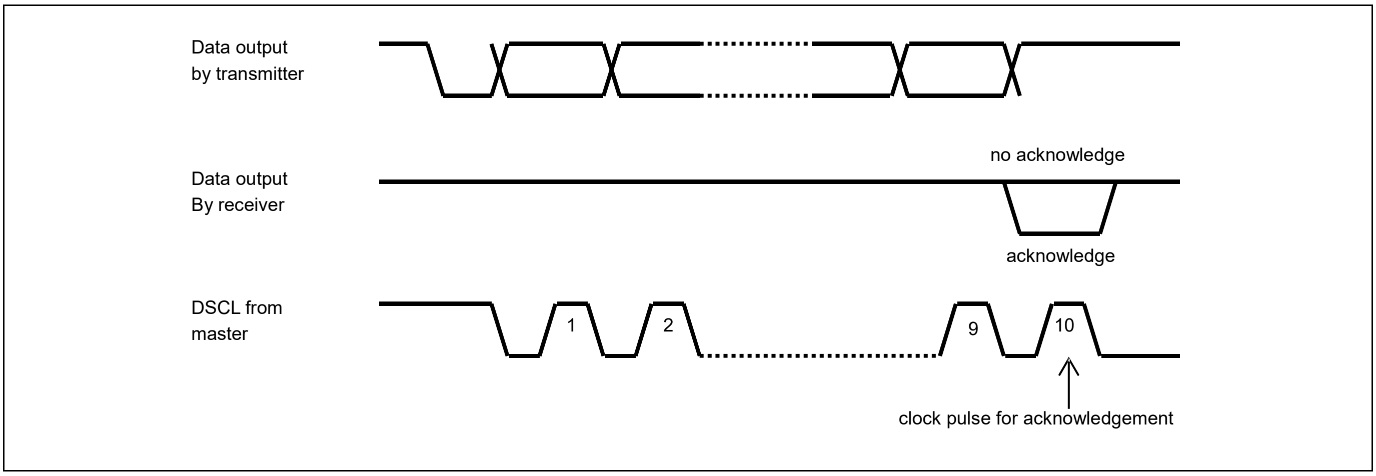


Figure 14.6 Acknowledge on the serial bus

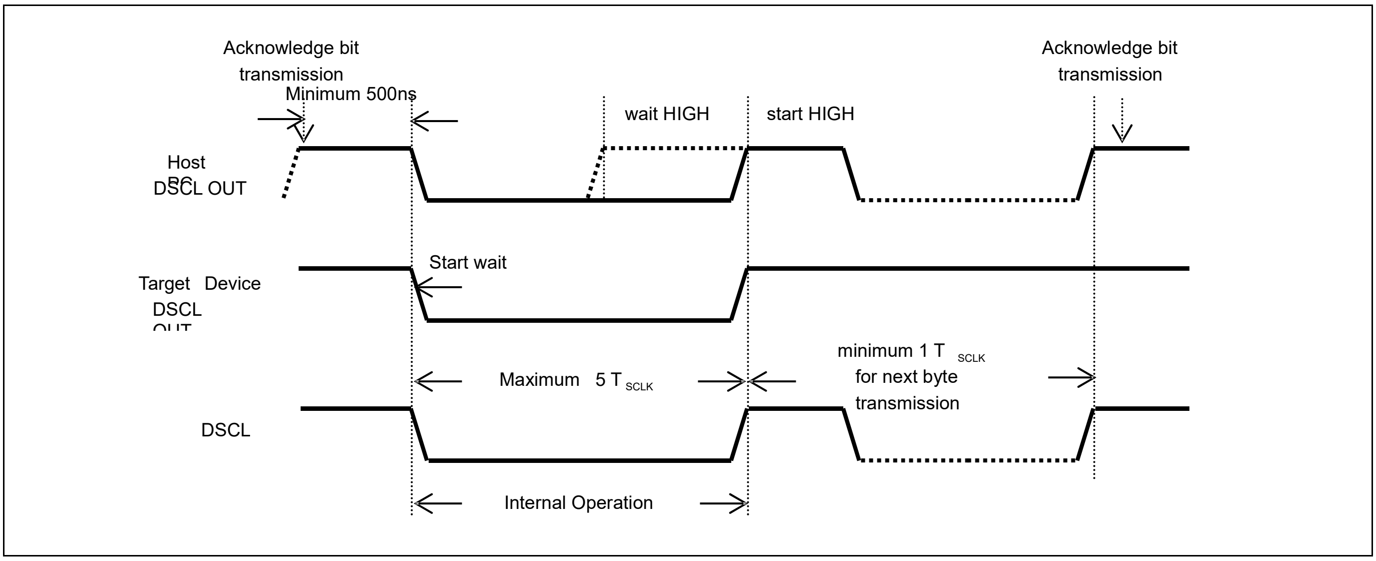


Figure 14.7 Clock synchronization during wait procedure

14.2.3 Connection of Transmission

Two-pin interface connection uses open-drain(wire-AND bidirectional I/O).

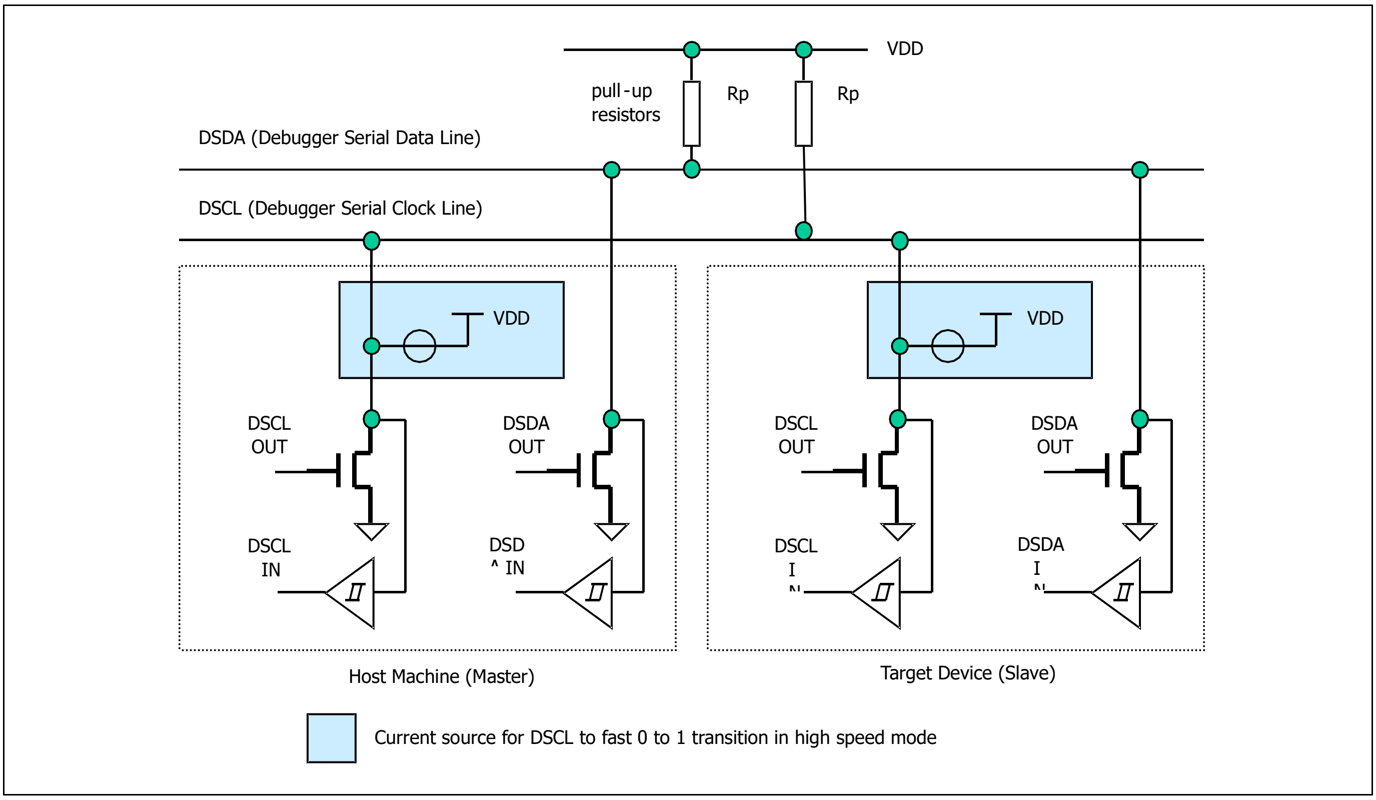

VDD
pull-up resistors
Rp
Rp
DSDA (Debugger Serial Data Line)
DSCL (Debugger Serial Clock Line)
VDD
VDD
DSCL OUT
DSDA OUT
DSCL IN
DSDA IN
DSCL OUT
DSDA OUT
DSCL IN
DSDA IN
Host Machine (Master)
Target Device (Slave)
Current source for DSCL to fast 0 to 1 transition in high speed mode

Figure 14.8 Connection of transmission

15 Memory Programming

15.1 Overview

15.1.1 Description

MC96F1206 has flash memory to which a program can be written, erased, and overwritten while mounted on the board. Serial ISP mode is supported.

15.1.2 Features

- Flash Size : 6Kbytes
- Single power supply program and erase
- Command interface for fast program and erase operation
- Up to 10,000 program/erase cycles at typical voltage and temperature for flash memory
- Security feature

15.2 Flash Control and status register

Registers to control Flash are Mode Register (FEMR), Control Register (FECR), Status Register (FESR), Time Control Register (FETCR), Address Low Register (FEARL), Address Middle Register (FEARM) and address High Register (FEARH). They are mapped to SFR area and can be accessed only in programming mode.

15.2.1 Register Map

Name	Address	Dir	Default	Description
FEMR	EAH	R/W	00H	Flash Mode Register
FECR	EBH	R/W	03H	Flash Control Register
FESR	ECH	R/W	80H	Flash Status Register
FETCR	EDH	R/W	00H	Flash Time Control Register
FEARL	F2H	R/W	00H	Flash Address Low Register
FEARM	F3H	R/W	00H	Flash Address Middle Register
FEARH	F4H	R/W	00H	Flash Address High Register

Table 15.1 Register Map

15.2.2 Register Description for Flash

FEMR (Flash Mode Register) : EAH

7	6	5	4	3	2	1	0
FSEL	-	PGM	ERASE	PBUFF	OTPE	VFY	FEEN
R/W	-	R/W	R/W	R/W	R/W	R/W	R/W

Initial value : 00H

FSEL Select flash memory.

0 Deselect flash memory

1 Select flash memory

PGM Enable program or program verify mode with VFY

0 Disable program or program verify mode

1 Enable program or program verify mode

ERASE Enable erase or erase verify mode with VFY

0 Disable erase or erase verify mode

1 Enable erase or erase verify mode

PBUFF Select page buffer

0 Deselect page buffer

1 Select page buffer

OTPE Select OTP area instead of program memory

0 Deselect OTP area

1 Select OTP area

VFY Set program or erase verify mode with PGM or ERASE

Program Verify: PGM=1, VFY=1

Erase Verify: ERASE=1, VFY=1

FEEN Enable program and erase of Flash. When inactive, it is possible to read as normal mode

0 Disable program and erase

1 Enable program and erase

FEARL (Flash address low Register) : F2H

7	6	5	4	3	2	1	0
ARL7	ARL6	ARL5	ARL4	ARL3	ARL2	ARL1	ARL0
W	W	W	W	W	W	W	W

Initial value : 00H

ARL[7:0] Flash address low

FECR (Flash Control Register) : EBH

7	6	5	4	3	2	1	0
AEF	-	EXIT1	EXIT0	WRITE	READ	nFERST	nPBRST
R/W	-	R/W	R/W	R/W	R/W	R/W	R/W

Initial value : 03H

AEF Enable flash bulk erase mode

0 Disable bulk erase mode of Flash memory

1 Enable bulk erase mode of Flash memory

EXIT[1:0] Exit from program mode. It is cleared automatically after 1 clock

EXIT1	EXIT0	Description
0	0	Don’t exit from program mode
0	1	Don’t exit from program mode
1	0	Don’t exit from program mode
1	1	Exit from program mode

WRITE Start to program or erase of Flash. It is cleared automatically after 1 clock

0 No operation

1 Start to program or erase of Flash

READ Start auto-verify of Flash. It is cleared automatically after 1 clock

0 No operation

1 Start auto-verify of Flash

nFERST Reset Flash control logic. It is cleared automatically after 1 clock

0 No operation

1 Reset Flash control logic.

nPBRST Reset page buffer with PBUFF. It is cleared automatically after 1 clock

PBUFF	nPBRST	Description
0	0	Page buffer reset
1	0	Write checksum reset

WRITE and READ bits can be used in program, erase and verify mode with FEAR registers. Read or writes for memory cell or page buffer uses read and write enable signals from memory controller. Indirect address mode with FEAR is only allowed to program, erase and verify

FESR (Flash Status Register) : ECH

7	6	5	4	3	2	1	0
PEVBSY	VFYGOOD	-	-	ROMINT	WMODE	EMODE	VMODE
R	R/W	R	R	R/W	R	R	R

Initial value : 80H

PEVBSY Operation status flag. It is cleared automatically when operation starts. Operations are program, erase or verification

0	Busy (Operation processing)
1	Complete Operation

VFYGOOD Auto-verification result flag.

0	Auto-verification fails
1	Auto-verification successes

ROMINT Flash interrupt request flag. Auto-cleared when program/erase/verify starts. Active in program/erase/verify completion

0	No interrupt request.
1	Interrupt request.

WMODE	Write mode flag
EMODE	Erase mode flag
VMODE	Verify mode flag

FEARM (Flash address middle Register) : F3H

7	6	5	4	3	2	1	0
ARM7	ARM6	ARM5	ARM4	ARM3	ARM2	ARM1	ARM0
W	W	W	W	W	W	W	W

Initial value : 00H

ARM[7:0] Flash address middle

FEARH (Flash address high Register) : F4H

7	6	5	4	3	2	1	0
ARH7	ARH6	ARH5	ARH4	ARH3	ARH2	ARH1	ARH0
W	W	W	W	W	W	W	W

Initial value : 00H

ARH[7:0] Flash address high

FEAR registers are used for program, erase and auto-verify. In program and erase mode, it is page address and ignored the same least significant bits as the number of bits of page address. In auto-verify mode, address increases automatically by one.

FEARs are write-only register. Reading these registers returns 24-bit checksum result

FETCR (Flash Time control Register) : EDH

7	6	5	4	3	2	1	0
TCR7	TCR6	TCR5	TCR4	TCR3	TCR2	TCR1	TCR0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Initial value : 00H

TCR[7:0] Flash Time control

Program and erase time is controlled by setting FETCR register. Program and erase timer uses 10-bit counter. It increases by one at each divided system clock frequency(=SCLK/128). It is cleared when program or erase starts. Timer stops when 10-bit counter is same to FETCR. PEVBSY is cleared when program, erase or verify starts and set when program, erase or verify stops.

Max program/erase time at 16Mhz system clock : (255+1) * 2 * (62.5ns * 128) = 4.096ms

In the case of 10% of error rate of counter source clock, program or erase time is 3.6~4.5ms

* * Program/erase time calculation

for page write or erase, Tpe = (TCON+1) * 2 * (SCLK * 128)

for bulk erase, Tbe = (TCON+1) * 4 * (SCLK * 128)

	Min	Typ	Max	Unit
program/erase Time	2.4	2.5	2.6	ms

Table 15.2 Program/erase Time

※ Recommended program/erase time at 16MHz (FETCR = 9Dh)

15.3 Memory map

15.3.1 Flash Memory Map

Program memory uses 6-Kbyte of Flash memory. It is read by byte and written by page. One page is 32-byte

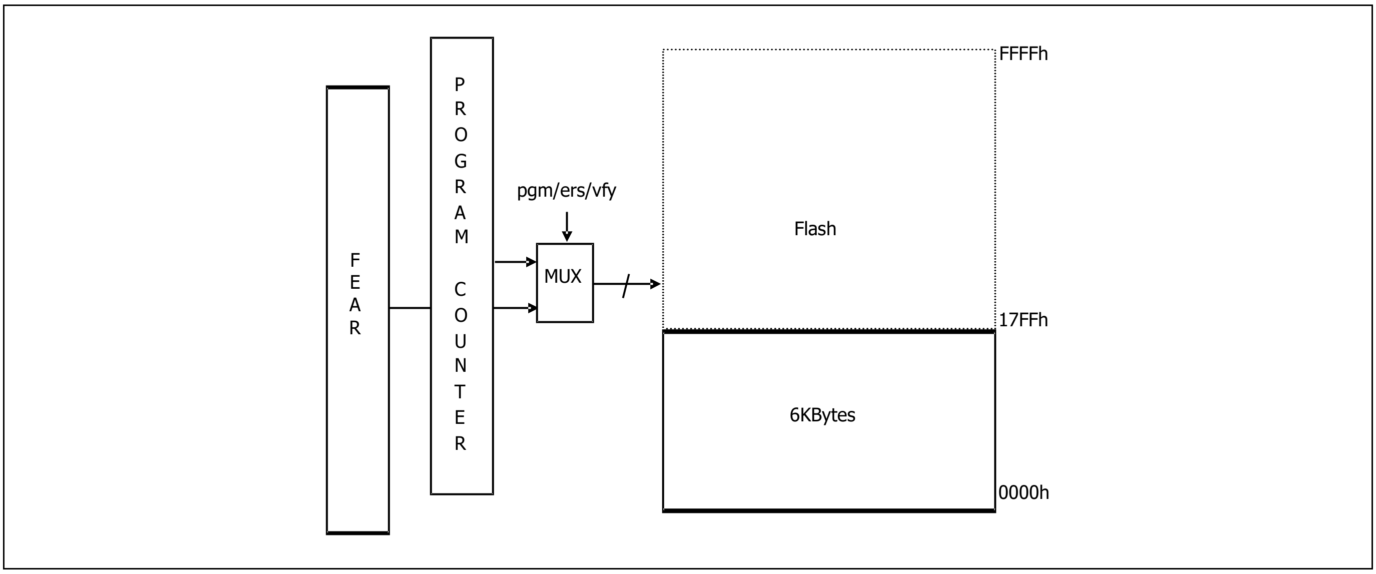
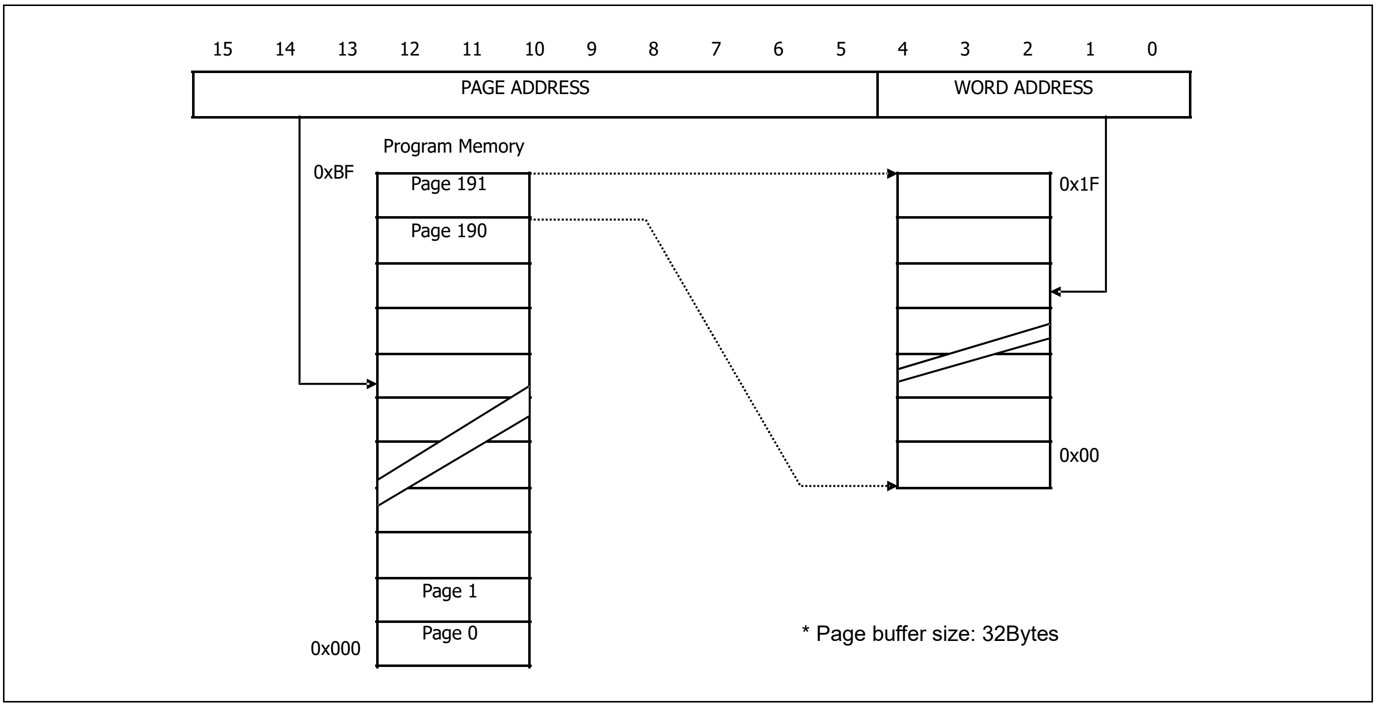


Figure 15.1 Flash Memory Map



* Page buffer size: 32Bytes

Figure 15.2 Address configuration of Flash memory

15.4 Serial In-System Program Mode

Serial in-system program uses the interface of debugger which uses two wires. Refer to chapter 14 in details about debugger.

15.4.1 Flash operation

Configuration (This Configuration is just used for follow description)

7	6	5	4	3	2	1	0
-	FEMR[4] &[1]	FEMR[5] &[1]	-	-	FEMR[2]	FECR[6]	FECR[7]
-	ERASE&VFY	PGM&VFY	-	-	OTPE	AEE	AEF

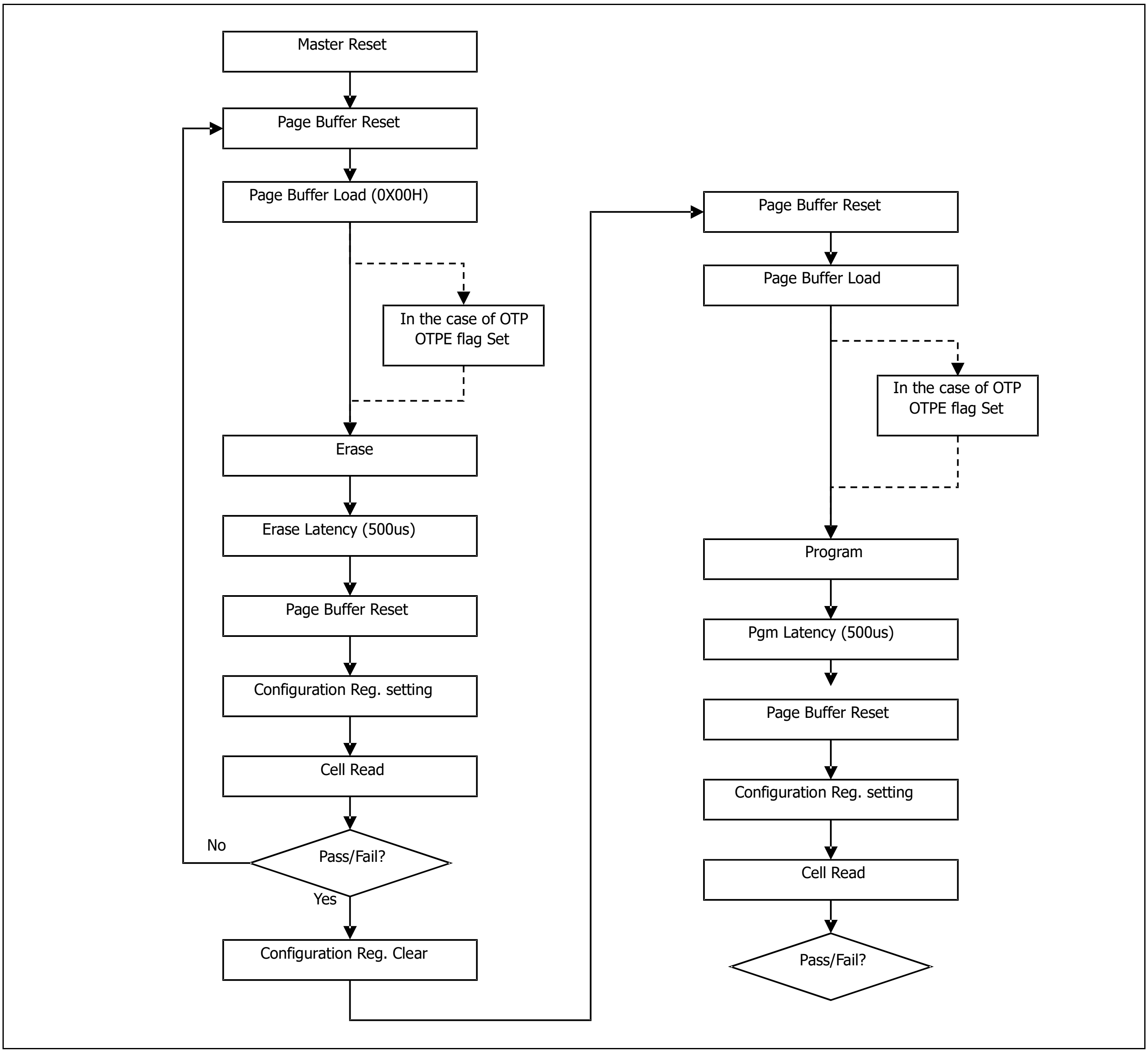


Figure 15.3 The sequence of page program and erase of Flash memory

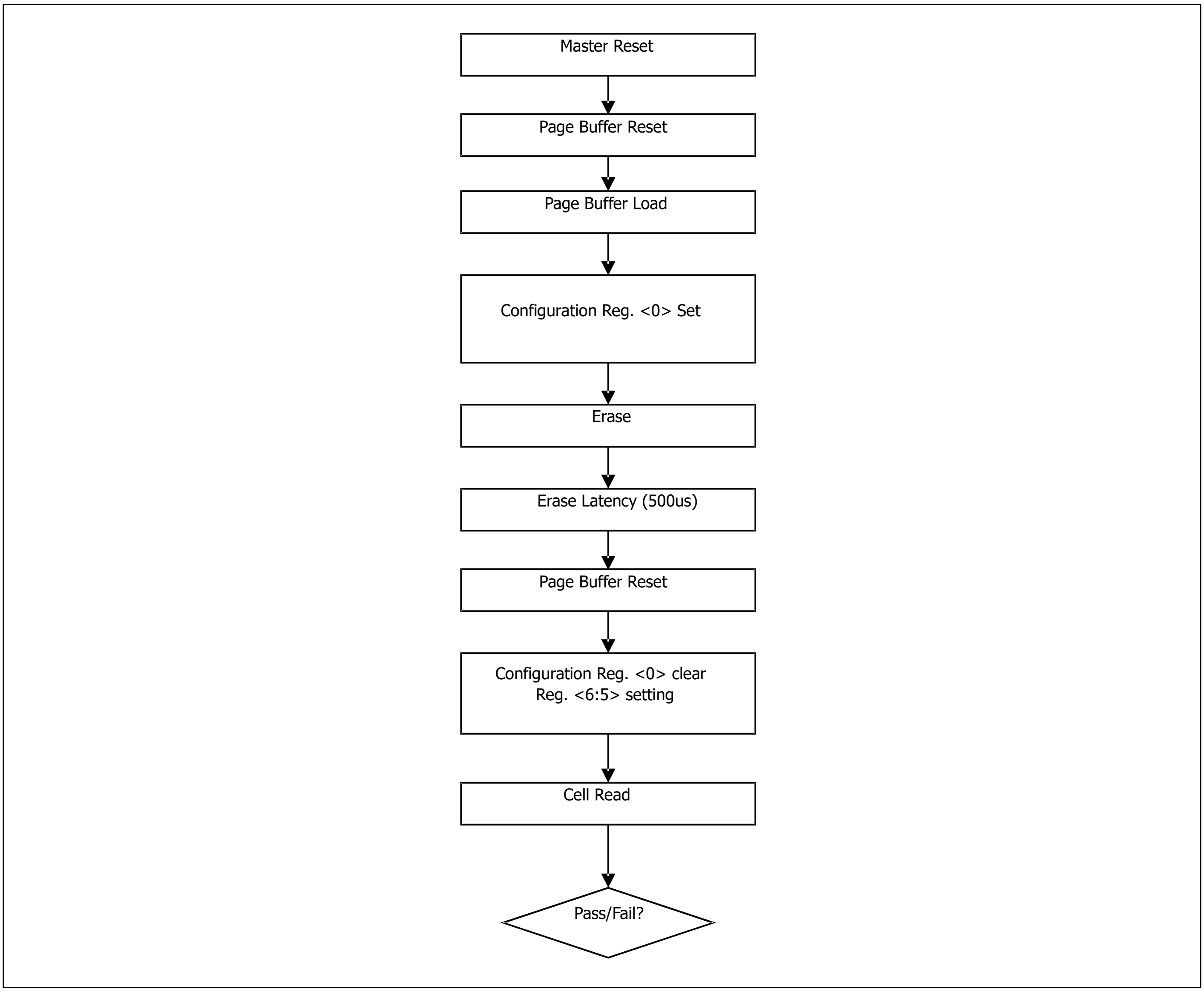


Figure 15.4 The sequence of bulk erase of Flash memory

15.4.1.1 Flash Read

Step 1. Enter OCD(=ISP) mode.

Step 2. Set ENBDM bit of BCR.

Step 3. Enable debug and Request debug mode.

Step 4. Read data from Flash.

15.4.1.2 Enable program mode

Step 1. Enter OCD(=ISP) mode.[1]

Step 2. Set ENBDM bit of BCR.

Step 3. Enable debug and Request debug mode.

Step 4. Enter program/erase mode sequence.[2]

(1) Write 0xAA to 0xF555.

(2) Write 0x55 to 0xFAAA.

(3) Write 0xA5 to 0xF555.

[1] Refer to how to enter ISP mode..

[2] Command sequence to activate Flash write/erase mode. It is composed of sequentially writing data of Flash memory.

15.4.1.3 Flash write mode

Step 1. Enable program mode.

Step 2. Reset page buffer. FEMR: 1000_0001 FECR:0000_0010

Step 3. Select page buffer. FEMR:1000_1001

Step 4. Write data to page buffer.(Address automatically increases by twin.)

Step 5. Set write mode. FEMR:1010_0001

Step 6. Set page address. FEARH:FEARM:FEARL=20'hx_xxxx

Step 7. Set FETCR.

Step 8. Start program. FECR:0000_1011

Step 9. Insert one NOP operation

Step 10. Read FESR until PEVBSY is 1.

Step 11. Repeat step2 to step 8 until all pages are written.

15.4.1.4 Flash page erase mode

Step 1. Enable program mode.

Step 2. Reset page buffer. FEMR: 1000_0001 FECR:0000_0010

Step 3. Select page buffer. FEMR:1000_1001

Step 4. Write 'h00 to page buffer. (Data value is not important.)

Step 5. Set erase mode. FEMR:1001_0001

Step 6. Set page address. FEARH:FEARM:FEARL=20'hx_xxxx

Step 7. Set FETCR.

Step 8. Start erase. FECR:0000_1011

Step 9. Insert one NOP operation

Step 10. Read FESR until PEVBSY is 1.

Step 11. Repeat step2 to step 8 until all pages are erased.

15.4.1.5 Flash bulk erase mode

Step 1. Enable program mode.

Step 2. Reset page buffer. FEMR: 1000_0001 FECR:0000_0010

Step 3. Select page buffer. FEMR:1000_1001

Step 4. Write 'h00 to page buffer. (Data value is not important.)

Step 5. Set erase mode. FEMR:1001_0001.

(Only main cell area is erased. For bulk erase including OTP area, select OTP area.(set FEMR to 1000_1101.)

Step 6. Set FETCR

Step 7. Start bulk erase. FECR:1000_1011

Step 8. Insert one NOP operation

Step 9. Read FESR until PEVBSY is 1.

15.4.1.6 Flash OTP area read mode

Step 1. Enter OCD(=ISP) mode.

Step 2. Set ENBDM bit of BCR.

Step 3. Enable debug and Request debug mode.

Step 4. Select OTP area. FEMR:1000_0101

Step 5. Read data from Flash.

15.4.1.7 Flash OTP area write mode

Step 1. Enable program mode.

Step 2. Reset page buffer. FEMR: 1000_0001 FECR:0000_0010

Step 3. Select page buffer. FEMR:1000_1001

Step 4. Write data to page buffer.(Address automatically increases by twin.)

Step 5. Set write mode and select OTP area. FEMR:1010_0101

Step 6. Set page address. FEARH:FEARM:FEARL=20'hx_xxxx

Step 7. Set FETCR.

Step 8. Start program. FECR:0000_1011

Step 9. Insert one NOP operation

Step 10. Read FESR until PEVBSY is 1.

15.4.1.8 Flash OTP area erase mode

Step 1. Enable program mode.

Step 2. Reset page buffer. FEMR: 1000_0001 FECR:0000_0010

Step 3. Select page buffer. FEMR:1000_1001

Step 4. Write 'h00 to page buffer. (Data value is not important.)

Step 5. Set erase mode and select OTP area. FEMR:1001_0101

Step 6. Set page address. FEARH:FEARM:FEARL=20'hx_xxxx

Step 7. Set FETCR.

Step 8. Start erase. FECR:0000_1011

Step 9. Insert one NOP operation

Step 10. Read FESR until PEVBSY is 1.

15.4.1.9 Flash program verify mode

Step 1. Enable program mode.

Step 2. Set program verify mode. FEMR:1010_0011

Step 3. Read data from Flash.

15.4.1.10 Flash program verify mode

Step 1. Enable program mode.

Step 2. Set program verify mode. FEMR:1010_0011

Step 3. Read data from Flash.

15.4.1.11 OTP program verify mode

Step 1. Enable program mode.

Step 2. Set program verify mode. FEMR:1010_0111

Step 3. Read data from Flash.

15.4.1.12 Flash erase verify mode

Step 1. Enable program mode.

Step 2. Set erase verify mode. FEMR:1001_0011

Step 3. Read data from Flash.

15.4.1.13 Flash page buffer read

Step 1. Enable program mode.

Step 2. Select page buffer. FEMR:1000_1001

Step 3. Read data from Flash.

15.4.2 Summary of Flash Program/Erase Mode

Operation mode		Description
FLASH	Flash read	Read cell by byte.
	Flash write	Write cell by bytes or page.
	Flash page erase	Erase cell by page.
	Flash bulk erase	Erase the whole cells.
	Flash program verify	Read cell in verify mode after programming.
	Flash erase verify	Read cell in verify mode after erase.
	Flash page buffer load	Load data to page buffer.

Table 15.3 Operation Mode

15.5 Mode entrance method of ISP and byte-parallel mode

15.5.1 Mode entrance method for ISP

TARGET MODE	DSDA	DSCL	DSDA
OCD(ISP)	‘hC	‘hC	‘hC

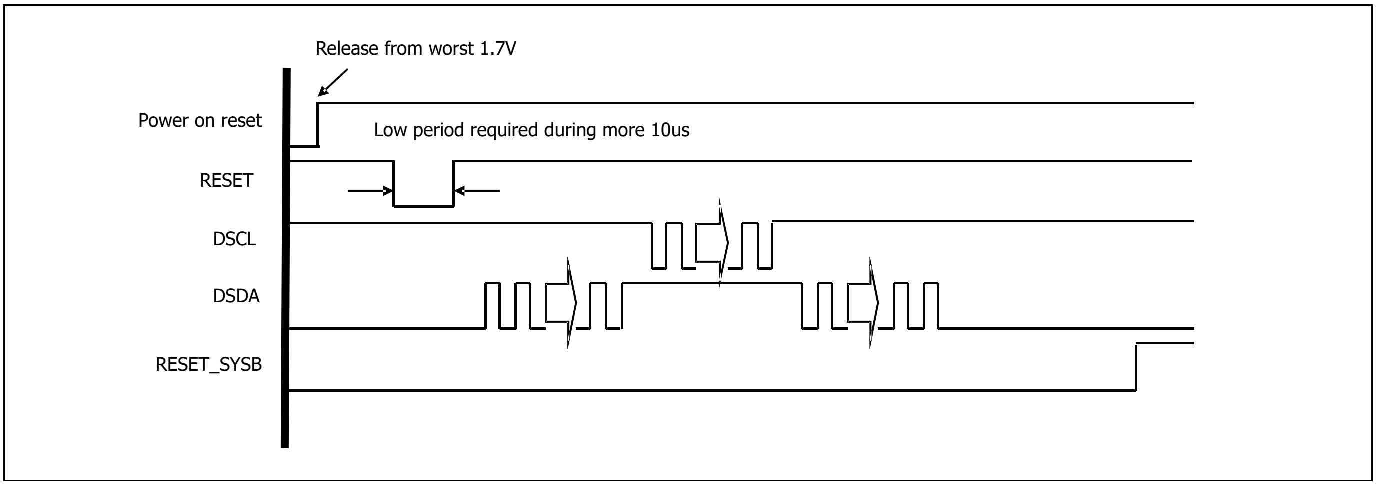


Figure 15.5 ISP mode

15.6 Security

MC96F1206 provides Lock bits which can be left unprogrammed (“0”) or can be programmed (“1”) to obtain the additional features listed in

Table 15.4. The Lock bits can be erased to “0” with only the bulk erase command and a value of more than 0x80 at FETCR.

LOCK MODE	USER MODE								ISP/PMODE							
	FLASH				OTP				FLASH				OTP			
LOCKF	R	W	PE	BE	R	W	PE	BE	R	W	PE	BE	R	W	PE	BE
0	O	O	O	X	X	X	X	X	O	O	O	O	O	O	O	O
1	O	O	O	X	X	X	X	X	X	X	X	O	O	X	X	O

Table 15.4 Security policy using lock-bits

- LOCKF: Lock bit of Flash memory
- R: Read
- W: Write
- PE: Page erase
- BE: Bulk Erase
- O: Operation is possible.
- X: Operation is impossible.

16 Configure option

16.1 Configure option Control Register

FUSE_CFG0 (Pseudo-Configure Data)

7	6	5	4	3	2	1	0
BSIZE[1]	BSIZE[0]	-	-	RSTEN	LOCKB	-	LOCKF
R	R	-	-	R	R	-	R

Initial value : 00H

BSIZE[1:0] Select Specific Area for Write Protection.
NOTE) When LOCKB is set, it's applied.

00 000h~7FFh (2KB)
01 000h~9FFh (2.5KB)
10 000h~BFFh (3KB)
11 000h~DFFh (3.5KB)

RSTEN Select RESETB pin.

0 Enable RESETB pin. (default)
1 Disable RESETB pin.

LOCKB Select Code Write Protection with Specific Area

0 Disable Code Write Protection
1 Enable Code Write Protection

LOCKF Select Code Read Protection.

0 Disable Code Read Protection
1 Enable Code Read Protection

17 APPENDIX

A. Instruction Table

Instructions are either 1, 2 or 3 bytes long as listed in the 'Bytes' column below.

Each instruction takes either 1, 2 or 4 machine cycles to execute as listed in the following table. 1 machine cycle comprises 2 system clock cycles.

ARITHMETIC				
Mnemonic	**Description**	**Bytes**	**Cycles**	**Hex code**
ADD A,Rn	Add register to A	1	1	28-2F
ADD A,dir	Add direct byte to A	2	1	25
ADD A,@Ri	Add indirect memory to A	1	1	26-27
ADD A,#data	Add immediate to A	2	1	24
ADDC A,Rn	Add register to A with carry	1	1	38-3F
ADDC A,dir	Add direct byte to A with carry	2	1	35
ADDC A,@Ri	Add indirect memory to A with carry	1	1	36-37
ADDC A,#data	Add immediate to A with carry	2	1	34
SUBB A,Rn	Subtract register from A with borrow	1	1	98-9F
SUBB A,dir	Subtract direct byte from A with borrow	2	1	95
SUBB A,@Ri	Subtract indirect memory from A with borrow	1	1	96-97
SUBB A,#data	Subtract immediate from A with borrow	2	1	94
INC A	Increment A	1	1	04
INC Rn	Increment register	1	1	08-0F
INC dir	Increment direct byte	2	1	05
INC @Ri	Increment indirect memory	1	1	06-07
DEC A	Decrement A	1	1	14
DEC Rn	Decrement register	1	1	18-1F
DEC dir	Decrement direct byte	2	1	15
DEC @Ri	Decrement indirect memory	1	1	16-17
INC DPTR	Increment data pointer	1	2	A3
MUL AB	Multiply A by B	1	4	A4
DIV AB	Divide A by B	1	4	84
DA A	Decimal Adjust A	1	1	D4

LOGICAL				
Mnemonic	**Description**	**Bytes**	**Cycles**	**Hex code**
ANL A,Rn	AND register to A	1	1	58-5F
ANL A,dir	AND direct byte to A	2	1	55
ANL A,@Ri	AND indirect memory to A	1	1	56-57
ANL A,#data	AND immediate to A	2	1	54
ANL dir,A	AND A to direct byte	2	1	52
ANL dir,#data	AND immediate to direct byte	3	2	53
ORL A,Rn	OR register to A	1	1	48-4F
ORL A,dir	OR direct byte to A	2	1	45
ORL A,@Ri	OR indirect memory to A	1	1	46-47
ORL A,#data	OR immediate to A	2	1	44
ORL dir,A	OR A to direct byte	2	1	42
ORL dir,#data	OR immediate to direct byte	3	2	43
XRL A,Rn	Exclusive-OR register to A	1	1	68-6F
XRL A,dir	Exclusive-OR direct byte to A	2	1	65

XRL A, @Ri	Exclusive-OR indirect memory to A	1	1	66-67
XRL A,#data	Exclusive-OR immediate to A	2	1	64
XRL dir,A	Exclusive-OR A to direct byte	2	1	62
XRL dir,#data	Exclusive-OR immediate to direct byte	3	2	63
CLR A	Clear A	1	1	E4
CPL A	Complement A	1	1	F4
SWAP A	Swap Nibbles of A	1	1	C4
RL A	Rotate A left	1	1	23
RLC A	Rotate A left through carry	1	1	33
RR A	Rotate A right	1	1	03
RRC A	Rotate A right through carry	1	1	13

DATA TRANSFER				
Mnemonic	**Description**	**Bytes**	**Cycles**	**Hex code**
MOV A,Rn	Move register to A	1	1	E8-EF
MOV A,dir	Move direct byte to A	2	1	E5
MOV A,@Ri	Move indirect memory to A	1	1	E6-E7
MOV A,#data	Move immediate to A	2	1	74
MOV Rn,A	Move A to register	1	1	F8-FF
MOV Rn,dir	Move direct byte to register	2	2	A8-AF
MOV Rn,#data	Move immediate to register	2	1	78-7F
MOV dir,A	Move A to direct byte	2	1	F5
MOV dir,Rn	Move register to direct byte	2	2	88-8F
MOV dir,dir	Move direct byte to direct byte	3	2	85
MOV dir,@Ri	Move indirect memory to direct byte	2	2	86-87
MOV dir,#data	Move immediate to direct byte	3	2	75
MOV @Ri,A	Move A to indirect memory	1	1	F6-F7
MOV @Ri,dir	Move direct byte to indirect memory	2	2	A6-A7
MOV @Ri,#data	Move immediate to indirect memory	2	1	76-77
MOV DPTR,#data	Move immediate to data pointer	3	2	90
MOVC A,@A+DPTR	Move code byte relative DPTR to A	1	2	93
MOVC A,@A+PC	Move code byte relative PC to A	1	2	83
MOVX A,@Ri	Move external data(A8) to A	1	2	E2-E3
MOVX A,@DPTR	Move external data(A16) to A	1	2	E0
MOVX @Ri,A	Move A to external data(A8)	1	2	F2-F3
MOVX @DPTR,A	Move A to external data(A16)	1	2	F0
PUSH dir	Push direct byte onto stack	2	2	C0
POP dir	Pop direct byte from stack	2	2	D0
XCH A,Rn	Exchange A and register	1	1	C8-CF
XCH A,dir	Exchange A and direct byte	2	1	C5
XCH A,@Ri	Exchange A and indirect memory	1	1	C6-C7
XCHD A,@Ri	Exchange A and indirect memory nibble	1	1	D6-D7

BOOLEAN				
Mnemonic	**Description**	**Bytes**	**Cycles**	**Hex code**
CLR C	Clear carry	1	1	C3
CLR bit	Clear direct bit	2	1	C2
SETB C	Set carry	1	1	D3
SETB bit	Set direct bit	2	1	D2
CPL C	Complement carry	1	1	B3
CPL bit	Complement direct bit	2	1	B2
ANL C,bit	AND direct bit to carry	2	2	82
ANL C,/bit	AND direct bit inverse to carry	2	2	B0

ORL C,bit	OR direct bit to carry	2	2	72
ORL C,/bit	OR direct bit inverse to carry	2	2	A0
MOV C,bit	Move direct bit to carry	2	1	A2
MOV bit,C	Move carry to direct bit	2	2	92

BRANCHING				
Mnemonic	**Description**	**Bytes**	**Cycles**	**Hex code**
ACALL addr 11	Absolute jump to subroutine	2	2	11→F1
LCALL addr 16	Long jump to subroutine	3	2	12
RET	Return from subroutine	1	2	22
RETI	Return from interrupt	1	2	32
AJMP addr 11	Absolute jump unconditional	2	2	01→E1
LJMP addr 16	Long jump unconditional	3	2	02
SJMP rel	Short jump (relative address)	2	2	80
JC rel	Jump on carry = 1	2	2	40
JNC rel	Jump on carry = 0	2	2	50
JB bit,rel	Jump on direct bit = 1	3	2	20
JNB bit,rel	Jump on direct bit = 0	3	2	30
JBC bit,rel	Jump on direct bit = 1 and clear	3	2	10
JMP @A+DPTR	Jump indirect relative DPTR	1	2	73
JZ rel	Jump on accumulator = 0	2	2	60
JNZ rel	Jump on accumulator ≠0	2	2	70
CJNE A,dir,rel	Compare A, direct jne relative	3	2	B5
CJNE A,#d,rel	Compare A, immediate jne relative	3	2	B4
CJNE Rn,#d,rel	Compare register, immediate jne relative	3	2	B8-BF
CJNE @Ri,#d,rel	Compare indirect, immediate jne relative	3	2	B6-B7
DJNZ Rn,rel	Decrement register, jnz relative	2	2	D8-DF
DJNZ dir,rel	Decrement direct byte, jnz relative	3	2	D5

MISCELLANEOUS				
Mnemonic	**Description**	**Bytes**	**Cycles**	**Hex code**
NOP	No operation	1	1	00

ADDITIONAL INSTRUCTIONS (selected through EO[7:4])				
Mnemonic	**Description**	**Bytes**	**Cycles**	**Hex code**
MOVC @(DPTR++),A	M8051W/M8051EW-specific instruction supporting software download into program memory	1	2	A5
TRAP	Software break command	1	1	A5

In the above table, an entry such as E8-EF indicates a continuous block of hex op-codes used for 8 different registers, the register numbers of which are defined by the lowest three bits of the corresponding code. Non-continuous blocks of codes, shown as 11→F1 (for example), are used for absolute jumps and calls, with the top 3 bits of the code being used to store the top three bits of the destination address.

The CJNE instructions use the abbreviation #d for immediate data; other instructions use #data.

B. Package relation

	MC96F1206 (16SOPN)	**MC96F1206 (20-Pin)**
Pin count	16	20
Max I/O	14	18
Difference (removed functions on standard MC96F1206)	P07, P10 ~ P12	

NOTE) The P07, P10-P12 pins should be selected as a push-pull output or an input with pull-up resistor by software control when the 16SOPN package is used.

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