Application Note

GUIDE OF POWER ON RESET

AN0026 Ver 1.0

Document information

Info	Content
Keywords	ABOV M8051/CM8051 Device
Abstract	This application note describes the Power on reset behavior to prevent malfunction when using the ABOV M8051/CM8051 device.

AE 1 Team
ABOV SEMICONDUCTOR

`

Revision history

Version	Date	Revision list
V1.0	18.07.06	Initial preliminary version

1. Overview

When the power rised of the device, POR (Power on reset) has a function to reset the device. POR is a built-in circuit to generate a device initialization signal so that the device can always start at the same condition every time the device is powered on.

External reset terminal for device reset and OCD port (DSDA, DSCL) can be used as general I / O, but appropriate external circuit is required to prevent POR operation. This document describes how to prevent start-up and malfunction of the device during POR.

2. Boot Process when Power-on

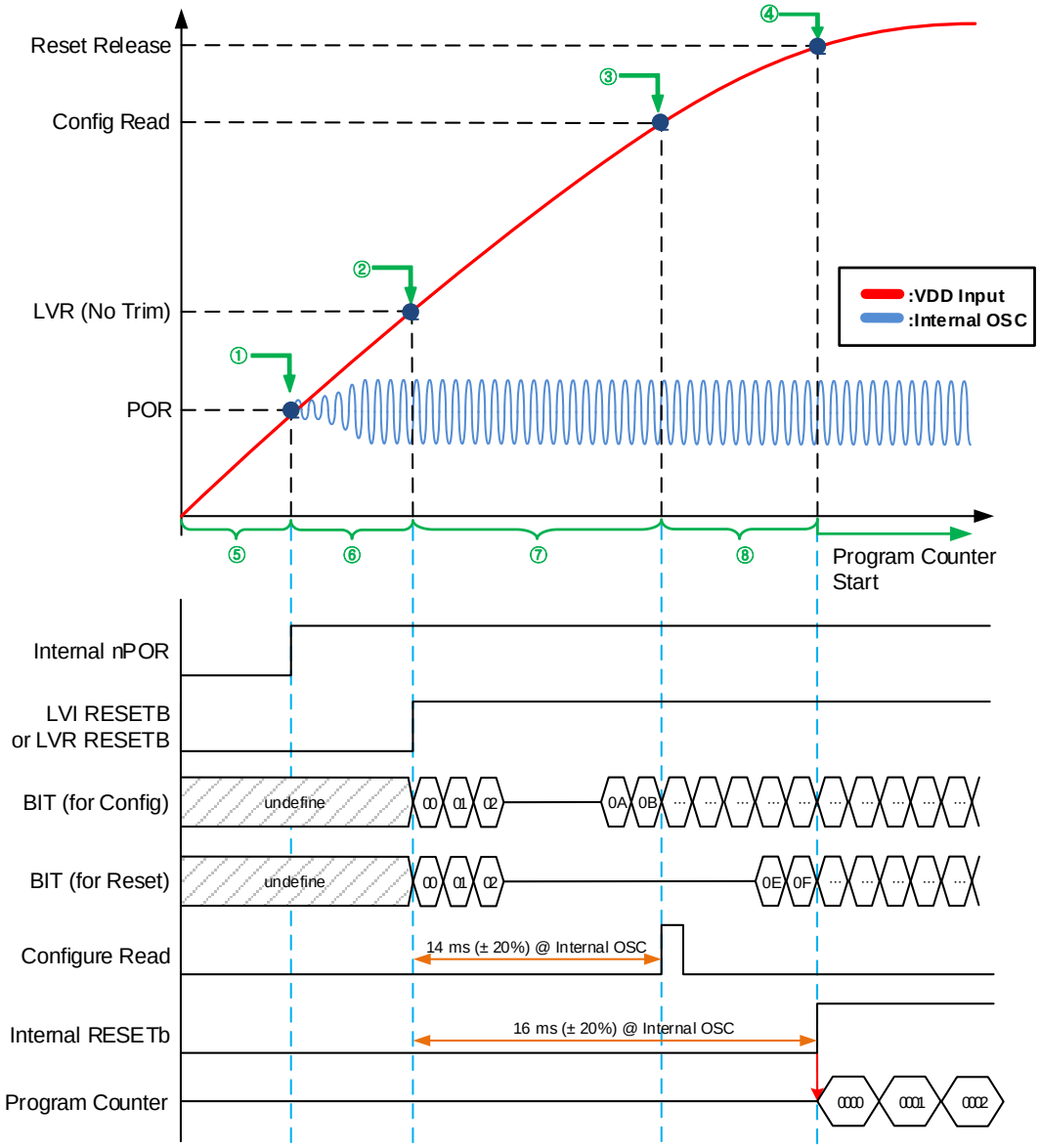


Figure 1. Boot Process when Power on

Note) BIT count, Configure Read Time, and Internal ResetB Time may be different for each device.

When the ABOV M8051 device reaches the POR voltage (①), the internal clock starts to operate and the built-in analog block prepares to initialize the device. When the VDD voltage rises to the LVR voltage (②), the Internal Reset state inside the device is released and the BIT (Basic Interval Timer) Count starts for configure read. In this case, there is an inaccuracy because the LVR voltage is not applied to the internal reference LDO trimming, and the VDD rising slew rate needs to be limited within a certain range for correct operation in design. The pre-trim LVR voltage may vary from device to device, but is usually within 1.4V to 2.0V. This value is adjusted to factory tested Trim value in Configure Read (③).

Configure read (③) and reset release (④) operate based on BIT (Basic Interval Timer) value from LVR point (②) instead of current VDD voltage value. Therefore, if the VDD rising slew rate of the interval from LVR (②) to Configure read (③) (⑦ in Figure 1) is less than about 0.025V / ms, erroneous operation may occur. This problem occurs because the Configure read does not meet the flash read voltage required to set the factory test trim value and internal register initialization value. If you have a slow VDD rising slew rate in POR in your application system, you can prevent the malfunction by delaying the LVR reset release (②) by reinforcing circuit to increase slew rate or by adding RC filter to external reset pin.

Also, by setting a sufficiently high LVIR (Low voltage Indicate reset), reset can be generated when VDD is below a certain voltage, and the reset release can be delayed until the LVIR voltage is exceeded. However, this method is used as an auxiliary protection measure because the inaccuracy to the LVIR voltage is higher than usual when the Configure read is not performed normally.

(T_A = -40°C ~ +85°C, VSS = 0V)

Parameter	Symbol	Conditions	MIN	TYP	MAX	Unit
POR Release Level	V_{POR}	–	–	1.1	–	V
VDD Voltage Rising Time	t_R	0V to 2.0V	0.05	–	30.0	V/ms
POR Current	I_{POR}	–	–	0.2	–	uA

Table 1. Example of Power-on Reset Characteristics

3. H/W design guide to prevent abnormal POR

In the Power-on Boot Process of the ABOV M8051 device, the three types of ports except I / O need to be managed. This terminal is VDD / GND which is directly powered, OCD terminal (DSCL, DSDA) used for Device Write and Debugging, and External Reset terminal used for external RESET input.

3.1 VDD/GND

For the microprocessor and other devices in the system to function correctly, it is also necessary to monitor the supply voltage during operations. Voltage drops or glitches on the power supply lines, can cause unwanted changes in the internal registers, which can lead to instructions being incorrectly executed, incorrect output signals and errors in the operations results. If noise is applied to the VDD rising slope due to external factors during the POR, the microprocessor may malfunction because the microprocessor continues to operate and does not recognize that the voltage has fallen below the threshold due to the internal RC time constants. Therefore, VDD / GND requires a power capacitor for VDD drop and a decoupling capacitor for high frequency noise. Normally, electrolytic / tantalum capacitors of 10uf / 9V or more are recommended for power capacitors and multilayer ceramic capacitors of 0.1uF or more are recommended for decoupling capacitors. Decoupling capacitors should be placed as close as possible to the microprocessor.

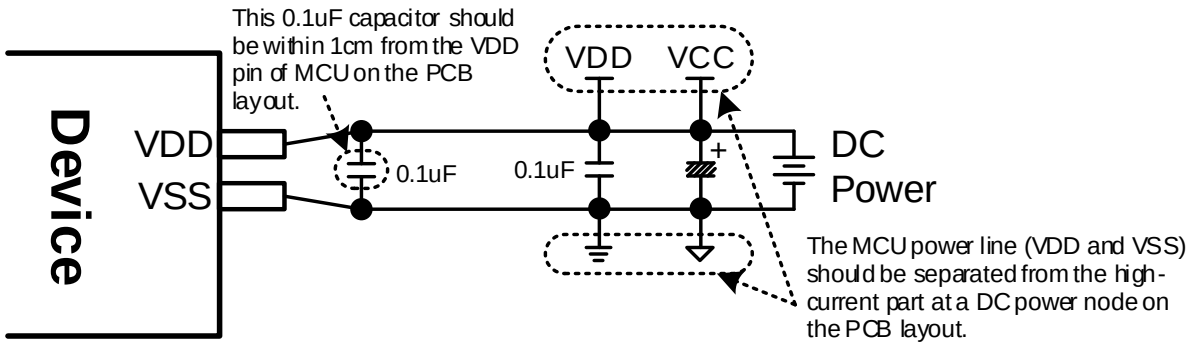
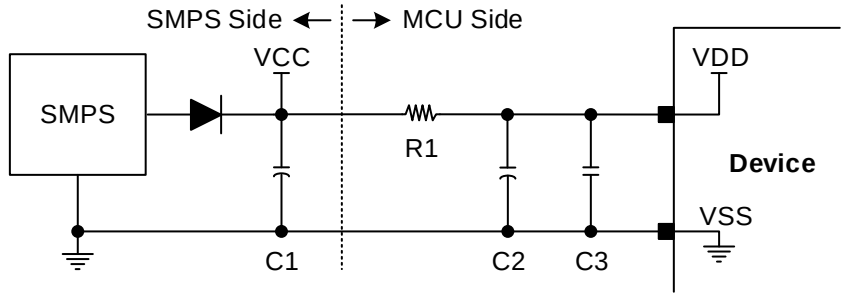


Figure 2. Recommended Power circuit part when using DC power.

When an application uses AC power, it may be more susceptible to noise in the transient state, and additional circuit reinforcement may be required.



1. The C1 capacitor is to flatten out the voltage of the SMPS power, VCC.
   √ Recommended C1: 470uF/25V more.
2. The R1 and C2 are the RC filter for VDD and suppress the ripple of VCC.
   √ Recommended R1: 10Ω - 20Ω
   √ Recommended C2: 47uF/25V more
   √ The R1 and C2 should be as close by the C3 as possible.
3. The C3 capacitor is used for temperature compensation because an electrolytic capacitor becomes worse characteristics at low temperature.
   √ Recommended C3: ceramic capacitor 2.2uF more
   √ The C3 should be within 1cm from VDD pin of MCU on the PCB layout.
4. The above circuit is recommended to improve noise immunity (EFT, Surge, ESD, etc) when the SMPS supplies the VDD of MCU.

Figure 3. Recommended Power circuit part when using AC power.

3.2 OCD Port (DSCL, DSDA)

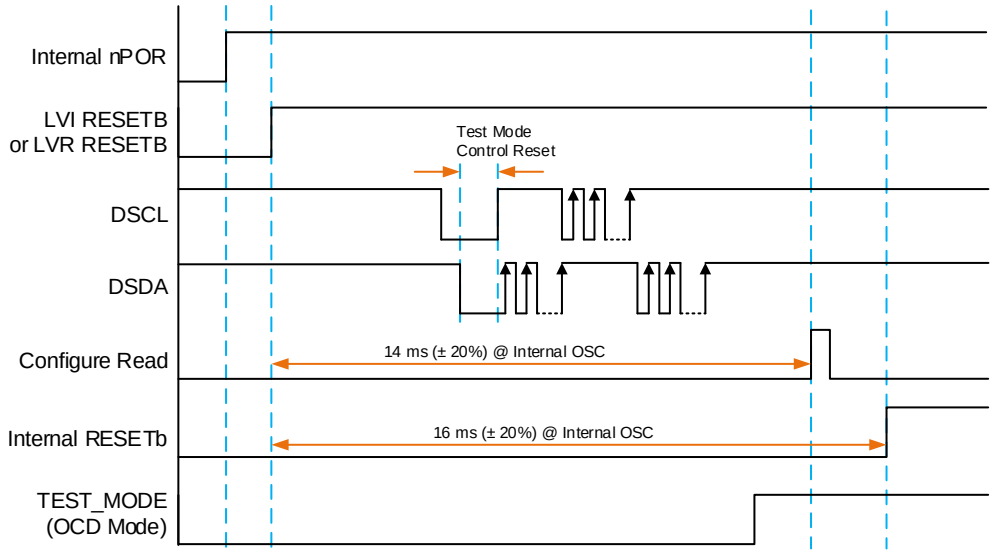


Figure 4. Test Mode (OCD mode) Sequence

The OCD port is used for flash program writing and device debugging. The device has a section that determines whether to use it in that mode of POR. This is done when the internal reset is cleared and waiting to clear Configure Read and Internal Reset. If the internal reset is cleared and DSCL and DSDA wait for a period of time from internal pull-up 'high' to 'low', the internal controller for entering test mode is initialized. Then, when DSCA and DSCA appointed communication, the test mode is entered.

As described above, OCD port is a port for special purpose. Even if it is used as Normal GPIO in User Program, it is necessary to limit the state to prevent malfunction during POR. Therefore, it is recommended to connect Pull-up Resistor to the outside of OCD Port and to fix OCD Port input to VDD / GND at POR. If it is difficult to apply pull-up on the circuit, install at least 0.1uf bypass capacitor to prevent Floating state at POR. However, if you install a bypass cap, you can not use on board writing and OCD Debugger.

3.3 External Reset

The External Reset pin can be set in the Configure option, and can be set during Flash write in the Write device and OCD mode.

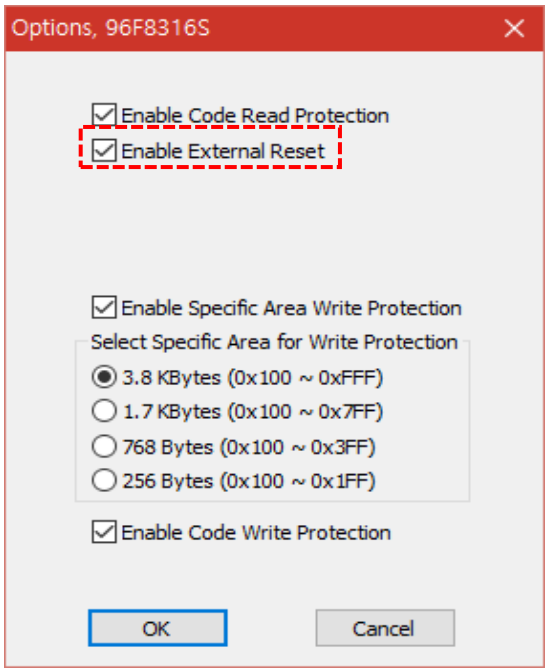


Figure 5. Example of option selection

External RESETB is internally input via the Schmitt trigger circuit. The reset pin is applied when it is kept 'low' for 10us or more within the operating range. After having stabilization time of about 10 ~ 20ms from the recognition time of RESETB, it transmits the signal for resetting the actual MCU to the inside.

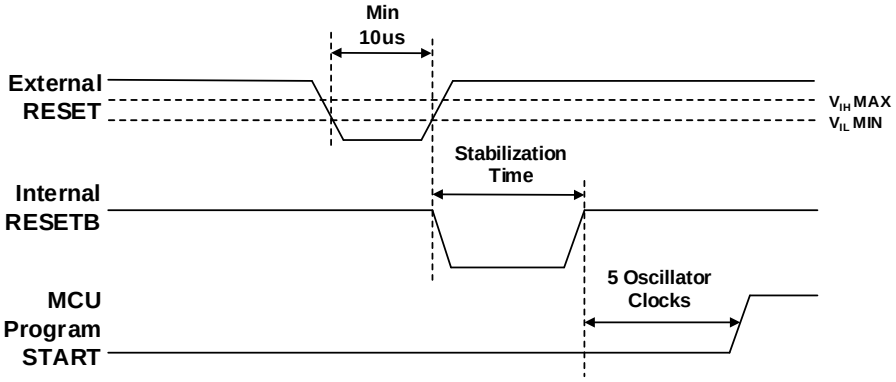


Figure 6. External Reset Time

External RESETB at POR operates as Initial Value until Configure Read. If the initial value is Enable RESETB and the input is 'Low' with External RESETB, the Device will remain in the Internal RESET state until the corresponding Pin becomes 'High'.

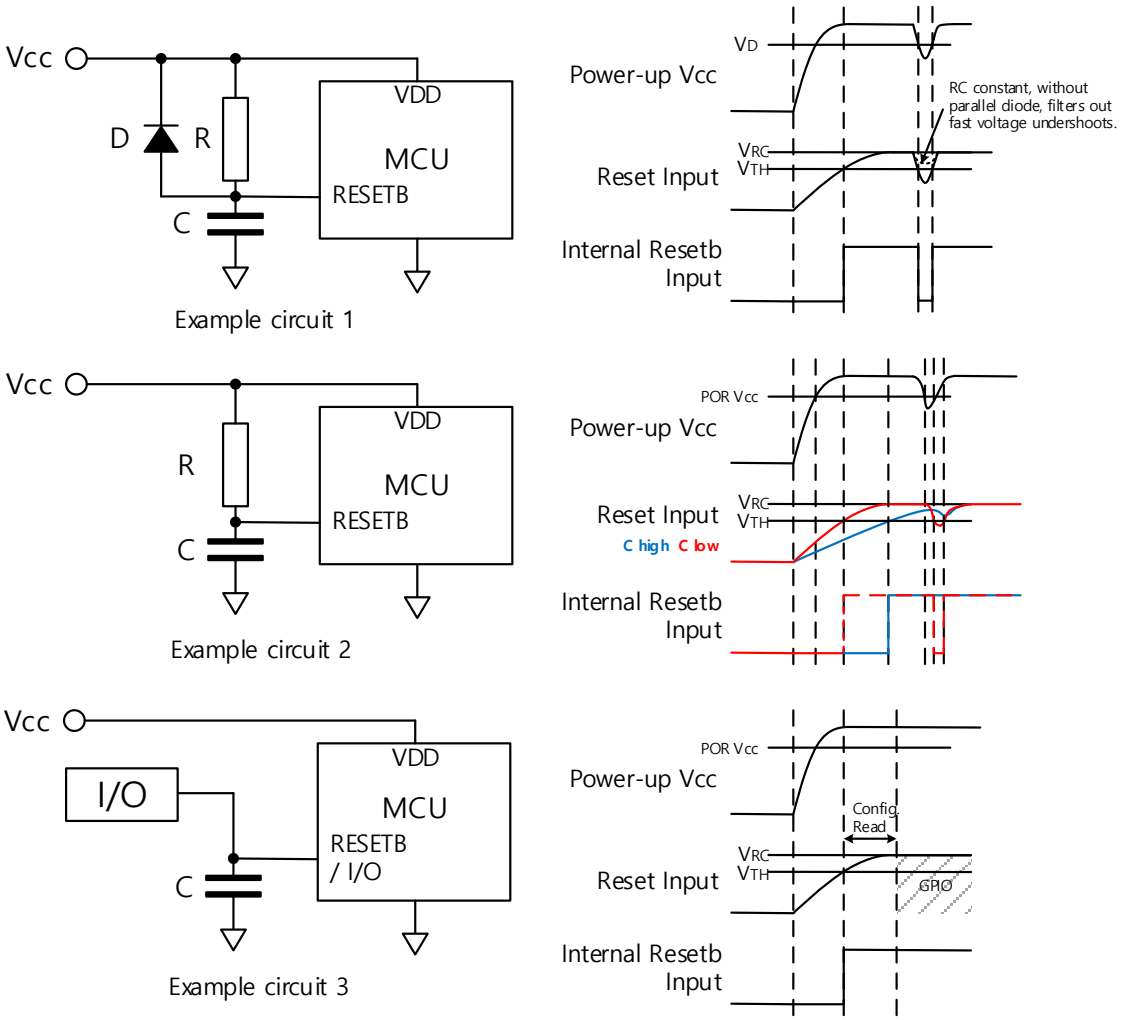


Figure 7. External Reset Pin Circuit

Even if the initial value is Disable RESETB, it affects Internal Reset prior to RESET. Therefore, when using the pin as GPIO, 0.1uF should be mounted like Figure7 example circuit 3. This prevents noise from being applied to the corresponding pins during POR, and to prevent the reset circuit from malfunction.

When used as an external RESETB, an RC filter can be added to the corresponding pin to increase the reset stabilization time when the POR is rising. (Figure 7. example circuit 2) However, the response to fast undershoot may be weak due to the time constant of the RC delay. If the power fluctuation due to the in-rush current of the power source part of the application is severe at the time of POR, the response time according to the power change can be improved by using the R-C-diode filter (Figure 7. example circuit 1).

Table of contents